Hardware Manual
for
XMC-MA4

Part Number: 15602-00000-A12
Cage Code: 4RK27 • NAICS: 334210

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CUSTOMER NOTES:

Revision Control History

Rev A12 Release Date: 17 January 2023

Note to the Reader and End-User:

Contact:

We welcome comments and suggestions. Please contact us at 888-429-1553 (toll free in US) or 505-994-3111 or visit our web site for support submit forms at www.altadt.com.

XMC-MA4
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XMC-MA4 Hardware Manual

Introduction

This manual provides detailed hardware information on the XMC-MA4 interface card.

In addition to this information, the reader may also want to reference the following documents provided on the CD and our Web Site

- **AltaCore**™ Specifications and User Manual: Detailed description of the 1553 protocol engine of the card. Most people do not need this detail and will mainly reference the **AltaAPI** manual for their application development.
- **AltaAPI**™ User's Manual: Detailed description of the application program interface (API) and device drivers of this software package.
- **AltaView**™ User's Manual: AltaView is the latest 1553 analyzer on the market and this manual details the usage of the product.
- **AltaRTVal**™ User's Manual: This manual details the usage of AltaRTVal, which is an automated program to run AS4111/4112 RT Validation and Production Test Plans.
- 1553 Tutorial and Reference, and 1553B Standard. These documents provide a detailed review of the 1553 standard, which is required for proper usage of this product. **SEE THIS DOCUMENT FOR WIRE & CABLING INFORMATION OF 1553 BUSSES – THIS IS REQUIRED FOR PROPER BUS OPERATIONS.**

ESD and General Handling of Computer Interface Cards

The Alta warranty requires that the product be handled with proper ESD controls. The JEDEC standard on ESD handling, JESD625, is available for free download at www.jedec.org. Please follow the standard's guideline for proper ESD handling methods. At a minimum the following guidelines should be followed:

- Avoid carpets in cool, dry areas.
- Leave the card in its anti-static packaging until ready to be installed.
- Dissipate static electricity before handling the card by touching a grounded metal object, such as the metal chassis of the system (the system should be plugged-in, but turned-off).
- Use antistatic devices, such as wrist straps and floor mats.
- Always hold the card by its edges. Avoid touching the components or connectors.
- Be sure to align card edge or assembly cable connector pins before installation. Misaligned connectors can cause damage to the card or system, especially at power-on.
- Take care when connecting or disconnecting cables. When disconnecting a cable, always pull on the cable connector, not on the cable itself.

XMC-MA4 Description

The Alta XMC-MA4 card is a standard XMC module designed for commercial and rugged, conduction cooled installations. The main difference between these two configurations is the P4 or P6 connector is not installed on standard commercial models, and for conduction cooled models, the front panel is not installed, but the P4 or P6 connector is for rear panel I/O access. The customer has various order options for commercial rear-panel (P4 or P6), extended temperature (industrial grade) components and conformal coating.

The XMC-MA4 front panel models include a transition cable assembly for 1553\ARINC and general I/O connections. Rear panel (conduction cooled or special order rear panel) models do not have a transition cable assembly (the customer constructs a custom cable assembly for the backplane of their system).

Card Level Specifications

- Single-Wide XMC card
- PCI Express 1.1 Compliant with MSI Support
- Up to Five MIL-STD-1553 Channels
    - Transformer Coupled Stub Interface Standard
    - Direct Coupled Stub Interface available upon request
- Up to 8 ARINC Channels (4 RX/TX Shared, 4 RX)
    - Note: Shared RX/TX channels could have severe RX voltage drain when not powered. Use dedicated RX only channels for embedded or critical systems. (See A429 Shared Channels Section for more detail.)
- 512 Kbyte RAM per 1553 Channel
- 512 Kbyte RAM for ARINC Bank
- IRIG-B Receiver (DC or AM)
- 6 Single-Ended Bi-Directional Avionics Discretes
    - 1760 Ext RT Addressing
- One RS-485 Discretes that can be used as (Ext Clock)
- One LVTTL Input and Output Trigger per Device Channel (6 Total)
- One TTL Bi-Directional Discrete (Ext Clock)
- Two Temperature Sensors
- Front Panel or Rear Panel (P4 or P6) I/O Option
- 9.0 Watts Max (Five/Eight Channel @ 100% Bus Loading)
- Operating Temperature range: 0-70C Standard
    - -40 to +85C Extended Temp Parts with –E or - C Option (as applicable).
- Relative humidity: 5 to 95% (non-condensing).
- RoHS Compliant

Power Specifications

Table 1. Idle Power

IDLE			
Channel	Input Voltage (V)	Amps (I)	Total Power (W)
N/A	3.3V	0.725	2.9925
	+12V	0.025	
	-12V	0.025	

Table 2. 50% Bus Loading Power

50% Bus Loading With 4 Channel A429			
Channel	Input Voltage (V)	Amps (I)	Total Power (W)
CH1	3.3V	0.9	3.57
	+12V	0.025	
	-12V	0.025	
CH2	3.3V	1.075	4.1475
	+12V	0.025	
	-12V	0.025	
CH3	3.3V	1.275	4.8075
	+12V	0.025	
	-12V	0.025	
CH4	3.3V	1.45	5.385
	+12V	0.025	
	-12V	0.025	
CH5	3.3V	1.625	5.9625
	+12V	0.025	
	-12V	0.025	

Table 3. 95% Bus Loading Power

95% Bus Loading With 4 Channel A429			
Channel	Input Voltage (V)	Amps (I)	Power (W)
CH1	3.3V	1.075	4.1475
	+12V	0.025	
	-12V	0.025	
CH2	3.3V	1.45	5.385
	+12V	0.025	
	-12V	0.025	
CH3	3.3V	1.8	6.54
	+12V	0.025	
	-12V	0.025	
CH4	3.3V	2.125	7.6125
	+12V	0.025	
	-12V	0.025	
CH5	3.3V	2.45	8.685
	+12V	0.025	
	-12V	0.025	

MTBF

The MTBF numbers shown below are highly conservative calculations and should be considered absolute worst case for the environment they are calculated for. Please contact your Local Sales Representative or Alta Technical Support for additional information regarding any concerns or questions that may arise regarding MTBF for this board.

Environment: Ground Benign, 25C

- Transformer Coupled Stub Interface Standard
- Direct Coupled Stub Interface available upon request

1553 Channel Count*	MTBF
1/5	193,413
2/5	183,367
4/5	166,104
5/5	158,638

Environment: Ground Benign, 25C

Table 5. MTBF Rear (P4\P6) I/O

1553 Channel Count*	MTBF
1/5	193,094
2/5	183,077
4/5	165,869
5/5	158,423

*Note: MTBF numbers were calculated with Four Shared and Eight RX ARINC Channels

XMC-MA4 Photographs

The following pictures show the front side and back side of a standard commercial card.

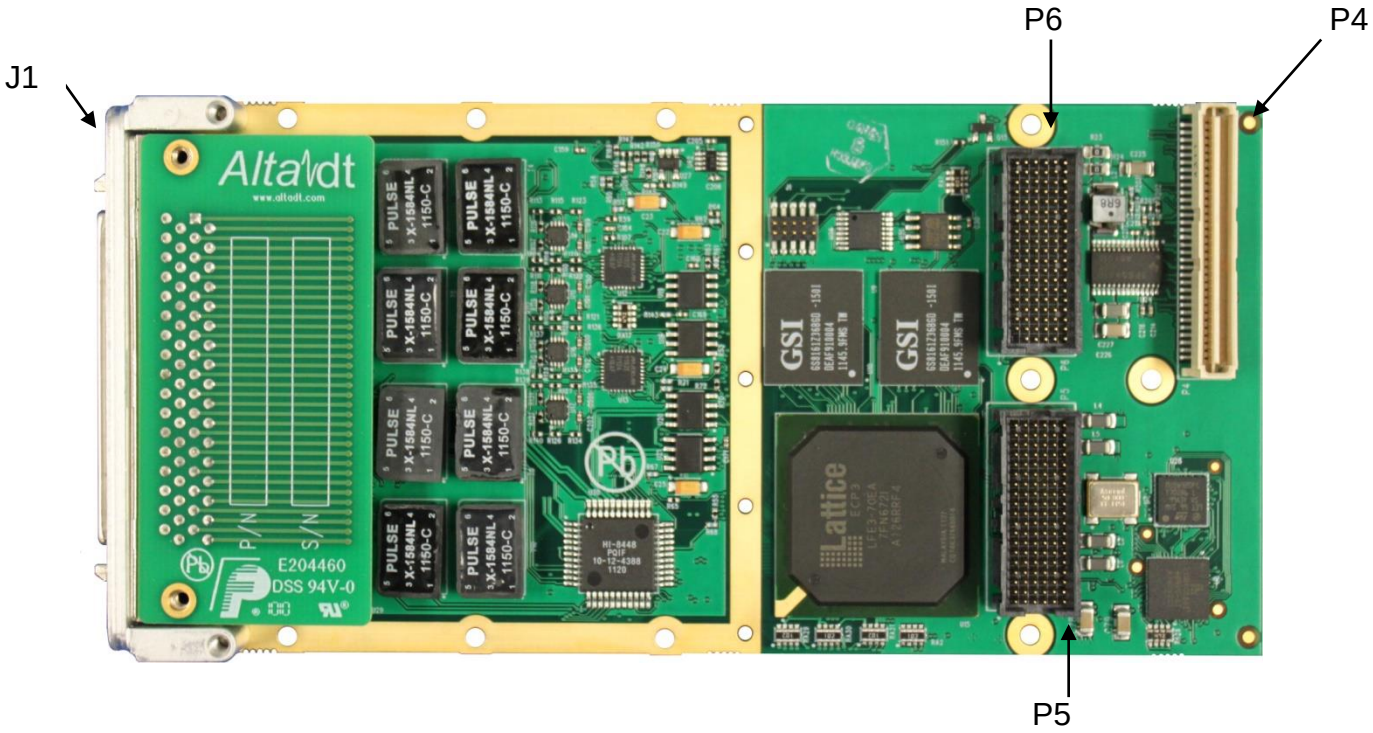

Figure 1. XMC-MA4 Front Side

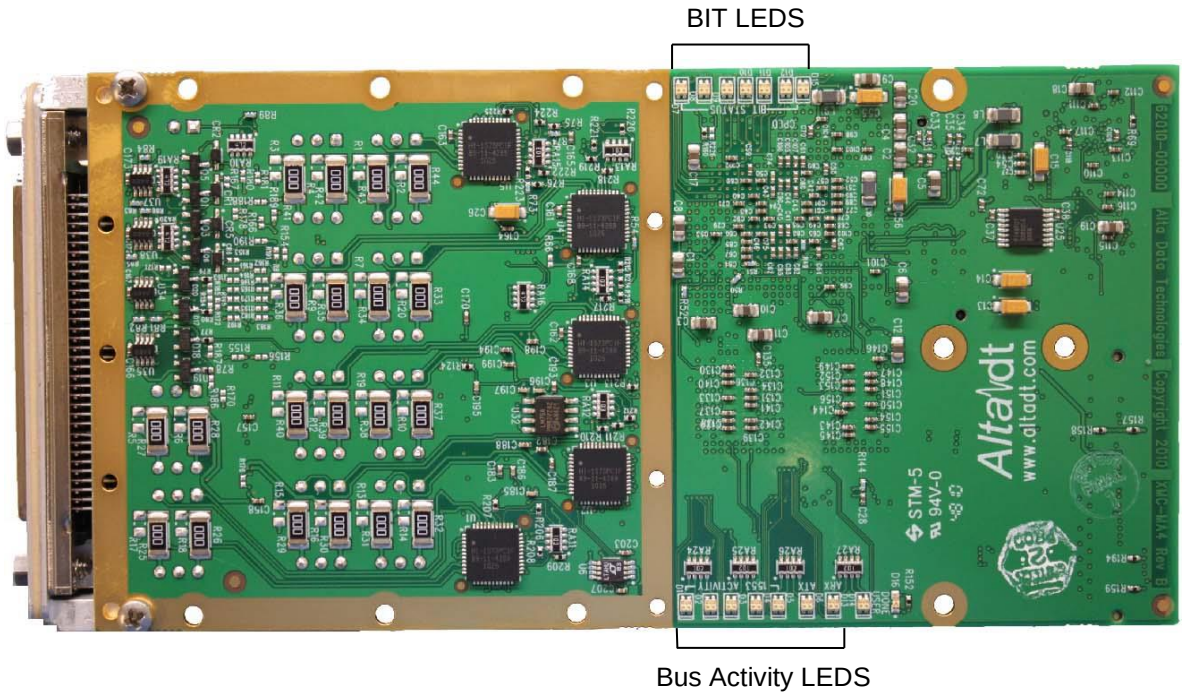

Figure 2. XMC-MA4 Back Side

LED Descriptions

Table 6. LED Descriptions

LED	Name	Description
D1	Channel One 1553 Bus Activity	Green=No Errors, Red=Errors Detected
D2	Channel Two 1553 Bus Activity	Green=No Errors, Red=Errors Detected
D3	Channel Three 1553 Bus Activity	Green=No Errors, Red=Errors Detected
D4	Channel Four 1553 Bus Activity	Green=No Errors, Red=Errors Detected
D5	Channel Five 1553 Bus Activity	Green=No Errors, Red=Errors Detected
D6	Channel ARINC TX Activity	Green=No Errors, Red=Errors Detected
D13	Channel ARINC RX Activity	Green=No Errors, Red=Errors Detected
D7	Channel One BIT Status	Green=No Errors, Red=Errors Detected
D8	Channel Two BIT Status	Green=No Errors, Red=Errors Detected
D9	Channel Three BIT Status	Green=No Errors, Red=Errors Detected
D10	Channel Four BIT Status	Green=No Errors, Red=Errors Detected
D11	Channel Four BIT Status	Green=No Errors, Red=Errors Detected
D12	Channel Four BIT Status	Green=No Errors, Red=Errors Detected
D14	User LED	Set on or off by the User – Red/Green/Amber
D15	Board Status	Green=No Error, Red=FPGA Load Error Amber= Power Supply Failure
D16	FPGA Loaded	Green=FPGA Loaded, Off=FPGA Not Loaded

J1 (Front Panel) and P4 (Rear Panel) Connector Pin-Outs

The following tables provide pin-outs for the J1 Front Panel, P4 and P6 Rear Panel connectors. P5 is a standard XMC VITA Pin-out. (See Appendix A for SCSI Cable Information).

Table 7: J1 Front Panel SCSI 3 Pin-Outs

SCSI Pin#	Signal	SCSI Pin#	Signal
1	1553 CH 1A+	35	1553 CH 1A-
2	1553 CH 1B+	36	1553 CH 1B-
3	1553 SHIELD	37	GND
4	TRIG IN 1	38	TRIG OUT 1
5	1553 CH 2A+	39	1553 CH 2A-
6	1553 CH 2B+	40	1553 CH 2B-
7	TRIG IN 2	41	TRIG OUT 2
8	1553 CH 3A+	42	1553 CH 3A-
9	1553 CH 3B+	43	1553 CH 3B-
10	1553 SHIELD	44	GND
11	TRIG IN 3	45	TRIG OUT 3
12	1553 CH 4A+	46	1553 CH 4A-
13	1553 CH 4B+	47	1553 CH 4B-
14	TRIG IN 4	48	TRIG OUT 4
15	1553 CH 5A+	49	1553 CH 5A-
16	1553 CH 5B+	50	1553 CH 5B-
17	TRIG IN 5	51	TRIG OUT 5
18	1553 SHIELD	52	GND
19	A429 RX1+/TX1+	53	A429 RX1-/TX1-
20	A429 RX2+/TX2+	54	A429 RX2-/TX2-
21	A429 RX3+/TX3+	55	A429 RX3-/TX3-
22	A429 RX4+/TX4+	56	A429 RX4-/TX4-
23	A429 RX5+	57	A429 RX5-
24	A429 RX6+	58	A429 RX6-
25	A429 RX7+	59	A429 RX7-
26	A429 RX8+	60	A429 RX8-
27	TRIG IN 6	61	TRIG OUT 6
28	SDISC1 / RTADDR_1	62	DDISC1+ (RS-485)
29	SDISC2 / RTADDR_2	63	DDISC1- (RS-485)
30	SDISC3 / RTADDR_3	64	GND
31	SDISC4 / RTADDR_4	65	EXT CLK I/O – TTL I/O
32	SDISC5 / RTADDR_5	66	~EXT RT ADD ENABLE
33	SDISC6 / RTADDR_P	67	GND
34	IRIG IN	68	IRIG GND

Table 8: P4 Rear Panel Pin-Outs

Pin#	Signal	Pin#	Signal
1	1553 CH 1A+	2	1553 CH 1B+
3	1553 CH 1A-	4	1553 CH 1B-
5	TRIG IN 1	6	TRIG IN 2
7	TRIG OUT 1	8	TRIG OUT 2
9	1553 CH 2A+	10	1553 CH 2B+
11	1553 CH 2A-	12	1553 CH 2B-
13	TRIG IN 3	14	1553 SHIELD
15	TRIG OUT 3	16	1553 SHIELD
17	1553 CH 3A+	18	1553 CH 3B+
19	1553 CH 3A-	20	1553 CH 3B-
21	TRIG IN 4	22	TRIG IN 5
23	TRIG OUT 4	24	TRIG OUT 5
25	1553 CH 4A+	26	1553 CH 4B+
27	1553 CH 4A-	28	1553 CH 4B-
29	1553 CH 5A+	30	1553 CH 5B+
31	1553 CH 5A-	32	1553 CH 5B-
33	A429 RX1+/TX1+	34	A429 RX2+/TX2+
35	A429 RX1-/TX1-	36	A429 RX2-/TX2-
37	A429 RX3+/TX3+	38	A429 RX4+/TX4+
39	A429 RX3-/TX3-	40	A429 RX4-/TX4-
41	A429 RX5+	42	A429 RX6+
43	A429 RX5-	44	A429 RX6-
45	A429 RX7+	46	A429 RX8+
47	A429 RX7-	48	A429 RX8-
49	TRIG IN 6	50	TRIG OUT 6
51	SDISC1 / RTADDR_1	52	GND
53	SDISC2 / RTADDR_2	54	DDISC1+ (RS-485)
55	SDISC3 / RTADDR_3	56	DDISC1- (RS-485)
57	SDISC4 / RTADDR_4	58	EXT CLK I/O – TTL I/O
59	SDISC5 / RTADDR_5	60	GND
61	SDISC6 / RTADDR_P	62	~EXT RT ADD ENABLE
63	IRIG IN	64	IRIG GND

Table 9: P6 Pin-Outs

Pin#	A	B	C	D	E	F
1	1553 CH 1B+	1553 CH 1B-	TRIG_IN1	1553 CH 1A+	1553 CH 1A-	TRIG_OUT1
2	GND	GND	TRIG_IN2	GND	GND	TRIG_OUT2
3	1553 CH 2B+	1553 CH 2B-	TRIG_IN3	1553 CH 2A+	1553 CH 2A-	TRIG_OUT3
4	GND	GND	1553_SHIELD	GND	GND	1553_SHIELD
5	1553 CH 3B+	1553 CH 3B-	TRIG_IN4	1553 CH 3A+	1553 CH 3A-	TRIG_OUT4
6	GND	GND	TRIG_IN5	GND	GND	TRIG_OUT5
7	1553 CH 4B+	1553 CH 4B-	N/C	1553 CH 4A+	1553 CH 4A-	N/C
8	GND	GND	N/C	GND	GND	N/C
9	1553 CH 5B+	1553 CH 5B-	N/C	1553 CH 5A+	1553 CH 5A-	N/C
10	GND	GND	N/C	GND	GND	N/C
11	A429 RX1-/TX1-	A429 RX1+/TX1+	TRIG_IN6	A429 RX2+/TX2+	A429 RX2-/TX2-	TRIG_OUT6
12	GND	GND	N/C	GND	GND	N/C
13	A429 RX3-/TX3-	A429 RX3+/TX3+	N/C	N/C	N/C	N/C
14	GND	GND	EXT CLK I/O – TTL I/O	GND	GND	GND
15	A429 RX5-	A429 RX5+	~EXT RT ADD ENABLE	A429 RX4+/TX4+	A429 RX4-/TX4-	GND
16	GND	GND	IRIG_IN	GND	GND	IRIG_GND
17	A429 RX6+	A429 RX6-	SDISCR2 / RTADDR_2	A429 RX7-	A429 RX7+	SDISCR1 / RTADDR_1
18	GND	GND	SDISCR4 / RTADDR_4	GND	GND	SDISCR3 / RTADDR_3
19	DDISC1+ (RS-485)	DDISC1- (RS-485)	SDISCR6 / RTADDR_P	A429 RX8+	A429 RX8-	SDISCR5 / RTADDR_5

Arinc-717 Operation

TX Operation

When a channel is set to transmit in Harvard Bi-Phase mode, this forces a TX channel pair (channels 1&2 and 3&4 pairs) to differentially drive the 0-5V positive leg of the ARINC-429 drivers. The odd channel is the positive differential signal and the even channel leg is the negative differential signal used to create Harvard Bi-Phase 717 encoding. This setting is provided for older ARINC-717 DFDRS systems. This setting ONLY applies to the first four TX channels.

Table 10. TX Connections for ARINC-717 operation (Front IO)

J1Pin#	Signal	J1 Pin#	Signal
19	A717 TX1+	53	N/C
20	A717 TX1-	54	N/C
21	A717 TX2+	55	N/C
22	A717 TX2-	56	N/C

Table 11. TX Connections for ARINC-717 operation (P4 IO)

P4 Pin#	Signal	P4 Pin#	Signal
33	A717 TX1+	34	A717 TX1-
37	A717 TX2+	38	A717 TX2-

Table 12. TX Connections for ARINC-717 operation (P6 IO)

P6 Pin#	Signal	P6 Pin#	Signal
B11	A717 TX1+	D11	A717 TX1
B13	A717 TX2+	D15	A717 TX2-

RX Operation

When a channel is set to receive in Harvard Bi-Phase mode, the same connector inputs are used as when operating in standard ARINC-A429 mode. This ONLY applies to the first two RX channels. See the ARINC (RX & TX) Protocol Engine Specifications-User's Manual for more information on setting the channel to operate in Harvard bi-phase mode.

Table 13. RX Connections for ARINC-717 operation (Front IO)

J1 Pin#	Signal	J1 Pin#	Signal
19	A717 RX1+	53	A717 RX1-
20	A717 RX2+	54	A717 RX2-

Table 14. RX Connections for ARINC-717 operation (P4 IO)

J4 Pin#	Signal	J4 Pin#	Signal
33	A717 RX1+	35	A717 RX1-
34	A717 RX2+	36	A717 RX2-

Table 15. RX Connections for ARINC-717 operation (P6 IO)

J4 Pin#	Signal	J4 Pin#	Signal
33	A717 RX1+	34	A717 RX1-
35	A717 RX2+	36	A717 RX2-

Software Device vs. Physical Channel

The Alta XMC-MA4 can contain one or more ***devices.*** A **device** is 8 channels (RX/TX configuration will vary). Another term for device is **bank. Device = Bank** (This is group of ARINC 8 or less channels)**.** The following table serves as a cross reference between software designation of bank/channel and the cards physical channel.

Table 16. Software vs. Physical Channel

Software Device	Physical Channel
Bank 1, Channel 1	RX1/TX1
Bank 1, Channel 2	RX2/TX2
Bank 1, Channel 3	RX3/TX3
Bank 1, Channel 4	RX4/TX4
Bank 1, Channel 5	RX5
Bank 1, Channel 6	RX6
Bank 1, Channel 7	RX7
Bank 1, Channel 8	RX8

A429 Shared Channels

The XMC-MA4 provides some shared RX/TX channels which include a line-driver for transmit operation and a receiver connected to the same pins. Under normal powered operation for a shared channel, the transmit channel may either drive the bus or act as high impedance allowing for receive operation. When the XMC-MA4 does not have power applied during normal operation, the line-driver acts as a low impedance source on the bus which can cause the bus voltage to fall below the minimum of the ARINC 429 specification if an external device is transmitting on the bus. In this case, Alta recommends that RX only channels be used for the application instead of shared channels.

Non-Volatile Memory Write Prohibit

The XMC-MA4 provides a non-volatile memory write prohibit input on Pin C16 of the P5 Connector. When this signal is asserted high, the XMC-MA4 will disable writes to non-volatile memory on the board. The XMC-MA4 board will accept transitions on this signal at any time while valid power is applied to the board.

PCI Device Information

PCI Device ID: 0x021A
PCI Vendor ID: 0xAD00

The table below explains the memory regions that should be mapped by the host.

Table 17. Host Mapping

Base Address Reg	Type	Size (Bytes)	Description
BAR 0	Memory	512	Local Configuration Registers (Mapped)
BAR 1	N/A		Not Used
BAR 2	Memory	4 Meg	User Memory Space (Mapped)
BAR 3-5	N/A		Not Used

Host Memory Map

The figure below shows the basic memory map configuration for the XMC-MA4 interface with 512K Bytes of RAM per channel Special configurations may vary.

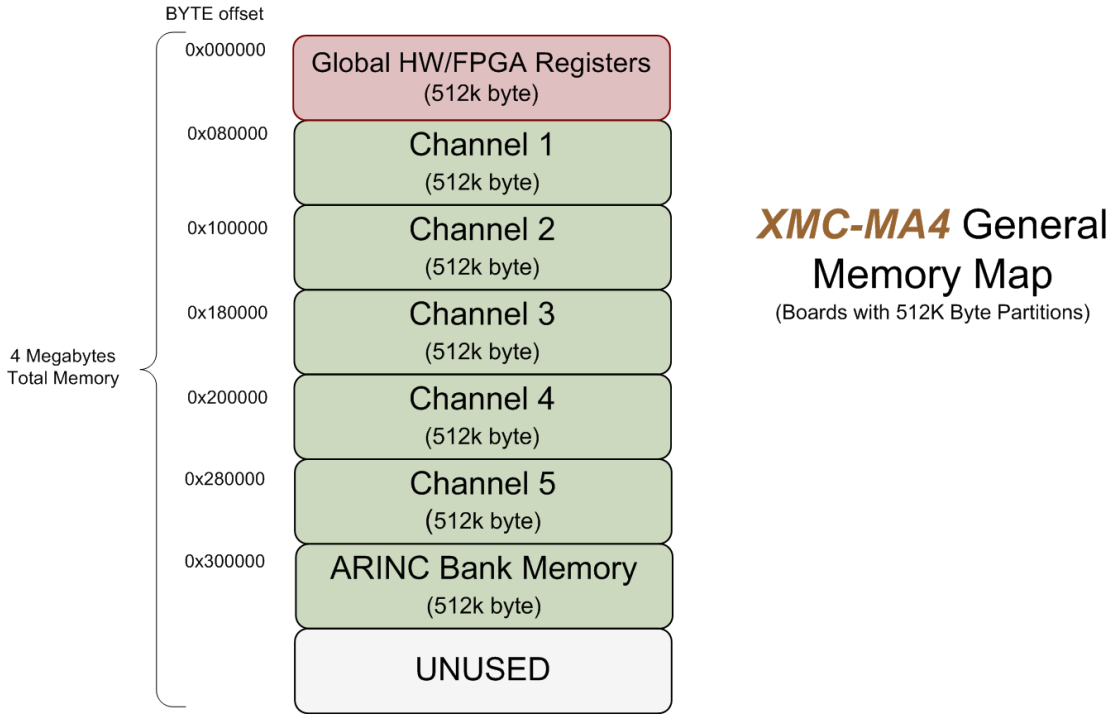

Figure 3. Basic Memory Map

XMC-MA4 Global Registers

The first Megabyte of the XMC-MA4 memory map contains backplane and global card level settings and status values that affect processing for all channels. Details on Global Registers may be found in the Alta Core-1553 Spec User's manual.

Revision Information

Date	Rev	Description
06/27/11	A0	Initial Release
05/02/12	A1	-Updated P4 Rear Panel Pin-Outs -Added P6 Panel Pin-Outs -Updated XMC photos to show P6 Connector
06/10/13	A2	Removed P4_ designation from some GND pins in P6 pin-out table
02/24/15	A3	Updated Appendix A - Added photos of cables and added option for thumb screw Added Software Device vs. Physical Channel table
10/12/15	A4	Updated cable assembly information
12/07/16	A5	Updated Table 9 to Match Table 8
01/31/17	A6	Updated cable information to include whether or not cables contain PVC
05/09/17	A7	Added A429 Shared Channels paragraph
07/20/18	A8	Added bullet about shared channels to specifications
10/01/19	A9	Updated NAICS number and % on table 3
11/19/19	A10	Corrected pin-out number 15 on table 9
03/01/21	A11	Corrected Table 8 (pin 61) and Table 9 (pin 19C)
01/17/23	A12	Updated Card Level specifications and contact info

Appendix A: SCSI Cable Information & Pin-Outs

(Front Panel Information Only. See Main Section of Manual for Applicable Rear Panel Information)

Description:

SCSI-3 to Ten 1553 Stub Connections (5 Channels) and Female DB50 Auxiliary Connector.

Alta Cable Assembly Part Numbers (Reorder Numbers)

SCSI-MA4-5-01-T (five channel**)
SCSI-MA4-4-01-T (four channel**)
SCSI-MA4-3-01-T (three channel**)
SCSI-MA4-2-01-T (two channel**)
SCSI-MA4-1-01-T (one channel**)

* Does not contain PVC
** Contains PVC

SCSI 3 Front Panel Connector Information:

- Clip Style
  - SCSI CON: AMP #1-5750913-7 (or equiv)
  - Backshell: Amp #5749195-2 (or equiv)
- Thumb Screw (-T)

CON and Backshell: Norcomp 989-068-130L121 (or equiv)

NOTE: Cables come standard with Thumb Screw option (-T). If Clip Style is needed remove the -T from Part Number when ordering.

SCSI-MA4-5-01
Cable Shown

Cables are EU and China RoHS Compliant.

RoHS 2002/95/EC

Cable Assembly Markings & Information:

- Shrink-wrap from SCSI to 1553/Aux Cable
  - 1” from SCSI Base add label
    - P1 - Part No: SCSI-MA4-X-01-T (X=Channel Count) (T=Thumb Screw)
- 1553 Cable Labeling
  - 1” from base of connector add Shrink Wrap Color Code
    - CH1 A – Shrink Tube Color Code: Red
    - CH1 B –Shrink Tube Color Code: Red-Black Stripe (Red closest to 1553 connector).
    - CH2 A – Shrink Tube Color Code: Green
    - CH2 B –Shrink Tube Color Code: Green-Black Stripe (Green closest to 1553 connector).
    - CH3 A – Shrink Tube Color Code: Blue
    - CH3 B –Shrink Tube Color Code: Blue-Black Stripe (Blue closest to 1553 connector).
    - CH4 A – Shrink Tube Color Code: Yellow
    - CH4 B –Shrink Tube Color Code: Yellow-Black Stripe (Yellow closest to 1553 connector).
    - CH5 A – Shrink Tube Color Code: White
    - CH5 B –Shrink Tube Color Code: White-Black Stripe (White closest to 1553 connector).
  - 2” from base of connector add labels
    - J1 1553 CH1 A
    - J2 1553 CH1 B
    - J3 1553 CH2 A
    - J4 1553 CH2 B
    - J5 1553 CH3 A
    - J6 1553 CH3 B
    - J7 1553 CH4 A
    - J8 1553 CH4 B
    - J9 1553 CH5 A
    - J10 1553 CH5 B
- DB50 AUX Connector Labeling
  - 1” from base of connector add label
    - J11 AUX I/O
- 24” length on 1553 cables (tip to tip – including connectors).
- 18” length on DB50 AUX Cable (tip to tip – including connectors).
- 1553 thin Cable with 1553 3-Lug Female Connector
- Assembly Standard: IPC-610 Class 3
- Assemble with Lead free components and Lead free solder.
- Alta Requires a Certificate of Conformance with delivery

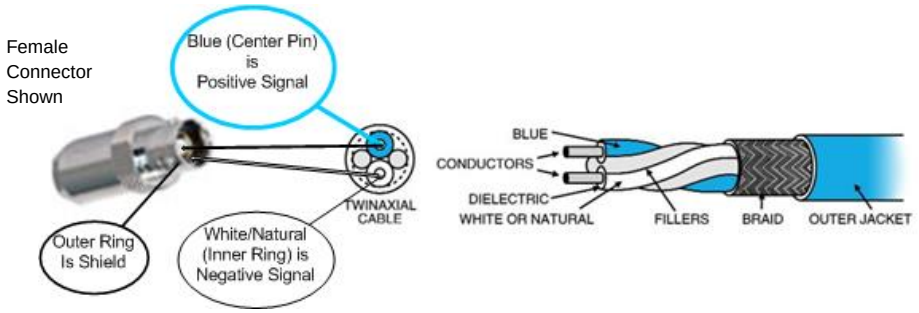

Table 18. SCSI Connector Pin-Outs

SCSI Pin#	Signal	SCSI Pin#	Signal
1	1553 CH 1A+	35	1553 CH 1A-
2	1553 CH 1B+	36	1553 CH 1B-
3	1553 SHIELD	37	GND
4	TRIG IN 1	38	TRIG OUT 1
5	1553 CH 2A+	39	1553 CH 2A-
6	1553 CH 2B+	40	1553 CH 2B-
7	TRIG IN 2	41	TRIG OUT 2
8	1553 CH 3A+	42	1553 CH 3A-
9	1553 CH 3B+	43	1553 CH 3B-
10	1553 SHIELD	44	GND
11	TRIG IN 3	45	TRIG OUT 3
12	1553 CH 4A+	46	1553 CH 4A-
13	1553 CH 4B+	47	1553 CH 4B-
14	TRIG IN 4	48	TRIG OUT 4
15	1553 CH 5A+	49	1553 CH 5A-
16	1553 CH 5B+	50	1553 CH 5B-
17	TRIG IN 5	51	TRIG OUT 5
18	1553 SHIELD	52	GND
19	RX1+/TX1+	53	RX1-/TX1-
20	RX2+/TX2+	54	RX2-/TX2-
21	RX3+/TX3+	55	RX3-/TX3-
22	RX4+/TX4+	56	RX4-/TX4-
23	RX5+	57	RX5-
24	RX6+	58	RX6-
25	RX7+	59	RX7-
26	RX8+	60	RX8-
27	TRIG IN 6	61	TRIG OUT 6
28	SDISC1 / RTADDR_1	62	DDISC1+ (RS-485)
29	SDISC2 / RTADDR_2	63	DDISC1- (RS-485)
30	SDISC3 / RTADDR_3	64	GND
31	SDISC4 / RTADDR_4	65	EXT CLK I/O – TTL I/O
32	SDISC5 / RTADDR_5	66	~EXT RT ADD ENABLE
33	SDISC6 / RTADDR_P	67	GND
34	IRIG IN	68	IRIG GND

Table 19. DB50 Connector Pin-Outs

DB50 Pin#	Signal	DB50 Pin#	Signal
1	RX1+/TX1+	26	RX1-/TX1-
2	RX2+/TX2+	27	RX2-/TX2-
3	RX3+/TX3+	28	RX3-/TX3-
4	RX4+/TX4+	29	RX4-/TX4-
5	RX5+	30	RX5-
6	RX6+	31	RX6-
7	RX7+	32	RX7-
8	RX8+	33	RX8-
9	N/C	34	GND
10	TRIG IN 1	35	TRIG Out 1
11	TRIG IN 2	36	TRIG Out 2
12	TRIG IN 3	37	TRIG Out 3
13	TRIG IN 4	38	TRIG Out 4
14	TRIG IN 5	39	TRIG Out 5
15	TRIG IN 6	40	TRIG Out 6
16	GND	41	GND
17	SDISC1 / RTADDR_1	42	DDISC1+ (RS-485)
18	SDISC2 / RTADDR_2	43	DDISC1- (RS-485)
19	SDISC3 / RTADDR_3	44	N/C
20	SDISC4 / RTADDR_4	45	EXT CLK I/O – TTL I/O
21	SDISC5 / RTADDR_5	46	~EXT RT ADD ENABLE
22	SDISC6 / RTADDR_P	47	GND
23	GND	48	N/C
24	IRIG IN	49	IRIGB IN GND
25	N/C	50	GND/SHIELD - Connected to metal DB hood (or to DB Connector if Plastic Hood)

Table 20. SCSI-DB Cross Reference

SCSI Pin	DB Pin	Signal	SCSI Pin#	DB Pin	Signal
1	NA	1553 CH 1A+	35	NA	1553 CH 1A-
2	NA	1553 CH 1B+	36	NA	1553 CH 1B-
3	NA	1553 SHIELD	37	16	GND
4	10	TRIG IN 1	38	35	TRIG OUT 1
5	NA	1553 CH 2A+	39	NA	1553 CH 2A-
6	NA	1553 CH 2B+	40	NA	1553 CH 2B-
7	11	TRIG IN 2	41	36	TRIG OUT 2
8	NA	1553 CH 3A+	42	NA	1553 CH 3A-
9	NA	1553 CH 3B+	43	NA	1553 CH 3B-
10	NA	1553 SHIELD	44	23	GND
11	12	TRIG IN 3	45	37	TRIG OUT 3
12	NA	1553 CH 4A+	46	NA	1553 CH 4A-
13	NA	1553 CH 4B+	47	NA	1553 CH 4B-
14	13	TRIG IN 4	48	38	TRIG OUT 4
15	NA	1553 CH 5A+	49	NA	1553 CH 5A-
16	NA	1553 CH 5B+	50	NA	1553 CH 5B-
17	14	TRIG IN 5	51	39	TRIG OUT 5
18	NA	1553 SHIELD	52	34	GND
19	1	RX1+/TX1+	53	26	RX1-/TX1-
20	2	RX2+/TX2+	54	27	RX2-/TX2-
21	3	RX3+/TX3+	55	28	RX3-/TX3-
22	4	RX4+/TX4+	56	29	RX4-/TX4-
23	5	RX5+	57	30	RX5-
24	6	RX6+	58	31	RX6-
25	7	RX7+	59	32	RX7-
26	8	RX8+	60	33	RX8-
27	15	TRIG IN 6	61	40	TRIG OUT 6
28	17	SDISC1 / RTADDR_1	62	42	DDISC1+ (RS-485)
29	18	SDISC2 / RTADDR_2	63	43	DDISC1- (RS-485)
30	19	SDISC3 / RTADDR_3	64	41	GND
31	20	SDISC4 / RTADDR_4	65	45	EXT CLK I/O – TTL I/O
32	21	SDISC5 / RTADDR_5	66	46	~EXT RT ADD ENABLE
33	22	SDISC6 / RTADDR_P	67	47	GND
34	24	IRIG IN	68	49	IRIG GND