NOT MEASUREMENT
SENSITIVE

MIL-HDBK-1553A
1 November 1988

SUPERSEDING
MIL-HDBK-1553
9 November 1984

MILITARY HANDBOOK

MULTIPLEX APPLICATIONS

HANDBOOK

AMSC: N/A

FSC: MCCR

NOTICE OF CHANGE

INCH-POUND

MIL-HDBK-1553A
NOTICE 2
23 March 1995

MILITARY HANDBOOK

MULTIPLEX APPLICATIONS HANDBOOK

TO ALL HOLDERS OF MIL-HDBK-1553A:

1. The following changes should be made to MIL-HDBK-1553A:

Pages i and ii

Delete Distribution Statement D and Export Control Warning Notice. Insert "Distribution Statement A. Approved for public release; distribution is unlimited."

2. RETAIN THIS NOTICE AND INSERT BEFORE TABLE OF CONTENTS.

3. Holders of MIL-HDBK-1553A will verify that changes indicated above have been entered. This notice page will be retained as a check sheet. This issuance is a separate publication. Each notice is to be retained by stocking points until the military handbook is completely revised or canceled.

Custodians:
Army – ER
Navy – AS
Air Force – 11

Preparing Activity:
Air Force – 11
(Project MCCR-0104)

AMSC: N/A

AREA: MCCR

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

W A R N I N G

INFORMATION SUBJECT TO EXPORT CONTROL LAWS

This document contains information subject to the International Traffic in Arms Regulation (ITAR) and/or the Export Administration Regulation (EAR) of 1979 which may not be exported, released, or disclosed to foreign nationals inside or outside the United States without first obtaining an export license. A violation of the ITAR or EAR may be subject to a penalty of up to 10 years imprisonment and a fine of $100,000 under 22 U.S.C. 2778 or section 2410 of the Export Administration Act of 1979. Include this notice with any reproduced portion of this document.

DESTRUCTION NOTICE - MIL-HDBK-1553A is an unclassified, limited document. Destroy unclassified, limited documents by any method that will prevent disclosure or reconstruction of the document.

DEPARTMENT OF DEFENSE

WASHINGTON DC

MIL-HDBK-1553A
Multiplex Applications Handbook
1 November 1988

1. This standardization handbook was developed by the Department of Defense in accordance with established procedures.

2. This handbook was approved on 1 November 1988 for printing and inclusion in the military standardization handbook series.

3. This document provides rationale and guidance on the use of requirements contained in MIL-STD-1553B, Aircraft Internal Time Division Command/Response Multiplex Data Bus. The complete handbook is not intended to be referenced in purchase specifications except for informational purposes, nor shall it supersede any specification requirements. However, specific sections or paragraphs in this handbook may be contractually called out in an equipment specification.

4. Every effort has been made to reflect the latest information on multiplex data bus applications. We intend to review this document periodically to insure it is complete and current. Users of this document are encouraged to report any errors discovered and any recommendations for changes or improvements to ASD/ENES, Wright-Patterson AFB OH 45433-6503.

5. Subject term listing:

Avionics integration
Bus, data
Data bus
Multiplex data bus

6. Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: ASD/ENES, Wright-Patterson AFB OH 45433-6503, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

Custodians:
Army - AV
Navy - AS
Air Force - 11

Preparing activity:
Air Force - 11

(Project MCCR-0029)

FOREWORD

1. This handbook is written to be used, in conjunction with MIL-STD-1553, by the project engineer who is specifying a new system or subsystem design for a Government procuring activity.

2. The primary purpose of this handbook is to give rationale and guidance to the contractual requirements in MIL-STD-1553B.

3. Further information on the background and purpose for this document can be found in Sections 10 and 20.

4. The office responsible for development and technical maintenance of this handbook is ASD/ENAS, Wright-Patterson AFB OH 45433-6503.

CONTENTS

FIGURES

TABLES

SECTION 10

INTRODUCTION

CONTENTS

TABLES

10. INTRODUCTION

New MIL-STD-1553 system designs and advances in microelectronics since the first MIL-HDBK-1553 was published were the motivation for this revision. It describes new MIL-STD-1553 state-of-the-art multiplexing, it retains the valuable fundamentals of the original handbook, and it contains help for—

a. Government engineers who write requirements for equipment with MIL-STD-1553 interfaces or specify systems that conform to MIL-STD-1553.

b. "Black box" designers who design equipment that interfaces with the MIL-STD-1553 multiplex bus.

c. System designers and integrators who design systems incorporating multiple units that communicate via a MIL-STD-1553 multiplex bus.

The published versions of MIL-STD-1553 documents and notices are not reproduced here. Readers must obtain copies of each and place them in their notebooks so that the context of the many references to the standard will be clear. Copies of MIL-STD-1553 and the latest notices in effect, as well as copies of this handbook (MIL-HDBK-1553), maybe obtained from the following address:

Commanding Officer
Naval Publications and Forms Center
5801 Tabor Avenue
Philadelphia, PA 19120
Telephone (215) 697-2179

In addition to the government documents, SAE publication AE-12, Systems Integration Handbook, addresses MIL-STD-1553 integration issues. This document maybe obtained from:

SAE
400 Commonwealth Drive
Warrendale, PA 15096-0001
Telephone (412) 776-4841

Scope. The primary orientation of this handbook (MIL-HDBK-1553) is to show how to apply MIL-STD-1553B (21 September 1978) as revised by changes of Notice 2 (8 September 1986). The differences between MIL-STD-1553B Notices 1 and 2 are explained where required.

Handbook organization. The contents of each of the 13 major sections into which this handbook is organized are as follows:

a. **Section 10-Introduction-A** short introduction and history of the development of MIL-STD-1553.

b. **Section 20-Commentary of MIL-STD-1553B and Notice 2—** Commentary and explanations of each paragraph of both MIL-STD-1553B and of its Notice 2.

c. **Section 30-Terminal/System Specification Considerations-** Aspects of terminals and systems for the Government engineer to consider when preparing specifications for procurement of units and systems that must meet MIL-STD-1553 requirements; includes an example specification.

d. **Section 40-Media** Design-Information that will be useful to the engineer responsible for designing bus wire, couplers, and transformers that meet MIL-STD-1553 requirements, including the media through which data are transmitted and their interconnecting electrical characteristics.

e. **Section 5-Terminal Design—** Information targeted for the "black box" hardware designer relating to the circuitry of the analog and digital portions of interface circuitry that must meet MIL-STD-1553 requirements.

f. **Section 60-System Design-** System methods targeted for the systems designer and integrator to use in meeting MIL-STD-1553 requirements.

g. **Section 70-Multiplex System Examples-** Examples of B-1B, CV-HELO, F-16C/D, AH-64, OV-1D and C-17A system designs, as well as the system topologies, design details, problems, and limitations of each; targeted at the systems designer.

h. **Section 80-Parameter Formats-** Guidelines for defining and using data words that meet MIL-STD-1553 requirements.

i. **Section 90-Comparison of MIL-STD-1553B Versions and Notices-** Compares the various versions and notices of MIL-STD-1553 to assist hardware or system design engineers who need to incorporate or interface with equipment built to a specific version or notice of MIL-STD-1553.

j. **Section 100-RT Validation Test Plan-** Remote terminal (RT) validation test plan, commonly required for development of equipment that must meet MIL-STD-1553 requirements.

k. **Section 110-Other test plans-** The Society of Automotive Engineers (SAE) AS-1 Committee has assembled several test plans that are listed in this section.

l. **Section 120-Definitions-** A list of definitions of terms used in the handbook.

m. **Section 130-index-** The index for the handbook.

MIL-STD-1553 background. The U.S. Department of Defense (DOD) sets standards to be used and applied by the military services and their contractors. A military standard is a document that establishes engineering and technical requirements for processes, procedures, practices, and methods that have been adopted as standard. One of these, MIL-STD-1553, "Digital Time Division Command/Response Multiplex Data Bus," has been in use since 1973 and is widely applied in military systems.

Because of its flexibility, MIL-STD-1553 has been used for many different design styles and implementations, sometimes causing difficulties in compatibility, modification, or growth. This release of MIL-HDBK-1553 discusses designs and implementations that have proven themselves and are usable in a variety of applications. This handbook should aid future designs by improving functionality and flexibility and decreasing cost.

MIL-STD-1553 chronology. Development of a standard digital time-division multiplex data bus began in early 1968 and has continued through the present with the latest revision (MIL-STD-1553B, Notice 2). The Society of Automotive Engineers (SAE), Aerospace Branch, established a subcommittee of industry and military personnel in 1968 to define some of the basic requirements of a serial data bus. This committee maintained a continuing exchange of industry and military views on the subject of serial data buses. The Multiplexing for Aircraft Committee (SAE-A2K) developed the first draft of a data bus standard. That draft represented a mixture of military standard requirements and procurement specification requirements. Its format allowed standardization on requirements that could be agreed upon and a slash sheet in the appendix for requirements that appeared to be vehicle particular. This document represented the best that the industry and the military could define at the time.

The benefit of this document was that it produced a sounding board for ideas. In this respect, it was successful and provided that step forward required to develop-

a. Air Force standard, MIL-STD-1553, "Aircraft Internal Time Division Command/Response Multiplex Data Bus," August 1973.

b. Navy specification, MIL-P81883, "Control Group, Electric Power, OK-XXX-(V)/A, General Specification for," May 1976.

During the years from inception of the SAE-A2K Committee to release of its first military documents, the industry was designing and producing hardware for various multiplex systems. Some of these systems were developed in the era prior to, or during development of, standardization (e.g., the F-15 and B-1A). The F-16 was the first to use the new Air Force MIL-STD-1553.

From 1973 to 1975 (when MIL-STD-1553A was released), both industry and the military (Air Force, Army, and Navy) coordinated their efforts to determine the degree of standardization required. During this time, several preliminary drafts of the Air Force and Navy documents were developed and industry comments were solicited extensively.

By late 1974, the DOD had directed the services to develop a coordinated position and to make the necessary revisions to MIL-STD-1553. Based on this effort, MIL-STD-1553A was released in April 1975. Since then, industry and the military have continued to coordinate the standard through symposia, studies, and military development programs. With the standard available, the industry and the military began to apply the data bus to more operational vehicles and systems. However, as uses multiplied, it became apparent that there were certain difficulties being encountered in application of MIL-STD-1553A.

Discussions concerning these difficulties were conducted between the SAE-A2K Committee and the DOD Triservices Committee (the group responsible for controlling the military standard). These discussions resulted in formation of an SAE task group (MIL-STD-1553 Update) in October 1976. The task group assignment was to develop suggested changes to MIL-STD-1553A. Once again, comments were solicited from industry and the military. These responses were extensive and involved foreign as well as domestic equipment suppliers and users of the standard. From this base, the task group developed and presented the proposed MIL-STD-1553B.

In October 1977, after reviewing and discussing suggested changes, the SAE-A2K Committee approved the proposed revisions. These revisions were then provided to the DOD Triservices Committee in December 1977. In January 1978, the DOD Triservices Committee solicited industry commentson changes to MIL-STD-1553A. Then, based on the recommended revisions and comments, the DOD Triservices Committee met on several occasions and produced a draft of MIL-STD-15536.

The draft of MIL-STD-15536 was presented to the SAE task group in April 1978 for review and comment. Following this review, one final meeting was held with task group members, in June 1978, during which a verbal agreement was reached between the SAE task group and the Triservices Committee. From this verbal agreement, final written approval was sought from the Triservices Committee. Upon receipt of the written approvals, MIL-STD-1553B was released as an official document on 21 September 1978.

Historically, Notice 1 to MIL-STD-1553B (released 12 February 1980) is best viewed as an interim effort to restrict the options in MIL-STD-1553B to a subset. On the other hand, Notice 2 (released 8 September 1986) is best viewed as a compromise among the DOD services, industry, and foreign nations that have a strong commitment to use MIL-STD-1553. It is written so that it supersedes Notice 1 but continues the same philosophy of restriction of options. However, Notice 2 adds requirements or clarifies ambiguous requirements based on industry and DOD experience. More than 2 years of discussion preceded the release of Notice 2.

MIL-STD-1553B is a standard and, except for electrical characteristic requirements, does not dictate implementation. However, there are interoperability problems that were not solved by either Notice 2 of the standard or the original version of MIL-HDBK-1553. In 1986, the Air Force instituted a validation testing

procedure that would verify whether or not a design complied with MIL-STD-1553 requirements. This Air Force initiative, developed by the SAE, resulted in the RT validation test plan. In all new systems, compliance with the test plan (section 100 of this release of MIL-HDBK-1553) will likely be required. As of 1988, a BC Validation Test Plan, a BC Production Test Plan and a System Test Plan have been developed. Additional test plans are being developed, coordinated, and published by the SAE.

Handbook updates. The original release of MIL-HDBK-1553 was on 9 November 1984. Notice 1 to MIL-HDBK-1553 added appendix A, "RT Validation Test Plan," on 26 September 1986 (the rest of the handbook was not changed at that time).

This release of MIL-HDBK-1553 reorganizes the information and updates desiqn sections of the handbook. Modifications are listed in table 10-1.

Table 10-1. MIL-HDBK-1553 Update Modifications

New section	Original section	Change/status
10 Introduction	Sections 10/20	Revised
20 Commentary on MIL-STD-1553B, and Notice 2	Section 70	Revised
30 Terminal and System Specification Considerations	None	New section
40 Media Design	None	New section
50 Terminal Design	Section 40	Revised
60 System Design	Sections 30/50	Revised
70 Multiplex System Examples	Section 60	Updated
80 Parameter Formats	Section 80	Updated
90 Comparison of MIL-STD-1553 Versions and Notices	Section 70	Updated
100 RT Validation Test Plan	Appendix A Notice 1	Updated
110 Other Test Plans	None	New section
120 Definitions	None	New section
130 Index	None	New section

SECTION 10 INDEX

SECTION 20

COMMENTARY OF MIL-STD-1553, NOTICE 2

CONTENTS

FIGURES

20. COMMENTARY ON MIL-STD-1553B AND NOTICE 2

20.1 Commentary on MIL-STD-1553B.

Section 20.1 contains commentaries on paragraphs of MIL-STD-1553B (referred to in the commentary as 1553B). The standard is reprinted in bold type and indented, followed by comments on the paragraphs that experience has shown require some clarification. (The comments are in normal type and full column width.) Applicable figures from MIL-STD-1553B are reproduced for the reader's convenience and are labeled "Figure _ of 1553 B."

Because Notice 2 to MIL-STD-1553B completely replaces Notice 1, there is no commentary on Notice 1. (A comparison of 1553 versions is provided in Section 90.) Notice 2 commentary follows the 1553B commentary (see 20.2). Whenever a 1553B paragraph was modified, supplemented, or restricted by Notice 2, the last sentence of the commentary on the affected paragraph contains a reference to the Notice 2 change.

AIRCRAFT INTERNAL TIME DIVISION
COMMAND/RESPONSE MULTIPLEX DATA BUS
FOREWORD

This standard contains requirements for aircraft internal time division command/response multiplex data bus techniques which will be utilized in systems integration of aircraft subsystems. Even with the use of this standard, subtle differences will exist between multiplex data buses used on different aircraft due to particular aircraft mission requirements and the designer options allowed in this standard. The system designer must recognize this fact, and design the multiplex bus controller hardware and software to accommodate such differences. These designer selected options must exist so as to allow the necessary flexibility in the design of specific multiplex systems in order to provide for the control mechanism, architecture redundancy, degradation concept and traffic patterns peculiar to the specific aircraft mission requirements.

1. SCOPE

1.1 Scope. This standard establishes requirements for digital, command/response, time division multiplexing (Data bus) techniques on aircraft. It encompasses the data bus line and its interface electronics illustrated on figure 1, and also defines the concept of operation and information flow on the multiplex data bus and the electrical and functional formats to be employed.

1.2 Application. When invoked in a specification or statement of work, these requirements shall apply to the multiplex data bus and associated equipment which is developed either alone or as a portion of an aircraft weapon system or subsystem development. The contractor is responsible for invoking all the applicable requirements of this Military Standard on any and all subcontractors he may employ.

A primary goal of the standard is to provide flexibility without creating new hardware and software designs for each new user. This is accomplished by specifying "use of" rather than "required to use" in the functional areas and by specifying the electrical interfaces explicitly so that designs by different manufacturers are electrically interchangeable and functionally compatible.

2. REFERENCED DOCUMENTS

2.1 Issue of document. The following document, of the issue in effect on date of invitation for bid or request for proposal, forms a part of the standard to the extent specified herein.

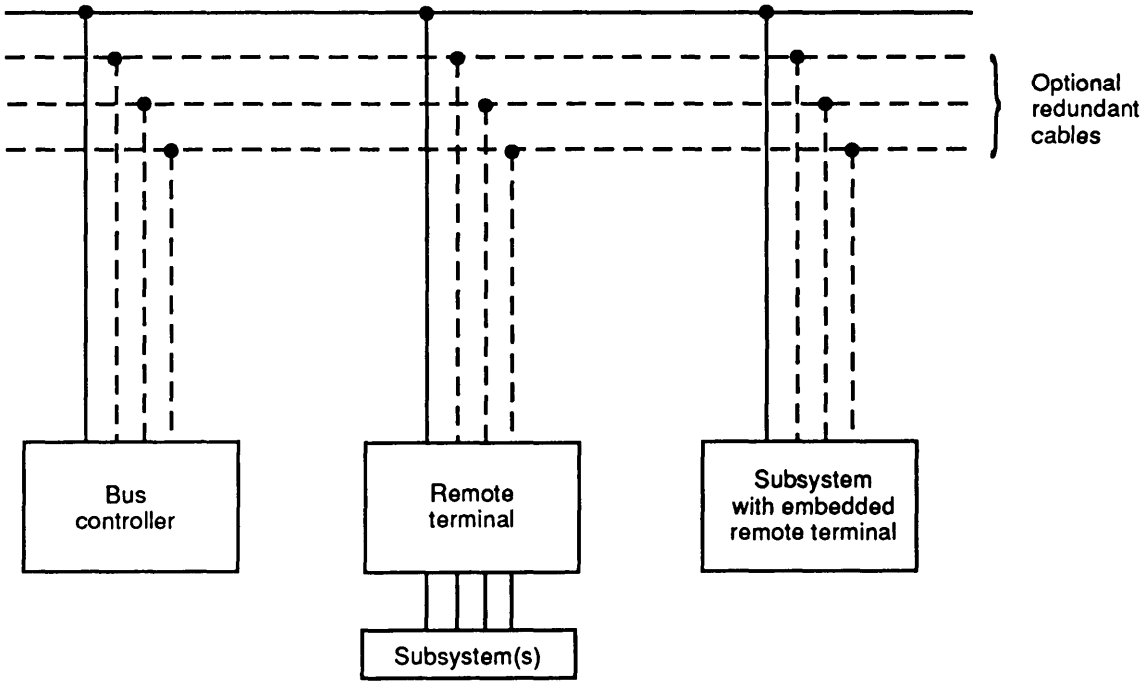


Figure 1 of 1553B. Sample Multiplex Data Bus Architecture

SPECIFICATION

MILITARY

MIL-E-8051 Electromagnetic Compatibility Requirements, Systems

(Copies of specifications, standards, drawings, and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

3. DEFINITIONS

3.1 Bit. Contraction of binary digit: maybe either zero or one. In information theory a binary digit is equal to one binary decision or the designation of one or two possible values or states of anything used to store or convey information.

3.2 Bit rate. The number of bits transmitted per second.

3.3 Pulse code modulation (PCM). The form of modulation in which the modulation signal is sampled, quantized, and coded so that each element of information consists of different types or numbers of pulses and spaces.

3.4 Time division multiplexing (TDM). The transmission of information from several signal sources through one communication system with different signal samples staggered in time to forma composite pulse train.

3.5 Half duplex. Operation of a data transfer system in either direction over a single line, but not in both directions on that line simultaneously.

3.6 Word. In this document a word is a sequence of 16 bits plus sync and parity. There are three types of words: command, status and data.

3.7 Message. A single message is the transmission of a command word, status word, and data words if they are specified. For the case of a remote terminal to remote terminal (RT to RT) transmission, the message shall include the two command words, the two status words, and data words.

3.8 Subsystem. The device or functional unit receiving data transfer service from the data bus.

3.9 Data bus. Whenever a data bus or bus is referred to in this document it shall imply all the hardware including twisted shielded pair cables, isolation resistors, transformers, etc., required to provide a single data path between the bus controller and all the associated remote terminals.

3.10 Terminal. The electronic module necessary to interface the data bus with the subsystem and the subsystem with the data bus. Terminals may exist as separate line replaceable units (LRUs) or be contained within the elements of the subsystem.

This definition of terminal is intentionally broad. Terminals in 1553B have common operational characteristics, as well as assigned roles in data bus operation. The three allowable roles are defined in 3.11, 3.12, and 3.13. Common operational requirements of terminals aredescribed in 4.4.1 of 1553B. Note that the definition gives designers complete freedom of functional partitioning of the operating parts of a terminal and that there is also no restriction of physical partitioning.

3.11 Bus controller. The terminal assigned the task of initiating information transfers on the data bus.

3.12 Bus monitor. The terminal assigned the task of receiving bus traffic and extracting selected information to be used at a later time.

The purpose of a bus monitor is to monitor the data bus and record specified bus activity. Two basic roles have been identified for the monitor in 4.4.4 of 1553B:

a. An off-line application including flight test recording, maintenance recording, or mission analysis.

b. A unique data bus terminal that provides an internal backup bus controller (BBC) function with sufficient information to take over as the active BC in the event of a switchover or a failure of the active BC.

In each of these two roles, the bus monitor hardware may take the approach of having the performance capability of a terminal (unique address) or it may take the approach of attaching itself to the data bus without the knowledge of the other bus users (including the BC). In this second approach, no bus communication from or to the bus monitor by the BC is possible. The bus monitor acts as a passive listener to the specified traffic it is assigned to record. Obviously, the performance of a bus monitor requires the monitoring of the data bus for command words, status words, and data words. From this monitoring, the specific message collection process can occur during normal and abnormal (bus error and recovery) bus traffic. To aid in detecting these words (command and status), the optional instrumentation bit (bit 10 in the status word and the associated bit, bit 10 in the command word) maybe set to logic 0 and logic 1, respectively.

3.13 Remote terminal (RT). All terminals not operating as the bus controller or as a bus monitor.

3.14 Asynchronous operation. For the purpose of this standard, asynchronous operation is the use of an independent clock source in each terminal for message transmission. Decoding is achieved in receiving terminals using clock information derived from the message.

This definition refers to the electrical characteristic by which the timing of message bits in a word are decoded. This use of asynchronous operation should not be confused with an asynchronous message that may interrupt or suspend the transmission of synchronous (i.e., periodic) messages in an avionics system.

3.15 Dynamic bus control. The operation of a data bus system in which designated terminals are offered control of the data bus.

3.16 Command/Response. Operation of a data bus system such that remote terminals receive and transmit data only when commanded to do so by the bus controller.

3.17 Redundant data bus. The use of more than one data bus to provide more than one data path between the subsystem, i.e., dual redundant data bus, tri-redundant data bus, etc.

The redundant data bus definition identifies a particular approach for obtaining multiple data paths to improve message arrival probability. The use of a dual standby-redundant data bus is discussed in 4.6. Dual standby-redundant is normaily defined as two 1553B buses (two twisted, shielded pair cables), each capable of communicating among the BCs and RTs. in this mode, only one bus is active at any given time, except when superseding commands are sent on the standby bus. Under this condition, the terminal responds to the most recent command.

3.18 Broadcast. Operation of a data bus system such that information transmitted by the bus controller or a remote terminal is addressed to more than one of the remote terminals connected to the data bus.

The broadcast protocol allows a BC or RT to address more than one terminal connected to the system. To do this, a dedicated terminal address (11111) is transmitted in the command word, and each RT withholds the normal status word response.

3.19 Mode code. A means by which the bus controller can communicate with the multiplex bus related hardware, In order to assist in the management of information flow.

The mode codes (4.3.3.5.1.7) are used to help manage the information transfer system. Standardizing the function and protocol of the mode codes eliminates the need for using user-defined commands to control the bus and simplifies the job of the BC in managing the bus.

4. GENERAL REQUIREMENTS

4.1 Test and operating requirements. All requirements as specified herein shall be valid over the environmental conditions which the multiplex data bus system shall be required to operate.

All 1553B requirements are in effect for the environmental range specified for the system. It is anticipated that for most military applications, this will be described by MIL-E-5400, Class II and some nuclear hardening specifications; however, because of the diversity of environmental conditions, the standard does not specify these requirements. The system designer must determine (from system specifications) the range of environmental conditions over which the 1553B system is required to operate.

4.2 Data bus operation. The multiplex data bus system in its most elemental configuration shall be as shown on figure 1. The multiplex data bus system shall function asynchronously in a command/response mode, and transmission shall occur in a half-duplex manner. Sole control of information transmission on the bus shall reside with the bus controller, which shall Initiate all transmissions. The information flow on the data bus shall be comprised of messages which are, in turn, formed by three types of words (command, data, and status) as defined in 4.3.3.5.

4.3 Charateristics.

4.3.1 Data form. Digital data may be transmitted in any desired form, provided that the chosen form shall be compatible with the message and word formats defined in this standard. Any unused bit positions in a word shall be transmitted as logic zeroes.

This freedom of form in formatting data word information gives the designer considerable independence in defining data word formats. Refer to section 80, for guidance in this area.

4.3.2 Bit priority. The most significant bit shall be transmitted first with the less significant bits following in descending order of value in the data word. The number of bits required to definea quantity shall be consistent with the resolution or accuracy required. In the event that multiple precision quantities (information accuracy or resolution requiring more than 16 bits) are transmitted, the most significant bits shall be transmitted first, followed by the word(s) containing the lesser significant bits in numerical descending order. Bit packing of multiple quantities in a single data word is permitted.

Bit packing is used to improve transmission efficiency when subsystem data contain less than 16 bits of information per parameter (e.g., each datum may be a single bit, which is common for status information). MIL-STD-1553B allows the system to assemble several such data parameters into a single 1553B data word. Packing data into fewer words decreases the bus loading; however, it increases the amount of conversion done by the receiving subsystem.

4.3.3 Transmission method.

4.3.3.1 Modulation. The signal shall be transferred over the data bus in serial digital pulse code modulation form.

4.3.3.2 Data code. The data code shall be Manchester II hi-phase level. A logic one shall be transmitted as a bipolar coded signal 1/0 (i.e., a positive pulse followed by a negative pulse). A logic zero shall be a bipolar coded signal 0/1 (i.e., a negative pulse followed by a positive pulse). A transition through zero occurs at the midpoint of each bit time (see figure 2).

4.3.3.3 Transmission bit rate. The transmission bit rate on the bus shall be 1.0 megabit per second with a combined accuracy and long-term stability of ± 0.1 percent (i.e., t 1000 Hz)). The short-term stability (i.e., stability over 1.0 second interval) shall beat least 0.01 percent (i.e., ± 100 Hz).

4.3.3.4 Word size. The word size shall be 16 bits plus the sync waveform and the parity bit for a total of 20 bits times as shown on figure 3.

The 20-bit word size was selected because it represented the minimum number of bits in a word when 16 bits of data, a three-bit invalid Manchester sync pattern, and a single parity bit are used. The three-bit sync pattern is described in 4.3.3.5.1.1.

493.3.5 Word formats. The word formats shall be as shown on figure 3 for the command, data, and status words.

Three types of words are allowed: command, data, and status. Each is 20 bits long, including 16 bits of information, a three-bit sync pattern, and a one-bit parity. The command word contains the address of the terminal, a T/R bit set to indicate whether the terminal is to transmit or receive, the subaddress/mode field, and the word count/mode code. The subaddress is a pointer to the data in the terminal subsystem, and the word count indicates the number of words (up to 32). If the subaddress/mode field is all ones or zeros, this is a flag to indicate that the word count/mode code is a code. Therefore, a mode code maybe transmitted to

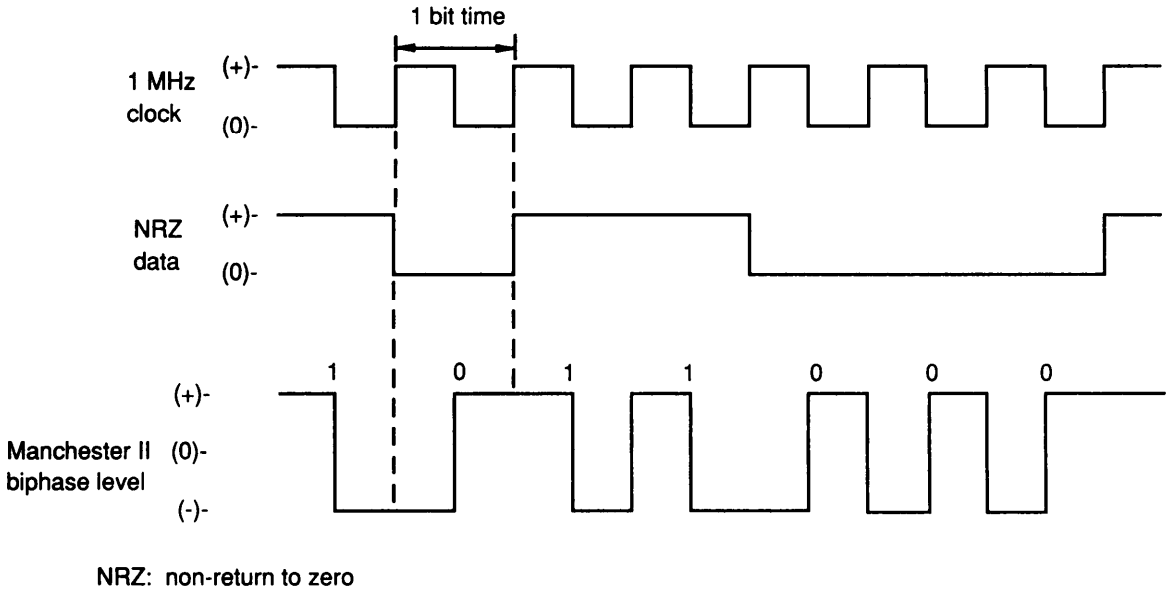


Figure 2 of 1553B. Data Encoding

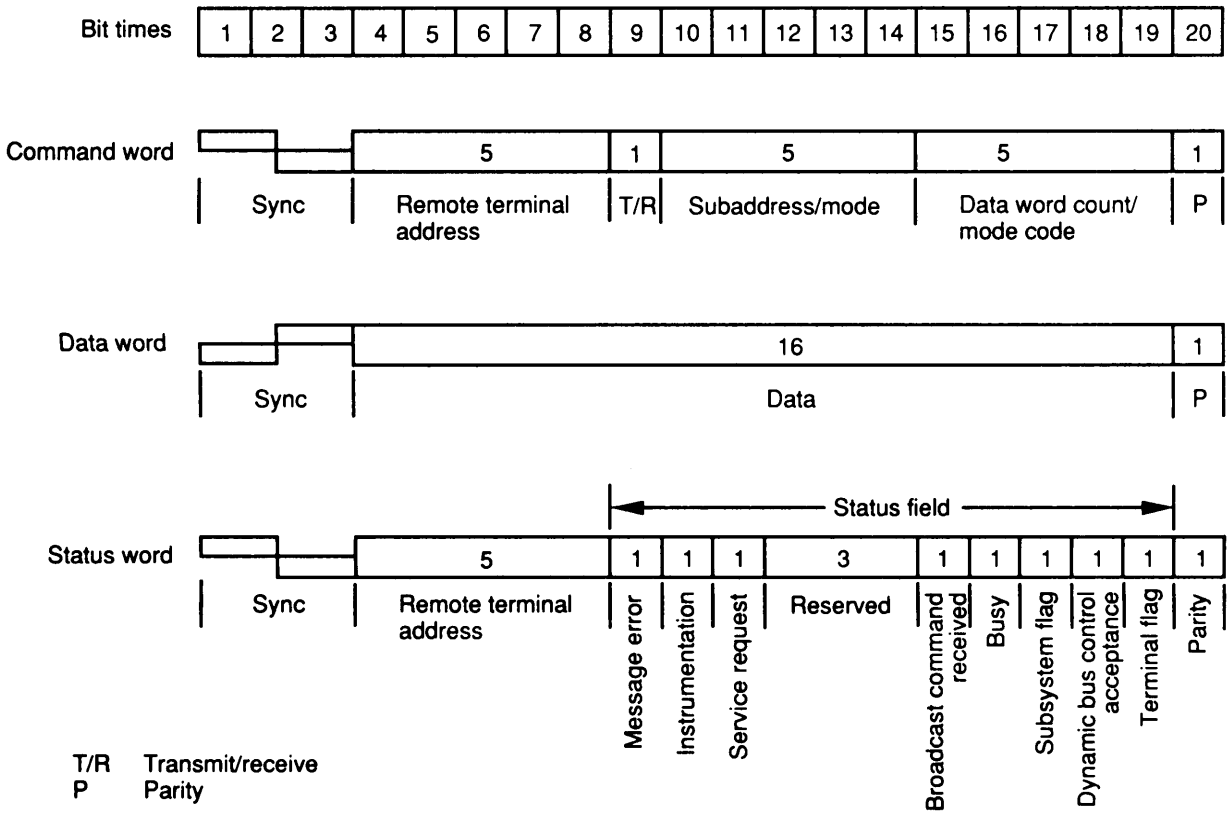


Figure 3 of 1553B. Word Formats

the terminal by the command word. The status word contains the terminal address and status bits. The command word format is discussed in 4.3.3.5.1, the data word format in 4.3.3.5.2, and the status word format in 4.3.3.5.3.

4.3.3.5.1 Command word. A command word shall be comprised of a sync waveform, remote terminal address field, transmit/receive (T/R) bit, subaddress/mode field, word count/mode code field, and a parity (P) bit (see figure 3).

The command word format is used to control and manage the information transfer system. Each portion of the command word is discussed in 4.3.3.5.1.1 through 4.3.3.5.1.7.17.

4.3.3.5.1.1 Sync. The command sync waveform shall bean invalid Manchester waveform as shown on figure 4. The width shall be three bit times, with the sync waveform being positive for the first one and one-half bit times, and then negative for the following one and one-half bit times. If the next bit following the sync waveform is a logic zero, then the last half of the sync waveform will have an apparent width of two clock periods due to the Manchester encoding.

4.3.3.5.1.2 Remote terminal address. The next five bits following the sync shall be the RT address. Each RT shall be assigned a unique address. Decimal address 31 (11111) shall not be assigned as a unique address. In addition to its unique address, a RT shall be assigned decimal address 31 (11111) as the common address, if the broadcast option is used.

Each RT will be assigned a unique address that it will respond to when that address is transmitted as part of a command word on the data bus by the active BC. Only one RT address cannot be assigned as a unique address—decimal address 31. This address has been assigned to all RTs as the common address for receiving broadcast data if the system uses the broadcast option.

The broadcast mode provides a mechanism for transmitting information to multiple RTs simultaneously with a single message. This is accomplished by reserving address 31 (11111) for broadcast messages. When a broadcast message is transmitted, the BC will use address 31 rather than a unique terminal address.

When an RT receives a broadcast message, the status word must not be transmitted in order to prevent simultaneous transmissions on the bus. With restrictions, broadcast messages can be used with subaddresses and mode codes.

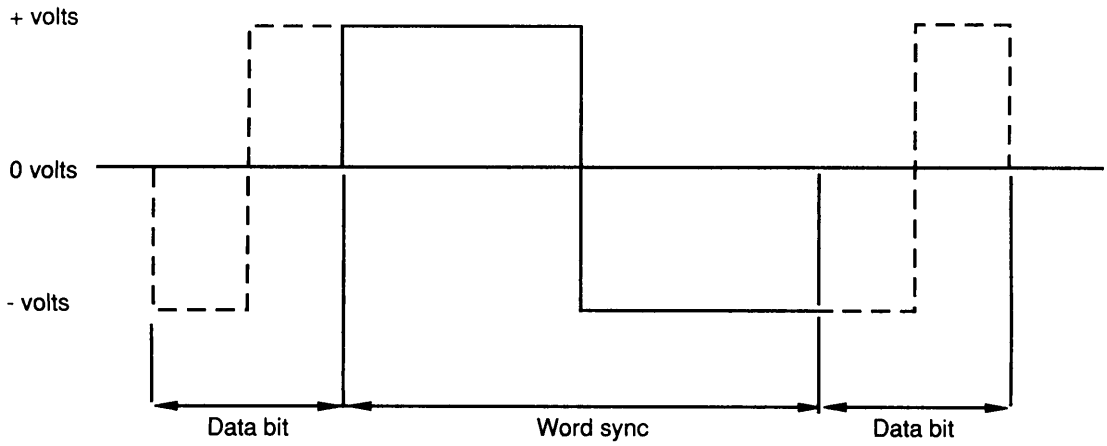


Figure 4 of 1553B. Command and Status Syn chronization

Indiscriminate use of the broadcast technique is not advisable. If used, it adds a failure mode to the system whenever a terminal in a failure mode uses address 31 for a message. Designers must question the benefit of discarding the command-response format, in which all message completion failures are known to the BC, to gain the benefits described below.

Proper use of the broadcast mode may yield several benefits:

a. Multiple terminals can be communicated with simultaneously, thereby permitting time synchronization of data or commands.

b. Bus duty cycle can be reduced by transmitting data required by multiple users simultaneously instead of sequentially. This also may reduce computer algorithm complexities because the broadcast mode would eliminate time skewing of the data among users.

c. Some error management can be enhanced by providing a single address by which all terminals can receive commands simultaneously. This would permit the BC to immediately command a state for the system rather than polling each unit individually with the same command in a serial fashion.

The broadcast message capability can reduce bus use considerably. This is particularly true for systems using multiple units for redundancy or systems dependent on parallel processing, thus requiring simultaneous data arrival at the processing units. As noted in 10.6 of the appendix, improper use of the broadcast format can result in undesirable system operation.

Since no status word response is allowed from the receiving terminal, discretion must be exercised when applying the capability. To provide message arrival verification, a bit in the status word is set when a valid broadcast message is received. This allows reporting of the reception if requested by the active BC using the transmit status word mode code.

In error situations, it may be advisable for the BC to request the last command word mode code to verify that the broadcast command was received. Asking for the last command word first preserves the last status word (i.e., the terminal does not reset or update status). In addition to data transfers, the ability to transmit a broadcast command message provides an effective method for managing the data bus system. This capability is performed using the broadcast address in combination with mode commands.

For dual standby-redundant systems, Notice 2 has additional requirements for RT addresses (see 30.3 and 30.6).

4.3.3.5.1.3 Transmit/receive. The next bit following the remote terminal address shall be the T/R bit, which shall indicate the action required of the RT. A logic zero shall indicate the RT is to receive, and a logic one shall indicate the RT is to transmit.

The transmit/receive (T/R) bit in the command word indicates the source of data flow in the information transfer system.

4.3.3.5.1.4 Subaddress/mode.The next five bits following the R/T bit shall be utilized to indicate an RT subaddress or use of mode control, as is dictated by the individual terminal requirements. The subaddress/mode values of 00000 and 11111 are reserved for special purposes, as specified in 4.3.3.5.1.7, and shall not be utilized for any other function.

The subaddress/mode field has two functions:

a. Identifies the subaddress of specific messages to or from an RT.

b. Indicates that a mode command for the information transfer system is being transmitted.

The use of either 00000 or 11111 in the subaddress/mode field will be decoded to indicate that a mode command is present in the next five-bit field. This limits the number of unique RT subaddresses to 30. If the instrumentation bit (see 4.3.3.5.3) is implemented, the RT will be limited to 15 unique subaddresses. The requirements for use of the instrumentation bit are in 4.3.3.5.3.4.

For dual standby-redundant systems, Notice 2 adds a recommendation for a data wraparound command for a transmit and receive subaddress (see 30.7). Notice 2 also states that an RT shall be capable of responding to both 00000 and11111 subaddress/mode codes and that the mode code indicators will not convey different information.

4.3.3.5.1.5 Data word count/mode code. The next five bits following the subaddress/mode field shall be the quantity of data words to be either sent out or received by the RT or the optional mode code as specified in 4.3.3.5.1.7. A maximum of 32 data words may be transmitted or received in any one message block. All 1's shall indicate a decimal count of 31, and all 0's shall indicate a decimal count of 32.

The dual function of this field provides for identifying message lengths for data messages or for mode codes. The five-bit field allows up to 32 data words to be transmitted in a message or 32 specific mode codes. A word count of one is represented logically as 00001. All zeros is defined as a word count of 32.

4.3.3.5.1.6 Parity. The last bit in the word shall be used for parity over the preceding 16 bits. Odd parity shall be utilized.

The use of a single parity bit per word was provided to identify bit errors occurring during the transmission and detection of a word. According to 10.4, "Theoretical and empirical evidence indicates that an undetected bit error rate of 10^{-12} can be expected from a practical multiplex system built to this standard." Also see 4.5.2.1.2.4 for the noise test.

4.3.3.5.1.7 Optional mode control. For RT's exercising this option a subaddress/mode code of 00000 or 11111 shall imply that the contents of the data word count/mode code field are to be decoded as a five bit mode command. The mode code shall only be used to communicate with the multiplex bus related hardware, and to assist in the management of information flow, and not to extract data from or feed data to a functional subsystem. Codes 00000 through 01111 shall only be used for mode codes which do not require transfer of a data word. For these codes, the T/R bit shall beset to 1. Codes 10000 through 11111 shall only be used for mode codes which require transfer of a single data word. For these mode codes, the T/R blt shall indicate the direction of data word flow as specified in 4.3.3.5.1.3. No multiple data word transfer shall be implemented with any mode code. The mode codes are reserved for the specific functions as specified in table I and shall not be used for any other purposes. If the designer chooses to implement any of these functions, the specific codes, T/R bit assignments, and use of a data word, shall be used as indicated. The use of the broadcast command option shall only be applied to particular mode codes as specified in table I.

The basic philosophy of the information transfer system is that it operates as a transparent communication link. "Transparent" means that an application's function does not need to be involved with the management of communication control. Obviously, the information transfer system requires management that introduces overhead into the transmission of data. The overhead consists of command words, status words, response times, and intermessage gaps. Within the command word, the mode codes provide data bus management capability. The mode codes have been divided into the two groups listed in table I of 1553B:

Transmit-receive bit	Mode code	Function	Associated data word	Broadcast command allowed
1	00000	Dynamic bus control	No	No
1	00001	Synchronize	No	Yes
1	00010	Transmit status word	No	No
1	00011	Initiate self-test	No	Yes
1	00100	Transmitter shutdown	No	Yes
1	00101	Override transmitter shutdown	No	Yes
1	00110	Inhibit terminal flag bit	No	Yes
1	00111	Override inhibit terminal flag bit	No	Yes
1	01000	Reset remote terminal	No	Yes
1	01001	Reserved	No	TBD
↓	↓	↓	↓	
1	01111	Reserved	No	TBD
1	10000	Transmit vector word	Yes	No
0	10001	Synchronize	Yes	Yes
1	10010	Transmit last command	Yes	No
1	10011	Transmit BIT word	Yes	No
0	10100	Selected transmitter shutdown	Yes	Yes
0	10101	Override selected transmitter shutdown	Yes	Yes
1 or 0	10110	Reserved	Yes	TBD
↓	↓	↓	↓	↓
1 or O	11111	Reserved	Yes	TBD

TBD: To be defined

Table I of 1553B. Assigned Mode Codes

a. Mode codes without a data word (00000-01111).

b. Mode codes with a data word (10000-11111).

The use of bit 15 in the command word (i.e., the MSB of the data word count/mode code field) to identify the two types was provided to aid in the decoding process. Also, the use of a single data word instead of multiple data words was adopted to simplify the mode circuitry. Generally, with these two types of mode commands, all management requirements of an information transfer system can be met.

Mode code messages are indicated when the subaddress/mode field in the command word is set to 00000 or 11111. (In either case, decimal subaddress 32 is defined to be equal to binary 00000 so that decimals 1 through 31 correspond to binary 00001 through 11111.) All control messages originate with the active BC and are received by a single receiver or by multiple receivers (broadcast). A terminal address value of 31 (11111) in the command word indicates a broadcast message, while any other terminal address identifies a unique message to a terminal on the bus. The mode command information is contained completely in the mode code/ word count field of the command word.

Table I of 1553B should be studied carefully to see the symmetry of the mode codes. The first 16 codes are not transmitted with a data word, the last 16 are. It is inappropriate to broadcast some of the mode codes

because of the possibility of bus crashes—simultaneous transmission by two or more terminals. (Requests for transmissions from RTs are examples.) Also, broadcast of dynamic bus control is inappropriate. The T/R bit is important for mode codes 17 to 31 because it defines whether the BC or the RT is to transmit the associated data word.

Assignment of mode codes is arbitrary with respect to early versions of 1553, which defined dynamic bus control and the separation of mode commands with and without data words. The purpose of reserved mode commands in each category (with and without data words) is important because it allows for controlled expansion of the standard. By controlling the mode command number and its definition, commonality among various terminals can be maintained. Each mode command is identified in table 1. All other mode codes are considered illegal commands. The message formats associated with mode commands are shown in figure 20-1.

Notice 2 specifies a minimum set of mode codes for implementation in RTs and requires BCs to have the capability to implement all of the mode codes (see 30.4.2).

4.3.3.5.1.7.1 Dynamic bus control. The controller shall issue a transmit command to an RT capable of performing the bus control function. This RT shall respond with a status word as specified in 4.3.3.5.3. Control of the data bus passes from the offering bus controller to the accepting RT upon completion of the transmission of the status word by the RT. If the RT rejects control of the data bus, the offering bus controller retains control of the data bus.

The dynamic bus control mode command (00000) is provided to allow the active BC a mechanism (using the information transfer system message formats) for offering a potential BC (operating as a RT) control of the data bus. Only the single-receiver command request (unique address) is allowed to be issued by the active BC. The response to this offering of bus control is provided by the receiving RT using the dynamic bus control acceptance bit in the status word (4.3.3.5.3). Rejection of this request by the RT requires the presently active BC to continue offering control to other potential controllers or remain in control. When a RT accepts control of the data bus system by setting the dynamic bus control acceptance bit in the status word, control is relinquished by the presently active BC, and the potential BC begins bus control.

Note that the foregoing sequence requires software (or firmware) implementation in all BCS. (Notice 2 prohibits the BC from ever issuing this mode command for Air Force applications.)

4.3.3.5.1.7.2 Synchronize (without data word). This command shall cause the RT to synchronize (e.g., to reset the internal timer, to start a sequence, etc.). The RT shall transmit the status word as specified in 4.3.3.5.3.

4.3.3.5.1.7.12 Synchronize (with data word). The RT shall receive a command word followed by a data word as specified in 4.3.3.5.2. The data word shall contain synchronization information for the RT. After receiving the command and data word, the RT shall transmit the status word as specified in 4.3.3.5.3.

The above two mode codes are used to inform the terminals of an event time to allow coordination among the active BC and receiving terminals. Synchronization information may be implicit in the command word (mode code 00001), or a data word (mode code 10001) may be used following the command word to provide the synchronization information. If a data word is used, bit definitions are the responsibility of the system designer.

4.3.3.5.1.7.3 Transmit status word. This command shall cause the RT to transmit the status word associated with the last valid command word preceding this command. This mode command shall not alter the state of the status word.

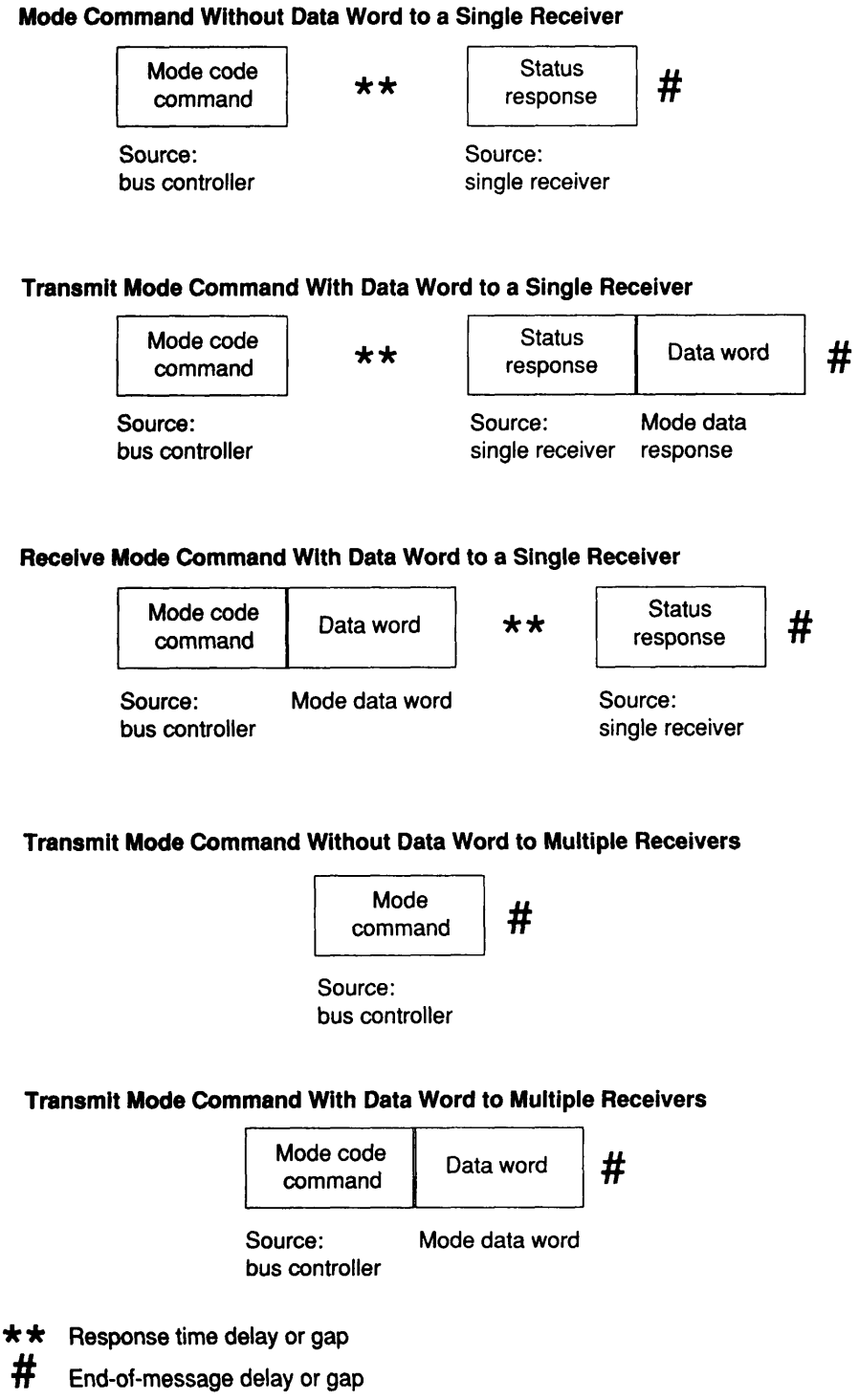


Figure 20-1. Mode Command Message Transfer Formats

Basically, this mode command causes the RT to transmit only the status word associated with the previous valid command. In other words, the RT should respond with the same status word that it transmitted for the last received valid command (not counting the transmit status word mode code).

The status word associated with this mode code (00010) is shown in figure 3 of 1553B and contains the same information as the status word defined in 4.3.3.5.3. Notice 2 (30.5.1) states that the RTstatus word transmitted by an RT shall contain valid information at all times, e.g., following RT power-up, during initialization, and during normal operation.

If the BC needs both the last status word and the command word, the transmit last command word mode command will provide both without updating the status word.

4.3.3.5.1.7.4 Initiate self-test. This command shall be used to initiate self-test within the RT. The RT shall transmit the status word as specified in 4.3.3.5.3.

The initiate self-test mode command (00011) is provided to initiate built-in test (BIT) circuitry within RTs. The mode code is usually followed (after sufficient time for test completion) by a transmit BIT word mode command that yields the results of the test. The message formats provided for this mode command allow for both individual requests and multiple requests. Notice that the initiate self-test mode command is associated with multiplex system terminal hardware only.

For dual standby-redundant systems, Notice 2 contains additional requirements and definitions (see 30.4.4).

4.3.3.5.1.7.14 Transmit built-in-test (BIT) word. This command shall cause the RT to transmit its status word as specified in 4.3.3.5.3 followed by a single data word containing the RT BIT data. This function is intended to supplement the available bits in the status word when the RT hardware is sufficiently complex to warrant its use. The data word, containing the RT BIT data, shall not be altered by the reception of a transmit last command or a transmit status word mode code. This function shall not be used to convey BIT data from the associated subsystem(s).

The transmit BIT word mode command (10011) provides the BIT results available from a terminal, as well as the status word. Obviously, broadcast by BCs of this command is not allowed. The internal contents of the BIT data word are provided to supplement the appropriate bits already available via the status word for complex terminals. Notice that the BIT word within the RT "...shall not be altered by the reception of a transmit last command or transmit status word mode code" received by the terminal. This allows error handling and recovery procedures to be used without changing the error data recorded in this word. However, the RT will only save the last command, and the status code field (of the status word) will not be changed, if transmit last command or transmit status word mode commands are transmitted. If, however, any other transmissions are made to the RT, the status code field may change, for example if a message error occurred during the transmission. (See 4.3.3.5.1.7.3 and 4.3.3.5.1.7.13.)

Also, note that the function of transmitting RT BIT data"... shall not be used to convey BIT data from the associated subsystem (s)."

Subsystem fault investigation, when indicated by the subsystem flag, is not specified or otherwise restricted by 1553B. Therefore, system designers must make the necessary provisions.

4.3.3.5.1.7.5 Transmitter shutdown. This command (to only be used with dual redundant bus systems) shall cause the RT to disable the transmitter associated with the redundant bus. The RT shall not comply with a command to shut down a transmitter on the bus from which this command is received. In all cases, the RT shall respond with a status word as specified in 4.3.3.5.3 after this command.

4.3.3.5.1.7.6 Override transmitter shutdown. This command (to only be used with dual redundant bus system) shall cause the RT to enable a transmitter which was previously disabled. The RT shall not comply with a command to enable a transmitter on the bus from which this command is received. In all cases, the RT shall respond with a status word as specified in 4.3.3.5.3 after this command.

4.3.3.5.1.7.15 Selected transmitter shutdown. This command shall cause the RT to disable the transmitter associated with a specified redundant data bus. The command is designed for use with systems employing more than two redundant buses. The transmitter that is to be disabled shall be identified in the data word following the command word in the format as specified in 4.3.3.5.2. The RT shall not comply with a command to shutdown a transmitter on the bus from which this command is received. In all cases, the RT shall respond with a status word as specified in 4.3.3.5.3.

4.3.3.5.1.7.16 Override selected shutdown. This command shall cause the RT to enable a transmitter which was previously disabled. The command is designed for use with systems employing more than two redundant buses. The transmitter that is to be enabled shall be identified in the data word following the command word in the format as specified in 4.3.3.5.2. The RT shall not comply with a command to enable a transmitter on the bus from which this command is received. In all cases, the RT shall respond with a status word as specified in 4.3.3.5.3.

Four mode commands are provided to control transmitters associated with terminals in a system. These commands can be sent to a single receiver or broadcast to multiple users.

The transmitter shutdown mode code (00100) is used in a dual standby-redundant bus structure where the command causes the transmitter associated with the redundant bus to terminate transmissions. No data word is provided for this mode. Note that 1553B does not specify whether or not to disable the receiver when the transmitter is disabled. If the receiver is left active, the RT may accept data it receives without the benefit of being able to respond if its bus is shut down. To disable both transmitters on an RT, the receivers must remain active. The option to disable the receiver for this mode code is left to the designer.

The override transmitter shutdown mode code (00101) is used in a dual standby-redundant bus structure where the command allows the previously disabled transmitter associated with the redundant bus to transmit when commanded by a normal bus command initiated by the active BC. No data word is provided for this mode code.

The selected transmitter shutdown mode code (10100) is used in a multiple (greater than two) redundant bus structure where the command causes the selected transmitter to terminate transmissions on its bus. A data word is used to identify the selected transmitter.

The override-selected transmitter shutdown mode code (10101) is used in a multiple (greater than two) redundant bus structure. This mode code allows the selected transmitter to transmit on its bus when a normal bus mode command is initiated by the active BC. A data word is used to identify the selected transmitter.

4.3.3.5.1.7.7 Initial terminal flag (T/F) bit. This command shall cause the RT to set the T/F bit in the status word specified in 4.3.3.5.3 to logic zero until otherwise commanded. The RT shall transmit the status word as specified in 4.3.3.5.3.

The inhibit terminal flag (T/F) mode code (00110) is used to set the T/F bit in the status word to an unfailed condition, regardless of the actual state of the terminal being addressed. This mode code is used primarily to prevent continued interrupts of the error handling and recovery system when the failure has been noted and the system reconfigured as required. This mode code prevents reporting of the future failures that normally

would be reported using the T/F in each subsequent status word response. The message format associated with the mode code allows for both single receivers and multiple receivers to respond. No data word is required with this mode code. Note that the T/F is implicitly limited to faults within the terminal.

4.3.3.5.1.7.8 Override inhibit T/F bit. This command shall cause the RT to override the inhibit T/F bit specified in 4.3.3.5.1.7.7. The RT shall transmit the status word as specified in 4.3.3.5.3.

The override inhibit T/F mode code (00111) negates the inhibit function thus allowing the T/F bit in the status response to report the current condition of the terminal. This mode code can be transmitted by the active BC to both single and multiple receivers. There is no data word associated with this mode code.

4.3.3.5.1.7.9 Reset remote terminal. This command shall be used to reset the RT to a power up initialized state. The RT shall first transmit its status word, and then reset.

The reset remote terminal mode code (01000) causes the addressed terminal to reset itself to a power-up initialized state. This mode code may be transmitted to either individual or multiple terminals.

For dual standby-redundant systems, Notice 2 contains additional requirements and definitions for this mode code (see 30.4.3).

4.3.3.5.1.7.9 Transmit vector word. This command shall cause the RT to transmit a status word as specified in 4.3.3.5.3 and a data word containing service request information.

The transmit vector word mode code (10000) is associated with the service request bit in the status word and is used to determine specific service being required by the terminal. The service request bit and the transmit vector word are the only means available (using 1553 protocol) for the terminal to request the scheduling of an asynchronous message if the terminal has more than one service request. The message format for this single receiver operation contains a data word associated with the response of the terminal. Figure 20-2 illustrates the message formats associated with this mode command.

4.3.3.5.1.7.13 Transmit last command word. This command shall cause the RT to transmit its status word as specified in 4.3.3.5.3 followed by a single data word which contains bits 4-19 of the last command word, excluding a transmit last command word mode code received by the RT. This mode command shall not alter the state of the RT's status word.

The transmit last command mode code (10010) is used in the error handling and recovery process to determine the last valid command received by the terminal, except for this mode code. The message format associated with the single receiver last command word contains a data word from the responding terminal. The data word contains the 16 bits of the last valid command word received. Notice that this mode command will not alter the state of the RT status word. This fact allows this mode command to be used in error handling and recovery operations without affecting the status word, which can have added error data.

4.3.3.5.1.7.10 Reserved mode codes (01001 to 01111). These mode codes are reserved for future use and shall not be used.

4.3.3.5.1.7.17 Reserved mode codes (10110 to 11111). These mode codes are reserved for future use and shall not be used.

Each of the mode code types (with and without data words) have several unused mode codes that are reserved for future use and may not be used in any systems complying with any version of the standard.

4.3.3.5.2 Data word. A data word shall be comprised of a sync waveform, data bits, and a parity bit (see figure 3).

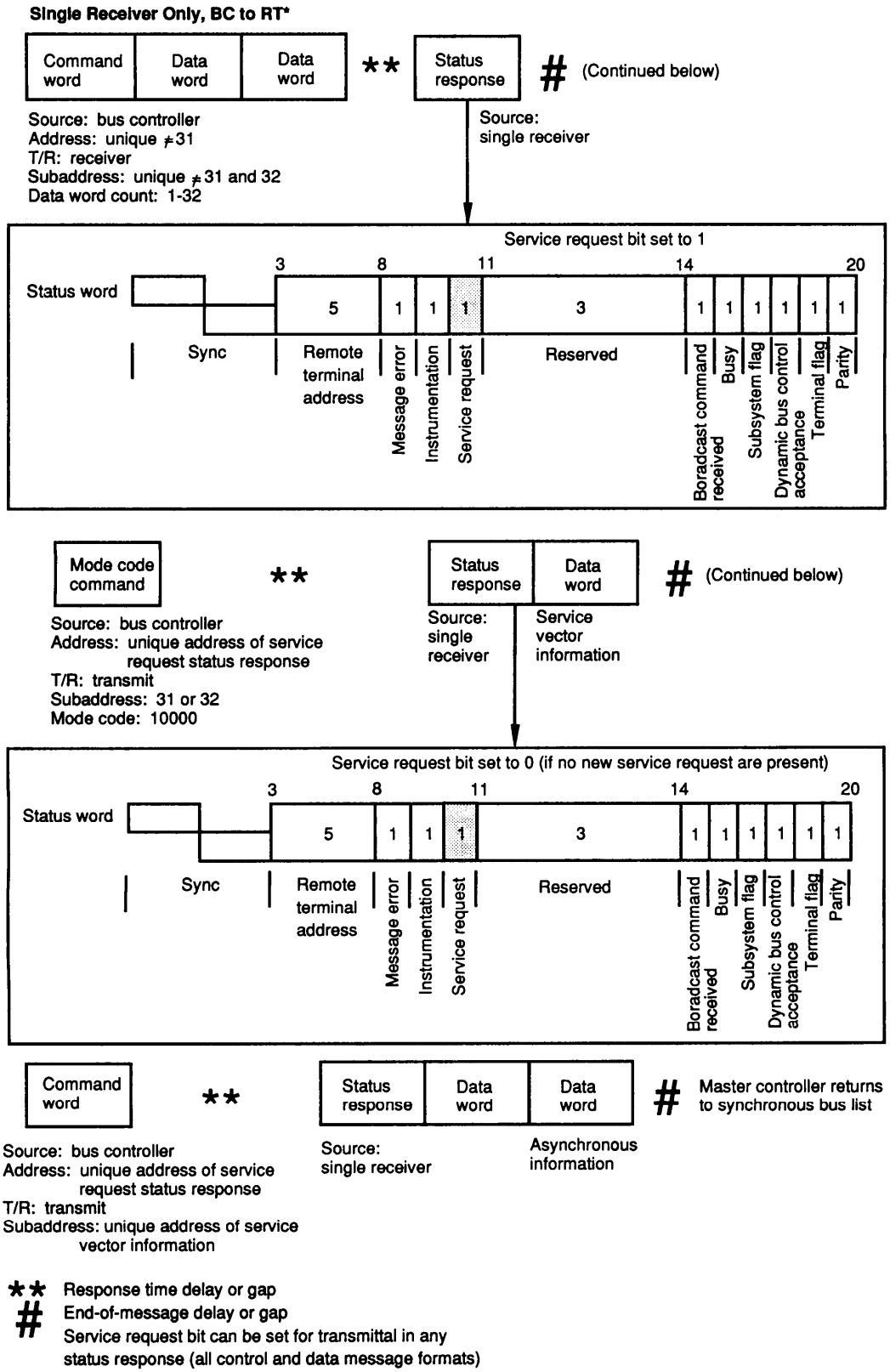


Figure 20-2. Transmit Vector Word Transfer Format

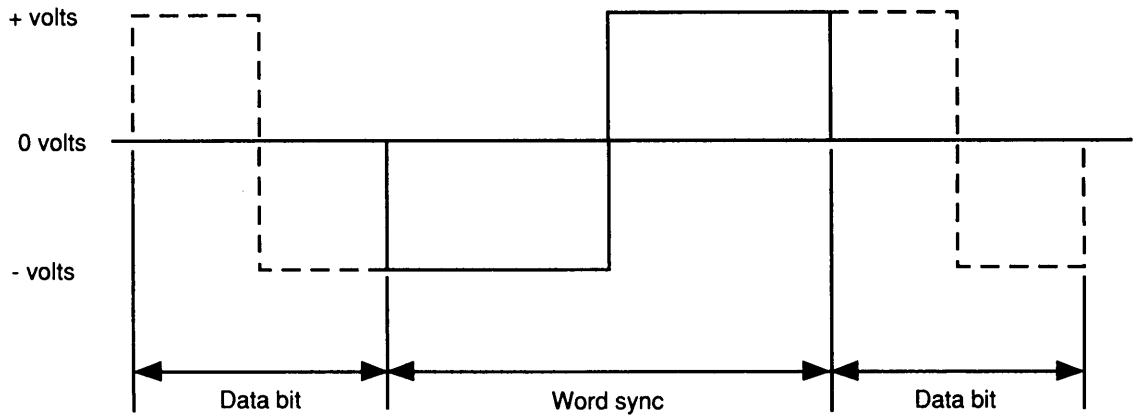


Figure 5 of 1553B. Data Sync

Figure 3 of 1553B illustrates the 1553B data word.

4.3.3.5.2.1 Sync. The data sync waveform shall be an invalid Manchester waveform as shown on figure 5. The width shall be three bit times, with the waveform being negative for the first one and one-half bit times, and then positive for the following one and one-half bit times. Note that if the bits preceding and following the sync are logic ones, then the apparent width of the sync waveform will be increased to four bit times.

4.3.3.5.2.2 Data. The sixteen bits following the sync shall be utilized for data transmission as specified in 4.3.2.

4.3.3.5.2.3 Parity. The last bit shall be utilized for parity as specified in 4.3.3.5.1.6.

Data words are used to transmit parameter data, which is the goal of the information transfer system. Data words are distinguished from command and status words by the inverted three-bit sync pattern. Both packed and unpacked data may be transmitted in the 16-bit data field. Odd parity on the data field provides data integrity identical to the command and status word formats.

4.3.3.5.3 Status word. A status word shall be comprised of a sync waveform, RT address, message error bit, instrumentation bit, service request bit, three reserved bits, broadcast command received bit, busy bit, subsystem flag bit, dynamic bus control acceptance bit, terminal flag bit, and a parity bit. For optional broadcast operation, transmission of the status word shall be suppressed as specified in 4.3.3.6.7.

4.3.3.5.3.1 Sync. The status sync waveform shall be as specified in 4.3.3.5.1.1.

4.3.3.5.3.2 RT address. The next five bits following the sync shall contain the address of the RT which is transmitting the status word as defined in 4.3.3.5.1.2.

The status word is part of the basic overhead requirements of the data bus system. The status word is shown in figure 3 of 1553B and is divided into the following fields:

a. Sync (same as command sync).

b. Remote terminal address.

c. Status.

d. Parity(P).

A five-bit field identifies the transmitting (remote) terminal address, while remote terminal status is based on data in the status field, which consists of the following information:

a. Message error bit.

b. Instrumentation bit.

c. Service request bit.

d. Reserved field (3 bits).

e. Broadcast command received bit.

f. Busy bit.

g. Subsystem flag bit.

h. Dynamic bus control acceptance bit.

i. Terminal flag bit.

Notice 2 has additional requirements for the status word of dual standby-redundant systems (see 30.5.1).

4.3.3.5.3.3 Message error bit. The status word bit at bit time nine (see figure 3) shall be utilized to indicate that one or more of the data words associated with the preceding receive command word from the bus controller has failed to pass the RT's validity tests as specified in 4.4.1.1. This bit shall also beset under the conditions specified in 4.4.1.2, 4.4.3.4 and 4.4.3.6. A logic one shall indicate the presence of a message error, and a logic zero shall show its absence. All RT's shall implement the message error bit.

The key to understanding the message error (ME) bit lies in 4.4.3.6. First, the command word must be valid and have the RT's assigned address. Then, if there is a data word validity problem or any words are not contiguous, the ME bit is set to a logic 1 in the status word but the status word is not transmitted. The ME bit can be obtained by using either of the two mode commands: transmit status or transmit last command. The only time the ME bit is set and the status word is transmitted in response to valid receive or transmit commands is per the illegal command detection response of 4.4.3.4.

4.3.3.5.3.4 Instrumentation bit. The status word bit time of 10 (see figure 3) shall be reserved for the instrumentation blt and shall always be a logic O. This bit Is intended to be used in conjunction with a logic one in blt time 10 of the command word to distinguish between a command word and a status word. The use of the instrumentation bit is optional.

The instrumentation bit in the status field is used to distinguish the status word from the command word. Since the sync field (three bits) is used to distinguish the command and status words from a data word, a mechanism to distinguish command and status is provided by the instrumentation bit. By setting this bit to logic 1 for the command word and to a logic 0 for all other conditions, the command and status words are identifiable. If used, this approach reduces the possible subaddress in the command word to 15 and requires subaddress 31 (11111) to be used to identify mode commands. In any case, the bit will remain set to logic 0 in the status word for all conditions.

4.3.3.5.3.5 Service reauest bit. The status word bit at bit time eleven (see figure 3) shall be reserved for the service request bit. The use of this bit is optional. This bit when used, shall indicate the need for the bus controller to take specific predefine actions relative to either the RT or associated subsystem. Multiple subsystems, interfaced to a single RT, which individually require a service request signal shall logically OR their individual signals into the single status word bit. In the event this logical OR is performed, then the designer must make provisions in a separate data word to identify the specific requesting subsystem. The service request bit is intended to be used only to trigger data transfer operations which take place on an exception rather than periodic basis. A iogic one shall indicate the presence of a service request, and a logic zero its absence. If this function is not implemented, the bit shall be set to zero.

The service request bit is provided to indicate to the active BC that a RT is requesting service. When this bit in the status word is set to logic one, the active BC may take a predetermined action or use a mode command (transmit vector word) to identify the specific request. The message format for acquiring this is discussed under transmit vector word mode command (figure 20-2).

4.3.3.5.3.6 Reserved status bits. The status word bits at bit times tweive through fourteen are reserved for future use and shall not be used. These bits shall beset to a logic zero.

The three-bit field (12-14) is reserved; it cannot be used in any system that complies with the standard and must be set to logic zero.

4.3.3.5.3.7 Broadcast command received bit. The status word at bit time fifteen shall be set to a logic one to indicate that the preceding valid command word was a broadcast command and a logic zero shall show it was not a broadcast command. if the broadcast command option is not used, this bit shall be set to a logic zero.

The broadcast command received bit is set to logic one when the preceding valid command word was a broadcast command (address 31). Since broadcast message formats require the receiving RTs to suppress their status words, the broadcast command received bit is set to identify that the command was received properly. The message format shown in figure 20-3 can be used to check the validity of the broadcast message. The broadcast command received bit will be reset when the next valid command is received by the RT, unless the next valid command is transmit status word or transmit last command.

4.3.3.5.3.8 Busv bit. The status word bit at bit time sixteen (see figure 3) shall be reserved for the busy bit. The use of this bit is optional. This bit, when used, shaii indicate that the RT or subsystem is unable to move data to or from the subsystem in compliance with the bus controller's command. A logic one shall indicate the presence of a busy condition, and a logic zero its absence. in the event the busy bit is set in response to a transmit command, then the RT shall transmit its status word only. If this function is not implemented, the bit shall be set to logic zero.

The busy bit in the status word is set to logic one to indicate to the active BC that the RT is unable to move data to or from the subsystem in compliance with the BC command. An example of the message format associated with a busy condition is shown in figure 20-4. A busy condition can exist within a RT at any time causing it to be nonresponsive to a command to send data or to be unable to receive data. This condition can exist for all message formats. In each case except the broadcast message formats, the active BC will determine the busy condition immediately upon status response. In the case of the broadcast message formats, this information will not be known unless the receiving terminals are polled after the broadcast message requesting their status. If the status word has the broadcast received bit set, the message was received and the terminal was not busy.

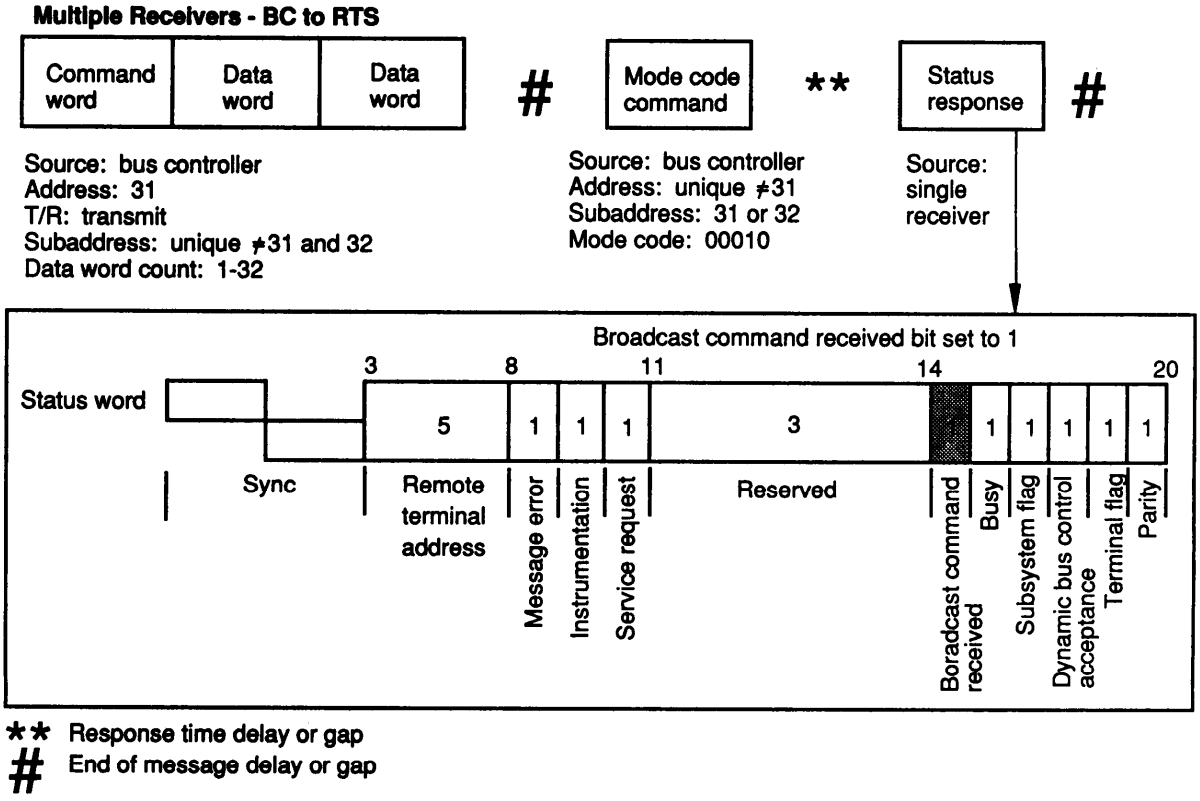


Figure 20-3. Broadcast Command Receive Bit

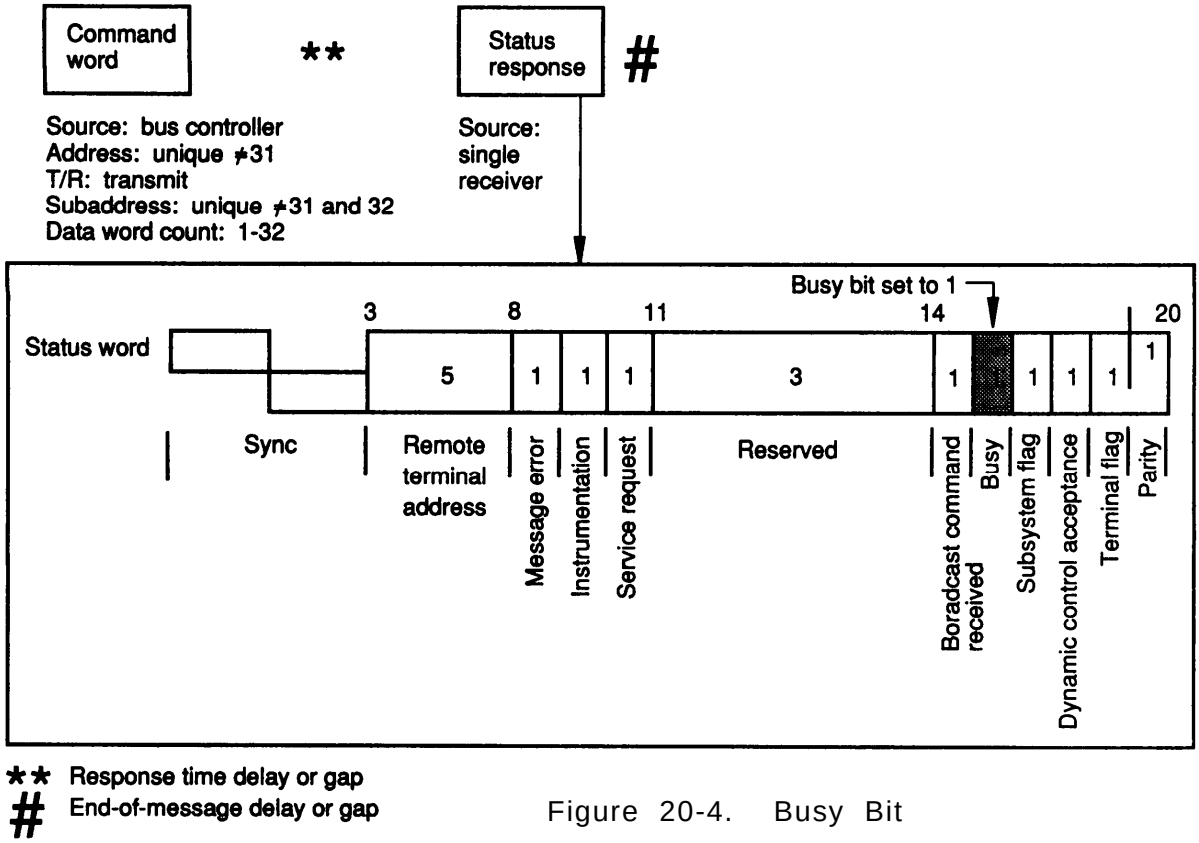


Figure 20-4. Busy Bit

For dual standby-redundant systems, Notice 2 has additional requirements for the busy bit implementation (see 30.5.3).

4.3.3.5.3.9 Subsystem flag bit. The status word bit at bit time seventeen (see figure 3) shall be reserved for the subsystem flag bit. The use of this bit is optional. This bit, when used, shall flag a subsystem fault condition, and alert the bus controller to potentially invalid data. Multiple subsystems, interfaced to a single RT, which individually require a subsystem flag bit signal shall logically OR their individual signals into the single status word bit. In the event this logical OR is performed, then the designer must make provisions in a separate data word to identify the specific reporting subsystem. A logic one shall indicate the presence of the flag, and a logic zero its absence. If not used, this bit shall be set to logic zero.

The subsystem flag bit is provided to indicate to the active BC that a subsystem fault condition exists and that data being requested from the subsystem may be invalid. The subsystem flag maybe set in any transmitted status word.

4.3.3.5.3.10 Dynamic bus control acceptance bit. The status word bit at bit time eighteen (see figure 3) shall be reserved for the acceptance of dynamic bus control. This bit shall be used if the RT implements the optional dynamic bus control function. This bit, when used, shall indicate acceptance or rejection of a dynamic bus control offer as specified in 4.3.3.5.1.7.1. A logic one shall indicate acceptance of control, and a logic zero shall indicate rejection of control. If this function is not used, this bit shall be set to logic zero.

This bit is provided to indicate the acceptance by an RT of the bus control offer by the presently active BC to become the next BC. The offer of bus control occurs when the presently active BC has completed its established message list and issues a dynamic bus control mode command to the RT that is to be the next potential controller. To accept the offer, the potential BC sets its dynamic bus control acceptance bit in the status word and transmits the status word. The establishment of who the next potential controller will be is a system issue.

4.3.3.5.3.11 Terminal flat bit. The status word bit at bit time nineteen (see figure 3) shall be reserved for the terminal flag function. The use of this bit is optional this bit, when used, shall flag a RT fault condition. A logic one shall indicate the presence of the flag, and a logic zero, its absence. If not used, this bit shall be set to logic zero.

The T/F bit is set to a logic one to indicate a fault within the RT. This bit is used in connection with three mode commands:

a. Inhibit terminal flag.

b. Override inhibit terminal flag.

c. Transmit BIT word.

The first two mode commands deactivate and activate the functional operation of the bit. The transmit BIT word mode command is used to acquire more detailed information about the terminal failure.

4.3.3.5.3.12 Parity bit. The least significant bit in the status word shall be utilized for parity as specified in 4.3.3.5.1.6.

The use of a single parity bit per word was provided to identify any bit errors occurring during the transmission and detection of a word. This odd parity check will detect an odd number of bit errors occurring in a word. This requirement produces an undetected bit error rate of 10^{-12}, which was considered satisfactory for a general-purpose information transfer system. (See also 4.3.3.5.1.6 of 1553B.)

4.3.3.5.4 Status word reset. The status word bit, with the exception of the address, shall be set to logic zero after a valid command word is received by the RT with the exception as specified in 4.3.3.5.1.7. If the conditions which caused bits in the status word to be set (e.g., terminal flag) continue after the bits are reset to logic zero, then the affected status word bit shall be again set, and then transmitted on the bus as required.

Figure 3 of 1553B shows the status word and the information available in this field. The reason for the reset definition is to provide:

a. The ability to obtain the latest status information of the RT. This prevents conditions from being reported for longer than they actually exist.

b. The ability to obtain the status code analysis of the results for a previous valid command. This allows orderly error handling and recovery by the BC using the with error analysis data contained within this field or other data associated within the RT (e.g., last command word and BIT).

A reason for obtaining a status word that has not been reset was discussed in 4.3.3.5.1.7.3. Even though all mode codes are referenced in 4.3.3.5.4, only two are required to retain the last status word in the terminal:

a. Transmit status word.

b. Transmit last command word.

In other words, all other valid messages received, including mode commands, will allow the RT to reset the status word, except these two.

Both of these mode codes can be transmitted to the RT without changing the bits in the status code field of the last valid command word in question. Therefore, it is essential that an error recovery procedure be established for the BC that takes into account (1) the ability of the RT hardware to collect error data, (2) the information transfer formats that must be implemented by the BC to prevent loss of data, and (3) the ability of the BC hardware and software to receive and react to these data. As many as three mode codes maybe involved in this process:

a. Transmit last command.

b. Transmit status word.

c. Transmit BIT word.

4.3.3.6 Message formats. The messages transmitted on the data bus shall be in accordance with the formats on figures 6 and figure 7. The maximum and minimum response times shall be as stated in 4.3.3.7 and 4.3.3.8. No message formats, other than those defined herein, shall be used on the bus.

For dual standby-redundant systems, as a minimum, Notice 2 requires that the RTs be capable of RT-to-BC, BC-to-RT, and RT-to-RT transfers, as well as mode command (without data word) transfers (see 30.8).

The command response protocol provides for two types of message formats: data messages and control messages. The 1553B paragraphs pertaining to data messages will be discussed first.

4.3.3.6.1 Bus controller to remote terminal transfers. The bus controller shall issue a receive command followed by the specified number of data words. The RT shall, after message validation, transmit a status word back to the controller. The command and data words shall be transmitted in a contiguous fashion with no interword gaps.

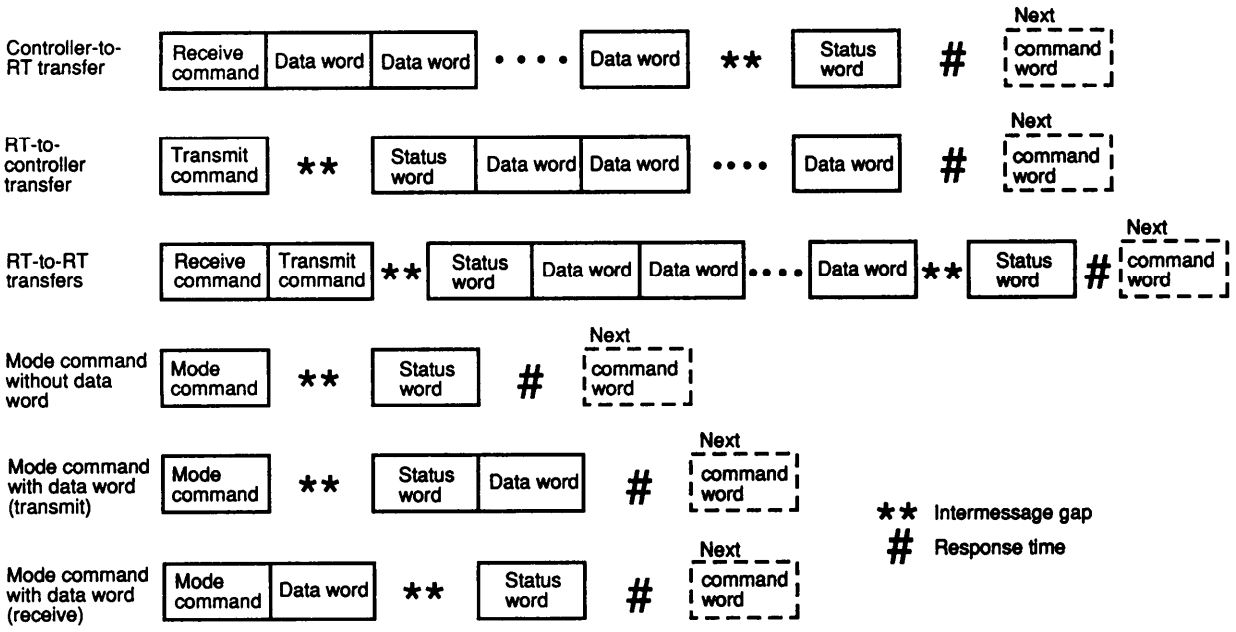


Figure 6 of 1553B. Information Transfer Formats

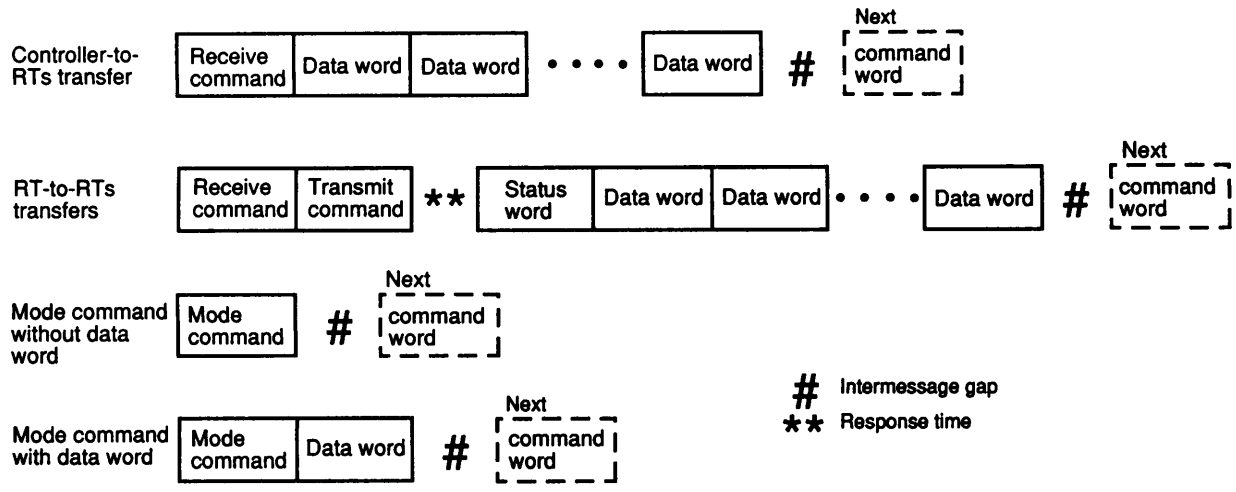


Figure 7 of 1553B. Broadcast Information Transfer Formats

4.3.3.6.2 Remote terminal to bus controller transfers. The bus controller shall issue a transmit command to the RT. The RT shall, after command word validation, transmit a status word back to the bus controller, followed by the specified number of data words. The status and data words shall be transmitted in a contiguous fashion with no interword gaps.

4.3.3.6.3 Remote terminal to remote terminal transfers. The bus controller shall issue a receive command to RT A followed contiguously by a transmit command to RT B. RT B shall, after command verification, transmit a status word followed by the specified number of data words. The status and data words shall be transmitted in a contiguous fashion with no gap. At the conclusion of the data transmission by RT B, RT A shall transmit a status word within the specified time period.

4.3.3.6.7 Optional broadcast command. See 10.6 for additional information on the use of the broadcast command.

4.3.3.6.7.1 Bus controller to remote terminal(s) transfer (broadcast). The bus controller shall issue a receive command word with 11111 in the RT address field followed by the specified number of data words. The command word and data words shall be transmitted in a contiguous fashion with no gap. The RT(s) with the broadcast option shall after message validation, set the broadcast command received bit in the status word as specified in 4.3.3.5.3.7 and shall not transmit the status word.

4.3.3.6.7.2 Remote terminal to remote terminal(s) transfers (broadcast). The bus controller shall issue a receive command word with 11111 in the RT address field followed by a transmit command to RT A using the RT's address. RT A shall, after command word validation, transmit a status word followed by the specified number of data words. The status and data words shall be transmitted in a contiguous fashion with no gap. The RT(s) with the broadcast option, excluding RT A, shall after message validation, set the broadcast received bit in the status word as specified in 4.3.3.5.3.7 and shall not transmit the status word.

The above message formats are used to transfer data among the subsystems. There are two data message types: single receiver and multiple receiver. They are transmitted as follows:

a. Single receiver.

1. BC to RT—Typically, this type of data transfer is related to the role of the processor that has the bus control function (e.g., a mission computer may have the requirement to be the data source for subsystems).

2. RT to BC-This type of data transfer is used to get data to the BC.

3. RT to RT—The BC does not need to receive and retransmit all data, even though it is in control of the bus. An important class of data transfers is the direct transfer of data from one RT to another, which can be used if the processor that contains the BC is not involved in processing the data and if data reformatting is not required. The BC may monitor the RT-to-RT transmission and thus receive the data.

b. Multiple receivers.

1. BC to multiple RTs.

2. RT to multiple RTs.

Each of these data message types is transmitted using command and status words for control operation. The command word is used to:

a. Identify the receiving terminal(s).

b. Identify if data are to be received or transmitted by the receiving terminal(s).

c. Identify the specific message (subaddress) within the RTs.

d. Notify the terminal(s) of the number of data words to be received or transmitted.

The command, status, and data word formats for these messages are described in 4.3.3.5.1, 4.3.3.5.2, and 4.3.3.5.3. Using these word formats, the format for data message transmissions is developed. Single-receiver data message formats are shown in figure 20-5. The data message formats used when there are multiple receiving terminals are shown in figure 20-6.

For duel standby-redundant systems, Notice 2 has additional requirements for using and implementing the broadcast command (see 30.6).

The 1553B paragraphs pertaining to control messages will now be discussed.

4.3.3.6.4 Mode command without data word. The bus controller shall issue a transmit command to the RT using a mode code specified in table l. The RT shall, after command word validation, transmit a status word.

4.3.3.6.5 Mode command with data word (transmit). The bus controller shall issue a transmit command to the RT using a mode code specified in table l. The RT shall, after command word validation, transmit a status word followed by one data word. The status word and data word shall be transmitted in a continuous fashion with no gap.

4.3.3.6.6 Mode command with data word (receive). The bus controller shall issue a receive command to the RT using a mode code specified in table l, followed by one data word. The command word and data word shall be transmitted in a contiguous fashion with no gap. The RT shall, after command and data word validation, transmit a status word back to the controller.

4.3.3.6.7.3 Mode command without data word (broadcast). The bus controller shall issue a transmit command word with 11111 in the RTaddress field, and a mode code specified in table l. The RT(s) with the broadcast option shall after command word validation, set the broadcast received bit in the status word as specified in 4.3.3.5.3.7 and shall not transmit the status word.

4.3.3.6.7.4 Mode command with data word (broadcast). The bus controller shall issue a receive command word with 11111 in the RT address field and a mode code specified in table l, followed by one data word. The command word and data word shall be transmitted in a contiguous fashion with no gap. The RT(s) with the broadcast option shall after message validation, set the broadcast received bit in the status word as specified in 4.3.3.5.3.7 and shall not transmit the status word.

Message formats within this protocol can be transmitted to a single receiver or to multiple receivers based on the command word address for the message.

Mode commands are specified by setting the subaddress/mode field of the command word to either 32 (00000) or 31 (11111). All control messages originate with the BC and are received by a single receiver or by multiple receivers (broadcast). A terminal address value of 31 (11111) in the command word indicates a broadcast message, while any other terminal address is used to identify unique mode commands to terrninals on the bus. The mode command information is in the word count/mode code field of the command word and in the attached data word if allowed by the mode command. Figure 20-7 shows various legal mode command formats, with and without data word.

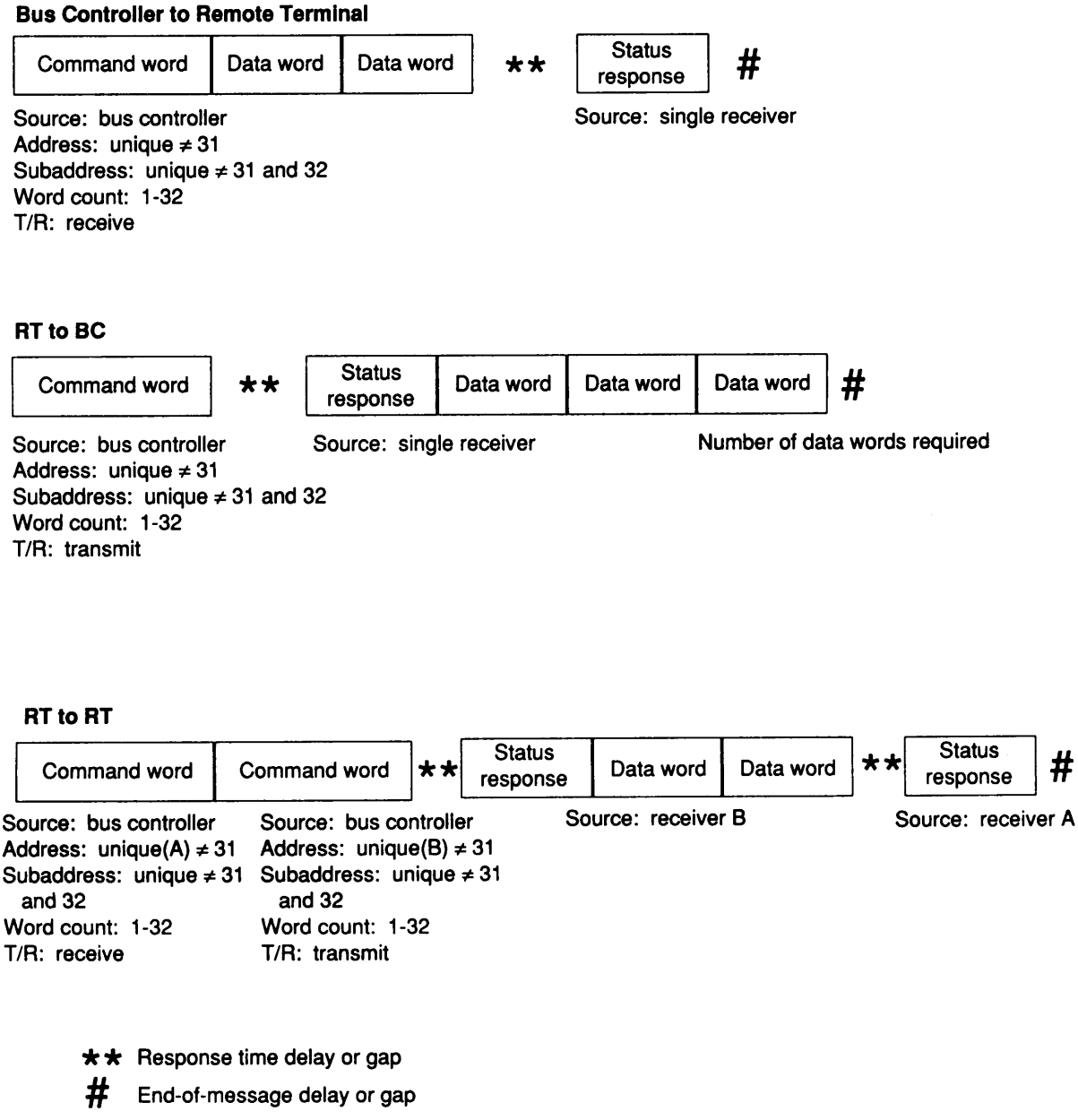


Figure 20-5. Single-Receiver Data Message Formats

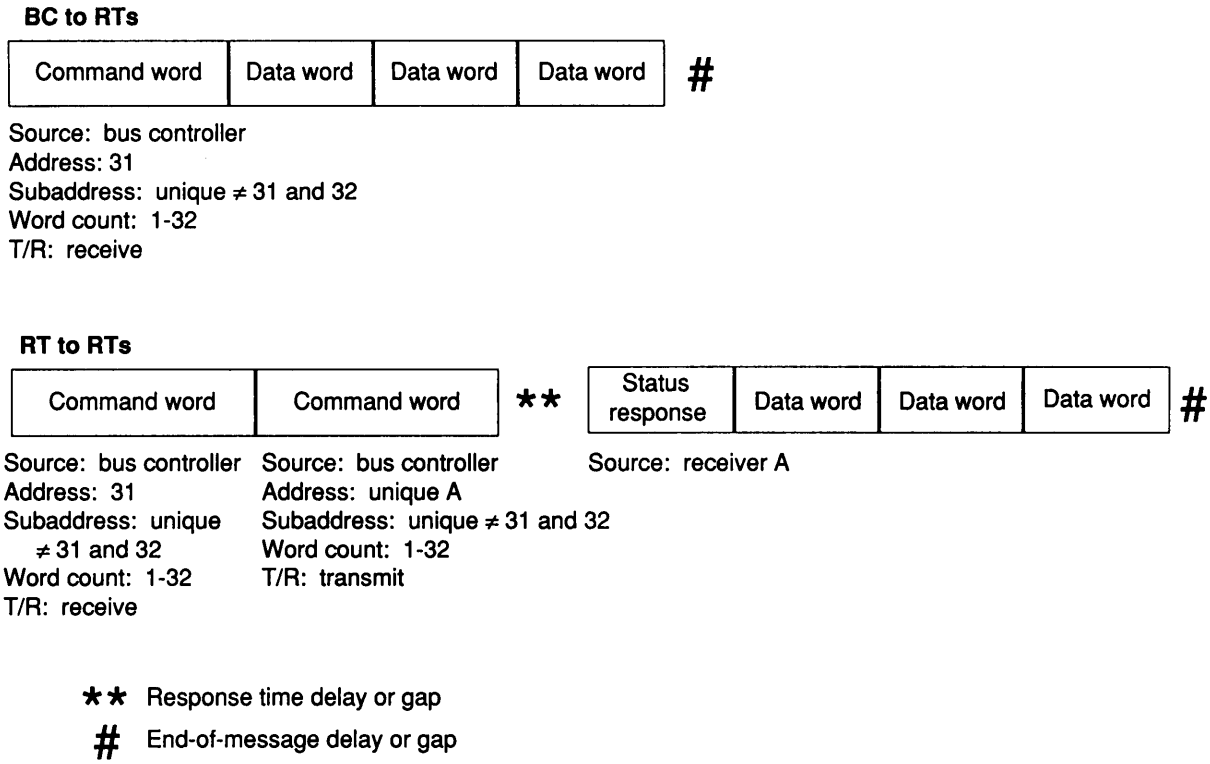


Figure 20-6. Multiple-Receiver Data Message Formats

43.3.7 Intermessage gap. The bus controller shall provide a minimum gap time of 4.0 microseconds (us) between messages as shown on figures 6 and figure 7. This time period, shown as T on figure 8, is measured at point A of the bus controller as shown on figure 9 or figure 10. The time is measured from the mid-bit zero crossing of the last bit of the preceding message to mid-zero crossing of the next command word sync.

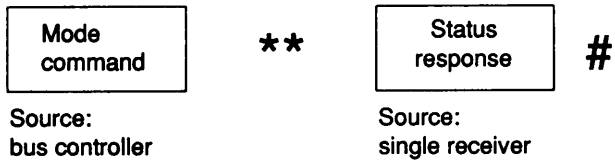
The purpose of this requirement is to clearly identify that the BC shall not transmit contiguous messages (must have a gap) and that the maximum response time (12 μs, see 4.3.3.8) does not apply to gaps between messages. The BC may issue messages with a gap time greater than 4 ps.

4.3.3.8 Response time. The RT shall respond, in accordance with 4.3.3.6, to a valid command word within the time period of 4.0 to 12.0 μs. This time period, shown as T on figure 8, is measured at point A of the RT as shown on figure 9 or figure 10. The time is measured from the mid bit zero crossing of the last word as specified in 4.3.3.6 and as shown on figures 6 and figure 7 to the mid-zero crossing of the status word sync.

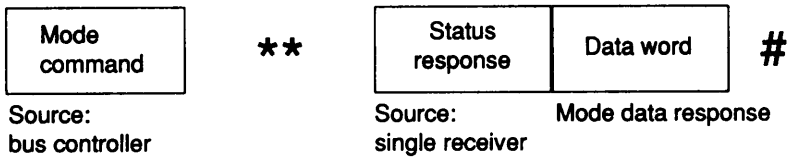
The point of measurement to establish the RT response time is defined here. The measurement is made using the previous midbit (zero) crossing and next midbit crossing as reference points.

4.3.3.9 Minimum no-reponse time-out. The minimum time that a terminal shall wait before considering that a response as specified in 4.3.3.8 has not occurred shall be 14.0 μs. The time is measured from the mid-bit zero crossing of the last bit of the last word to the mid-zero crossing of the expected status word sync at Point A of the terminal as shown on figure 9 or figure 10.

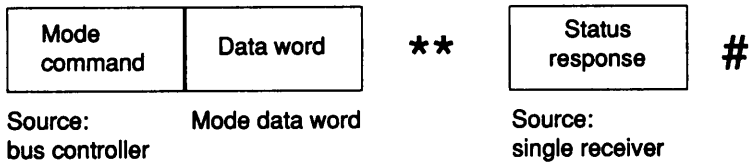
Mode Command Without Data Word to a Single Receiver



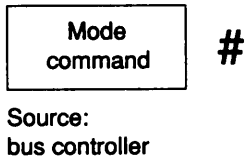
Transmit Mode Command With Data Word to a Single Receive



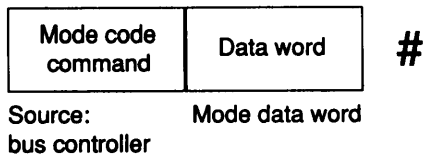
Reoeive Mode Command With Data Word to a Single Receive



Transmit Mode Command Without Data Word to Multiple Receivers



Transmit Mode Command With Data Word to Multiple Receivers



** Response time delay or gap

End-of-message delay or gap

Figure 20-7. Mode Command Transfer Formats

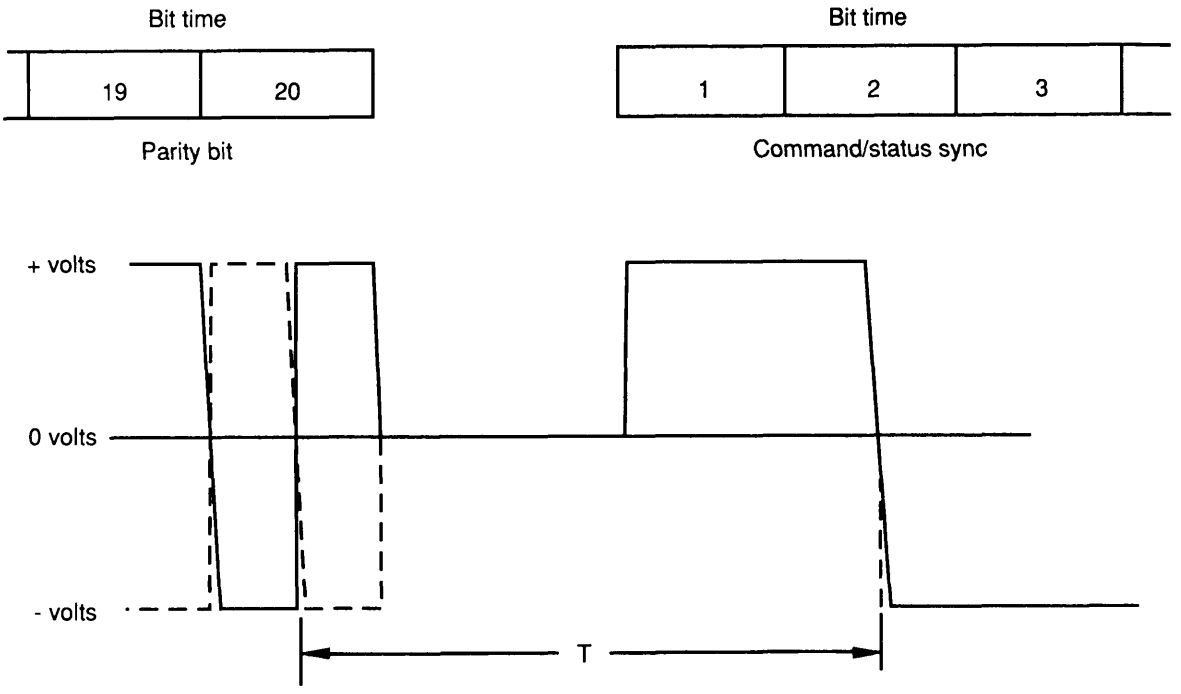


Figure 8 of 1553B. Intermessage Gap and Response Time.

This requirement is provided to clarify the minimum time that a BC will wait before concluding that the RT is not going to respond as requested.

For dual standby-redundant systems, Notice 2 specifies timeout requirements for the receiving RT during an RT-to-RT transfer (see 30.9).

4.4 Terminal Operation.

This portion of 1553B was provided to clarify the various terminals identified in the standard and their performance requirements. The first section covers common operational requirements that apply to all devices connected to the data bus system. Specific requirements include: BC (4.4.2), RT (4.4.3), and bus **monitor (4.4.4).**

4.4.1 Common operation. Terminals shall have common operating capabilities as specified in the following paragraphs.

4.4.1.1 Word validation. The terminal shall insure that each word conforms to the following minimum criteria:

a. The word begins with a valid sync field.

b. The bits area valid Manchester II code.

c. The information field has 16 bits plus parity.

d. The word parity is odd.

When a word fails to conform to the preceding criteria, the word shall be considered invalid.

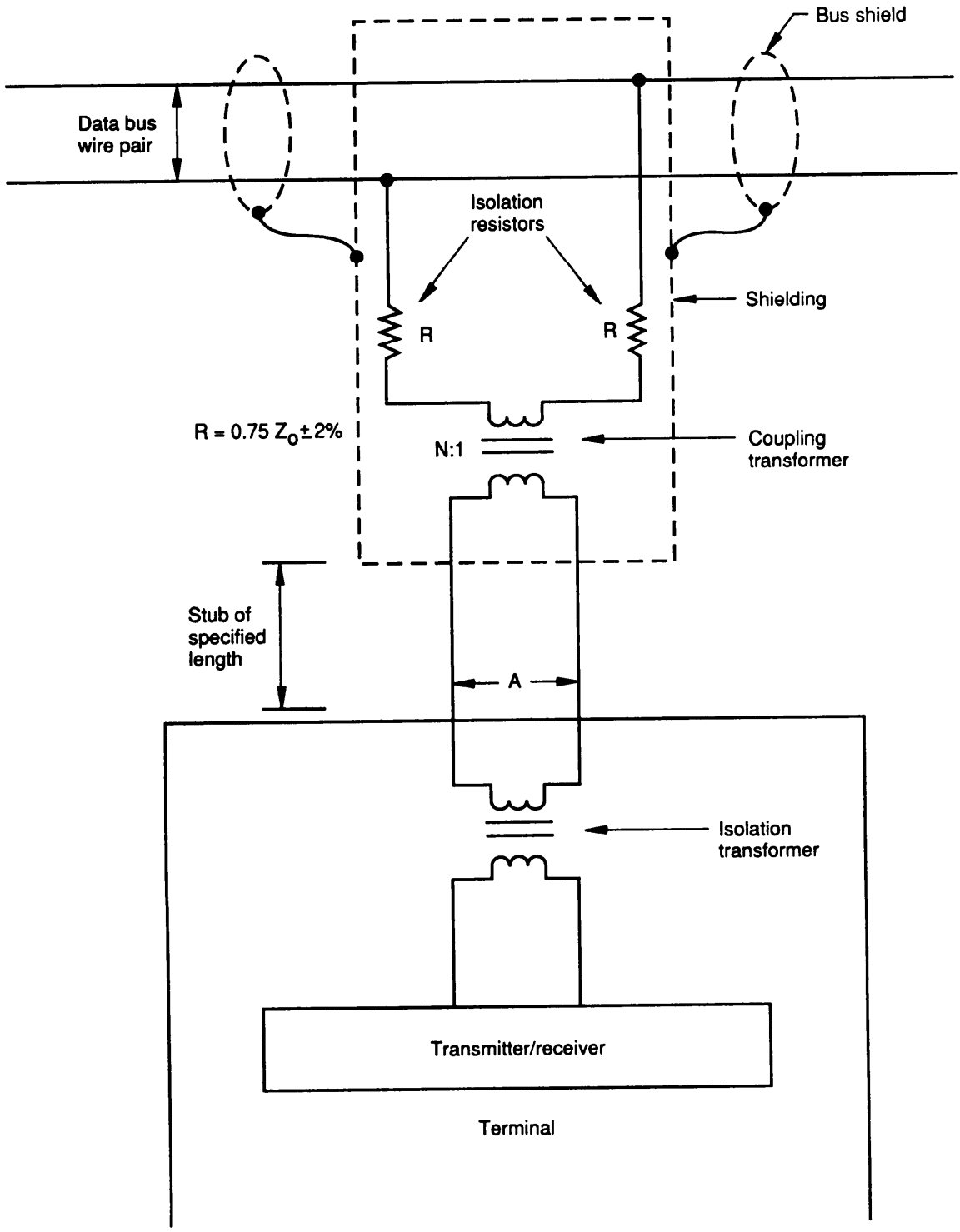


Figure 9 of 1553B. Data Bus Interface Using Transformer Coupling

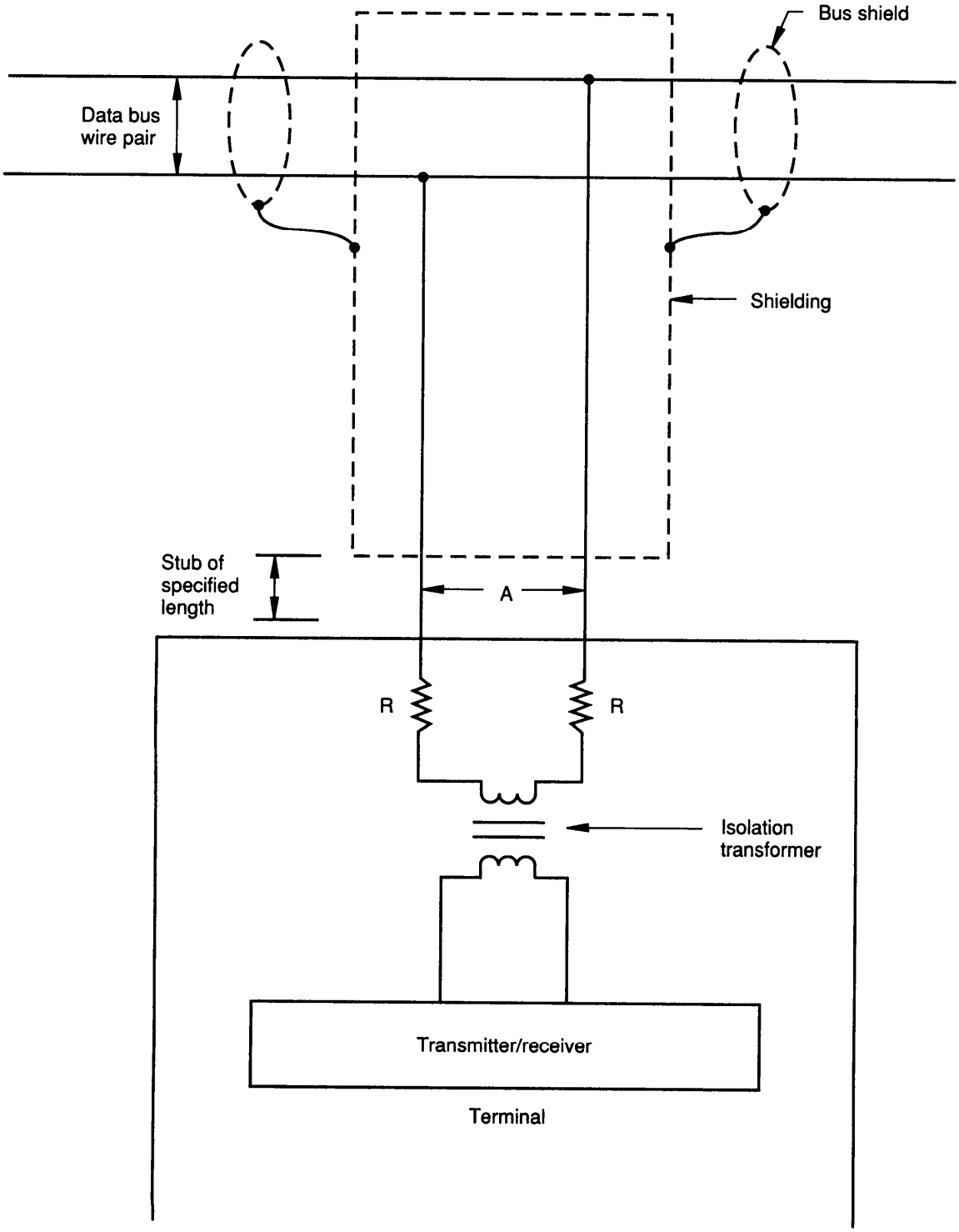


Figure 10 of 1553B. Data Bus Interface Using Direct Coupling

4.4.1.2 Transmission continuity. The terminal shall verify that the message is contiguous as defined in 4.3.3.6. Improperly timed data syncs shall be considered a message error.

4.4.1.3 Terminal fail-safe. The terminal shall contain a hardware implemented time-out to preclude a signal transmission of greater than 800.0 μs. This hardware shall not preclude a correct transmission in response to a command. Reset of this time-out function shall be performed by the reception of a valid command on the bus on which the time-out has occurred.

The common operation associated with BCS, RTs, and bus monitors connected to the data bus system are described in 4.4.1 through 4.4.1.3.

Contiguous data are as defined by paragraph 5.2.1.3.6 of the RT Validation Test Plan (Section 100 of this handbook). A timed-out fail-safe timer is always reset by reception of a valid command. There are several mechanisms to reset the fail-safe timer described in 1553B. These include:

a. Reception of a valid command on the bus on which the timeout has occurred (4.4.1.3).

b. Use of the mode command override transmitter shutdown (00101 for a two-bus system or 10101 for multiple-bus systems) on an alternate bus.

c. Use of the mode command reset RT (01000), which causes the RT to assume a power-up initialized state.

Items band care optional ways to reset the timer and may depend on system and hardware implementations. However, the preferred reset approach is to transmit the appropriate mode code.

4.4.2 Bus controller operating. A terminal operating as a bus controller shall be responsible for sending data bus commands, participating in data transfers, receiving status responses, and monitoring system status as defined in this standard. the bus controller function maybe embodied as either a stand-alone terminal, whose sole function is to control the data bus(s), or contained within a subsystem. Only one terminal shall be in active control of a data bus at any one time.

4.4.3 Remote terminal.

4.4.3.1 Operation. A remote terminal RT shall operate in response to valid commands received from the bus controller. The RT shall accept a command word as valid when the command word meets the criteria of 4.4.1.1, and the command word contains a terminal address which matches the RT address or an address of 11111, if the RT has the broadcast option.

4.4.3.2 Superseding valid commands. The RT shall be capable of receiving a command word on the data bus after the minimum intermessage gap time as specified in 4.3.3.7 has been exceeded, when the RT is not in the time period T as specified in 4.3.3.8 prior to the transmission of a status word, and when it is not transmitting on that data bus. A second valid command word sent to an RTshall take precedence over the previous command. The RT shall respond to the second valid command as specified in 4.3.3.8.

The intended purpose for the requirement for a superseding valid command is to allow the BC to reissue an identical transmission or issue a new transmission on the same bus to the same RT when an RT fails to respond to a command on that bus. This method is described as requiring a minimum time T (greater than a gap time but less than a full 32-word message) to occur prior to transmitting the second command. Therefore, the BC is assured that the RT is not responding, so a new command on the same bus is appropriate. Figure 8 in 1553B demonstrates this intermessage gap problem and solution.

Notice 2 pen-and-ink changes made to 4.4.3.2 are discussed later in the commentary on Notice 2 (20.2).

4.4.3.3 Invalid commands. A remote terminal shall not respond to a command word which fails to meet the criteria specified in 4.4.3.1.

Command words that fail to meet the word validation requirements cause the system to continue to look for a valid command word. When this condition occurs, it is identified as an invalid command; no change occurs to the status word and no response is transmitted by the RT.

The invalid command requirement also is used to cover failure in the decoding process of the command word. To prevent multiple responses by two or more terminals to a command word (one without a failure and one with) the terminal that cannot absolutely validate a command word must take the safe approach and reset the circuitry and continue to look for a valid command word that meets its particular requirements (address). All RTs should use this approach of not responding when there is a question about the commands. This approach is considered to be a fail-passive approach providing the least impact on the multiplex system.

4.4.3.4 Illegal command. An illegal command is a valid command as specified in 4.4.3.1, where the bits in the subaddress/mode field, data word count/mode code field, and the T/R bit indicate a mode command, subaddress, or word count that has not been implemented In the RT. It is the responsibility of the bus controller to assure that no illegal commands are sent out. The RT designer has the option of monitoring for illegal commands. If an RT that is designed with this option detects an illegal command and the proper number of contiguous valid data words as specified by the illegal command word, it shall respond with a status word only, setting the message error bit, and not use the information received.

Illegal commands are commands that have passed the validation test but are not part of terminal capability. These include command words where the subaddress/mode field, data word/mode code field, or the T/R bit are set such that they represent conditions not allowed in the system. An illegal command may be a combination of the above fields that is restricted or undefined by 1553B or the terminal designer. The BC is responsible for preventing illegal commands from being transmitted. Because the BC is responsible for all command and response message communications, it is a design goal that the BC not transmit illegal commands.

Two methods can be provided to meet this requirement: (1) careful generation of BC commands during development of the system, along with tight control of the change process during operational use, and (2) examination of failure modes of the controller hardware and software to determine potentially illegal generation and transmission of commands. An additional method of rejecting illegal commands in the multiplex system can be provided only by circuitry within the receiving RT. This approach is an optional capability for RTs built to the 1553B standard. If an RT with this capability detects an illegal command that meets all other validation requirements, the RT shall respond with a status word with only the message error bit set and not use the information sent or disregard the request for information.

4.4.3.5 Valid data reception. The remote terminal shall respond with a status word when a valid command word and the proper number of contiguous valid data words are received, or a single valid word associated with a mode code is received. Each data word shall meet the criteria specified in 4.4.1.1.

If the conditions in this paragraph are fulfilled, then the RT must respond with a status word. Valid data reception can also apply to broadcast messages, in which case a status word response will not be sent.

4.4.3.6 Invalid data reception. Any data word(s) associated with avaiid receive command that does not meet the criteria specified in 4.4.1.1 and 4.4.1.2 or an error in the data word count shall cause the remote terminai to set the message error bit in the status word to a logic one and suppress the transmission of the status word. if a message error has occurred, then the entire message shall be considered invalid.

A valid data reception for a nonbroadcast message requires a status response, whereas an invalid data reception suppresses the status response but requires certain other actions. This assumes message formats with associated data words, so mode commands without data words are rightly excluded from this group. Valid data reception for broadcast messages will suppress the status response, while invalid data reception will set the message error bit and suppress the status response. Therefore, all message formats containing at least one data word (e.g., broadcast data messages, nonbroadcast data messages, broadcast mode codes with a data word, and mode codes with a data word) are included in this requirement.

As stated in the requirement, the message command word has been validated and the error occurs in the data word portion of the message. The withholding or suppression of the status response alerts the BC error detection electronics to the fact that an incomplete message has occurred and some level of error recovery must occur. The setting of the message error bit in the status word that remains in the RT will provide additional information to the error recovery circuitry only if the BC requests the status word using the appropriate mode code.

Also notice that, if any part of the message is invalid, the entire received message must be considered invalid. This message invalidation requirement may cause problems for systems that have bit-oriented data rather than word or multiple word (message) oriented data. Errors in a word following the reception of good data will invalidate good data. It has been proposed that such a system invalidate all data words from the failure to the end of the message and use previously good data words. This approach, however, has not been allowed. Regardless of the approach, some system mechanisms will store the data and then tag the message as being invalid; others will not allow the user to receive the data. For the former, it is the responsibility of the user to examine the message valid indication prior to using the data; for the latter, the user must recognize that the data have not been updated.

4.4.4 Bus monitor operation. A terminal operating as a bus monitor shall receive bus traffic and extract selected information. While operating as a bus monitor, the terminal shall not respond to any message except one containing its own unique address if one is assigned. All information obtained while acting as a bus monitor shall be strictly used for off-line applications (e.g., flight test recording, maintenance recording or mission analysis) or to provide the back-up bus controller sufficient information to takeover as the bus controller.

A terminal may operate as a bus monitor for only two reasons: (1) information recording for offline analysis and (2) information source for backup BC. The unique feature of this terminal is that it has the ability to decode and accept for data storage any or all messages transmitted on the data bus without the knowledge of, or without affecting the operation of, the multiplex system or the terminals attached to the bus. A bus monitor can be made to respond by assigning a specific address to which it would respond, in which case it would act as an RT for that address and as a bus monitor for all the others.

4.5 Hardware characteristics.

4.5.1 Data bus characteristics.

4.5.1.1 Cable. The cable used for the main bus and all stubs shall be a two conductor, twisted, shielded, jacketed cable. The wire-to-wire distributed capacitance shall not exceed 30.0 picofarads per foot. The cables shall be formed with not less than four twists per foot where a twist is defined as a 360 degree rotation of the wire pairs; and, the cable shield shall provide a minimum of 75.0 percent coverage.

For dual standby-redundant applications, Notice 2 requires a minimum of 90.0% coverage for the shield (see 30.10.1).

4.5.1.2 Characteristic impedence. The nominal characteristic impedance of the cable (Z_0) shall be within the range of 70.0 ohms to 85.0 ohms at a sinusoidal frequency of 1.0 megahertz (MHz).

Notice 2 requires that the actual (not nominal) characteristic impedance must be within the above range (see 30.10.4).

4.5.1.3 Cable attenuation. At the frequency of 4.5.1.2, the cable power loss shall not exceed 1.5 decibels (dB)/100 feet (ft.).

A great deal of concern and confusion has resulted because of the cable network requirements including bus length, coupling, and stubbing. The standard chose not to specify a maximum main bus length because it is reasoned that cable length, number of terminals, and lengths of stubs are all subject to tradeoffs and must be considered in the design for reliable system operation. An arbitrary limit (such as the 300 ft specified in 1553A) should not be applied because all parameters of the network must be considered.

4.5.1.4 Cable termination. The two ends of the cable shall be terminated with a resistance, equal to the selected cable nominal characteristic impedance (Z_0) ±2.O percent.

4.5.1.5 Cable stub requrements. The cable shall be coupled to the terminal as shown on figure 9 or figure 10. Tie use of long stubs is discouraged, and the length of a stub should be minimized. However, if installation requirements dictate, stub lengths exceeding those lengths specified in 4.5.1.5.1 and 4.5.1.5.2 are permissible.

In the appendix, 10.5 also contains information on stubbing.

Notice 2, contains additional requirements for dual standby-redundant systems (see 30.10.5).

4.5.1.5.1 Transformer coupled stubs. The length of a transformer coupled stub should not exceed 20 feet. If a transformer coupled stub is used, then the following shall apply.

4.5.1.5.1.1 Coupling transformer. A coupling transformer, as shown on figure 9, shall be required. This transformer shall have a turns ratio of 1:1.41 ±3.O percent, with the higher turns on the isolation resistor side of the stub.

A generalized multiplex bus network configuration is shown in figure 1 of 1553B. The main bus is terminated at each end in the cable characteristic impedance to minimize reflections due to transmission line mismatch. With no stubs attached, the main bus looks like an infinite length transmission line and, so there are no disturbing reflections. When the stubs are added for connection of the terminals, the bus is loaded locally and a mismatch occurs with resulting reflections.

The degree of mismatch and signal distortion due to reflections area function of the impedance (Z) presented by the stub and terminal input impedance. To minimize signal distortion, it is desirable that the stub maintain a high impedance. This impedance is reflected back to the main bus. At the same time the impedance must be kept low so that adequate signal power will be delivered to the receiver input. Therefore, a tradeoff and compromise among these conflicting requirements is necessary to achieve the specified signal-to-noise ratio and system error rate performance.

Two methods for coupling a terminal to the main bus are defined in 1553B: transformer coupling and direct coupling. The two methods are shown in figures 9 and 10 of 1553B. Transformer coupling is usually used with long stubs (1 to 20 ft) and requires a coupler box, separate from the terminal, located near the junction of the main bus and stub. Direct coupling is usually limited for use with stubs of less than 1 ft. Fault isolation resistors (R) are included to provide protection for the main bus in case of a short circuit in the stub or terminal. The coupler transformer characteristics defined in 1553B area compromise between the signal level and distortion characteristics delivered to the terminals.

The coupler transformer turns ratio (1:1.41) provides impedance transformation for both terminal reception and transmission. The improvement of stub load impedance is a result of impedance transformation that is

proportional to the square of the turns ratio, assuming an ideal coupler transformer. The 1:1.41 transformer turns ratio also provides ideal termination of the stub for transmission of signals from the terminal to the main bus. The impedance at main bus is:

$$Z_B = \frac{Z_o}{2} + 2R \quad (1)$$

Where $R = 0.75Z_0$

$$Z_B = 0.5Z_o + 1.5Z_o = 2Z_o \text{ ohms} \quad (2)$$

The reflected impedance, Z_R, from the bus to the stub due to the transformer impedance transformation is:

$$Z_R = \frac{Z_B}{1.41^2} = \frac{2Z_o}{2} = Z_o \quad (3)$$

Therefore, the coupler transformer specified in 1553B provides the characteristics desired for reducing reflections and maintaining signal levels for systems where long stubs are required.

4.5.1.5.1.1.1 Transformer input impedence. The open circuit impedance as seen at point B on figure 11 shall be greater than 3000 ohms over the frequency range of 75.0 kilohertz (kHz) to 1.0 megahertz (MHz), when measured with a 1.0V root-mean-square (RMS) sin wave.

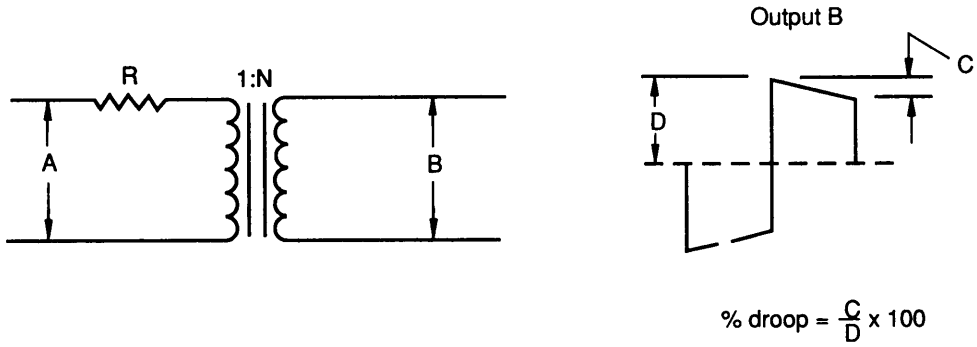


Figure 11 of 1553B. Coupling Transformer

The transformer open circuit impedance (Z_{oc}) is required to be greater than 3K ohms in 1553B systems. The measurement is made looking into the winding with the higher number of turns (1.41) with a 75-kHz to 1-MHz sine wave signal. The test amplitude at the transformer winding is adjusted to 1V rms. The critical factors in achieving the 3K ohm Z_{oc} is the distributed capacitance of the windings and the transformer primary inductance. The inductance of the transformer must be large enough to provide the open circuit impedance at 75 kHZ while the distributed capacitance should be small enough to maintain the open circuit impedance at the 1-MHZ test frequency. The inductance may obviously be increased by increasing the number of turns on the transformer. This technique, however, tends to increase the distributed capacitance, degrading high-frequency performance and therefore causing waveform integrity and common mode rejection to suffer.

The transformer is a very important element in determining the transceiver characteristics (e.g., input impedance, signal waveform integrity, and common mode rejection) required by 1553B. The considerations for transformer and associated input and output circuit design are:

a. Provide the specified input impedance at high frequencies (terminal input impedance 1000 ohms and 2000 ohms at 1 MHZ).

b. Maintain waveform integrity and low percentage droop for the lower frequency conditions (less than 20% for 250-kHz square wave).

c. Design for low interwinding capacitance to achieve common mode rejection (CMR)(45 dB CMR at ± 10V peak, dc to 2 MHz).

d. Maximize transformer leakage inductance. Because techniques to lower interwinding capacitance tend to increase leakage inductance, a tradeoff must be made to achieve good CMR performance while at the same time minimizing waveform tailoff distortion caused by leakage inductance.

These considerations are directly applicable to the design of the transceiver transformer. In addition to the transformer characteristics, other considerations for maintaining the terminal minimum input impedance specified in 1553B are as follows:

a. Minimize stray capacitance of wiring from the external connector and on the circuit card to the buffer amplifier (every 100 pF. results in approximately 1600 ohms shunt impedance).

b. Maintain high impedance at the receiver limiter and filter circuit inputs and transmitter driver outputs in the "of" state. These impedance must be maintained with the terminal (transceiver) power off.

4.5.1.5.1.1.2 Transformer waveform integrity. The droop of the transformer using the test configuration shown on figure 11 at point B, shall not exceed 20.0 percent. Overshoot and ringing as measured at point B shall be less that ±1.0 V peak. For this test, R shall equal 350.0 ohms 35.0 percent and the input A of figure 11 shall be a 250.0 kHz square wave. 27.0 V peak-to-peak, with a rise and fall time no greater than 100 nanoseconds (ns).

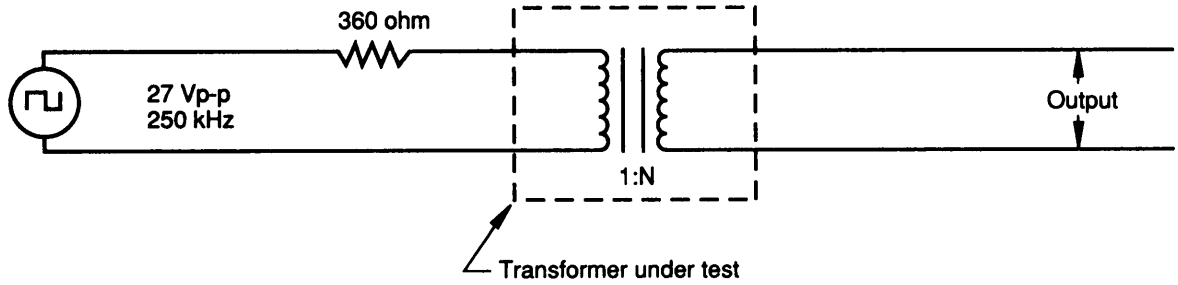
The ability of the coupler transformer to provide a satisfactory signal is specified in the droop, overshoot, and ringing requirements of 1553B shown in figure 20-8. Droop is specified at 20% maximum when driving the transformer with a 250-kHZ, 27V peak-to-peak (p-p) square wave. The test for the droop characteristic is made by driving the low-turns side winding through a 360-ohm resistor and measuring the signal at the open-circuited high-turns side winding. The droop of the transformer is determined mainly by the primary inductance. Because the primary inductance also provides the 3K-ohm open circuit impedance, the inductance should be made as high as possible without degrading the high-frequency performance of the transformer. Ringing and overshoot on the transformer signal is also shown in figure 20-8. The ±1V limit on these high-frequency perturbation can be achieved through careful attention to leakage inductance and transformer capacitance.

4.5.1.5.1.1.3 Transformer common mode rejection. The coupling transformer shall have a common mode rejection ratio greater than 45.0 dB at 1.0 MHz.

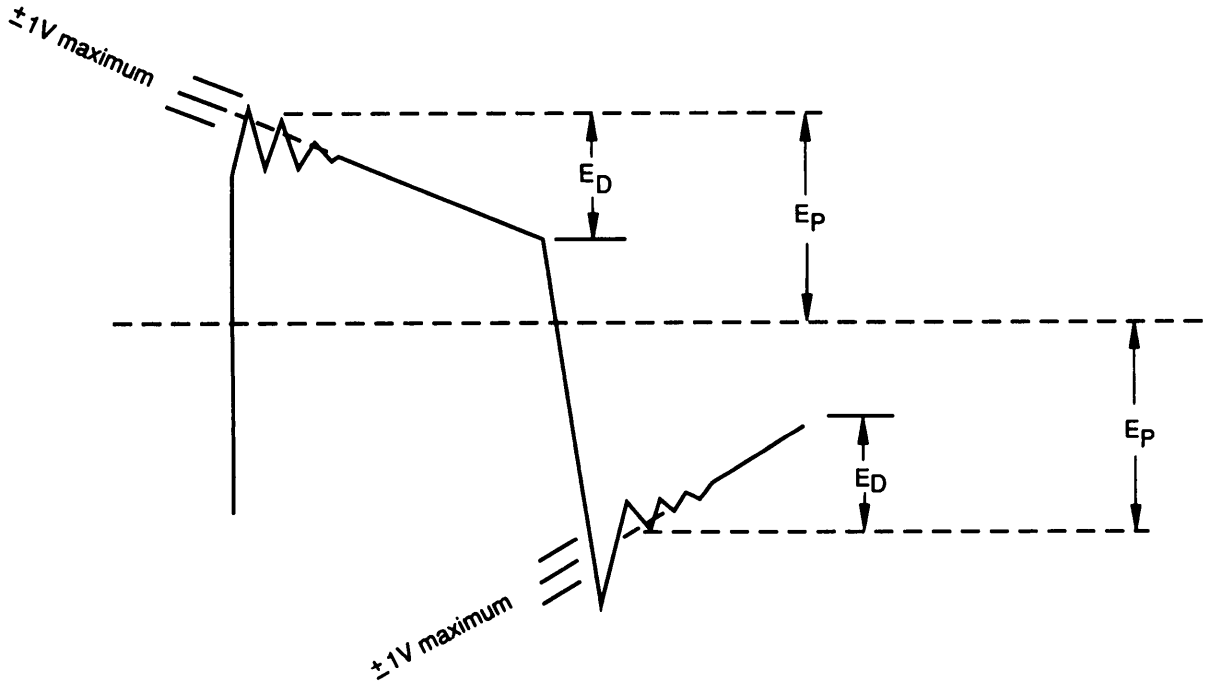
The common mode rejection of the isolation transformer is required to be greater than 45.0dB. The common mode test shown in figure 20-9 consists of driving the low-turns side winding while measuring the differential signal across the high-turns side. Common mode rejection can be improved by minimizing the interwinding capacitance and the core-to-winding capacitance. See section 40 for additional design considerations.

4.5.1.5.1.2 Fault isolation. An isolation resistor shall be placed in series with each connection to the data bus cable. This resistor shall have a value of 0.75 Z_o ohms plus or minus 2.0 percent, where 2_0 is the selected cable nominal characteristic impedance. The impedance placed across the data bus cable shall be no less than 1.5 Z_o ohms for any failure of the coupiing transformer, cable stub, or terminal transmitter/receiver.

4.5.1.5.1.3 Cable coupling. All coupling transformers and isolation resistors, as specified in 4.5.1.5.1.1 and 4.5.1.4.1.2, shall have continuous shielding which will provide a minimum of 75 percent coverage. The isolation resistors and coupling transformers shall be placed at minimum possible distance from the junction of the stub to the main bus.



N = turns ratio (1.41)



Output waveform

$$\% \text{ droop} = \frac{E_D}{E_P} \times 100$$

E_D: Voltage droop

E_P: Voltage peak

Figure 20-8. Waveform Test

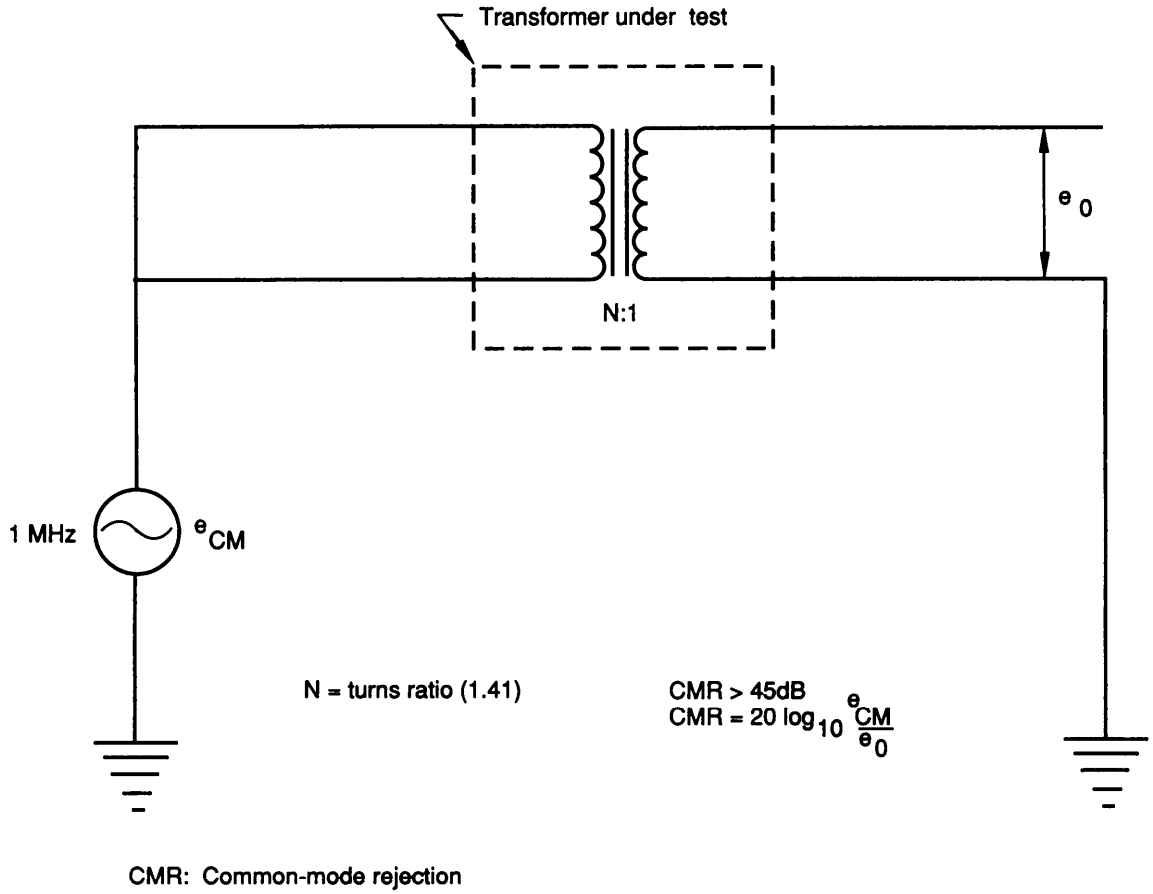


Figure 20-9. Common-Mode Test

4.5.1.5.1.4 Stub voltage requirements. Every data bus shall be designed such that all stubs at point A of figure 9 shall have a peak-to-peak ampiitude, line-to-line within the range of 1.0 and 14.0 V for a transmission by any terminal on the data bus. This shall include the maximum reduction of data bus signal amplitude in the event that one of the terminals has a fault which causes it to reflect a fault impedance specified in 4.5.1.5.1.2 on the data bus. This shall also include the worse case output voltage of the terminals as specified in 4.5.2.1.1.1 and 4.5.2.2.1.1.

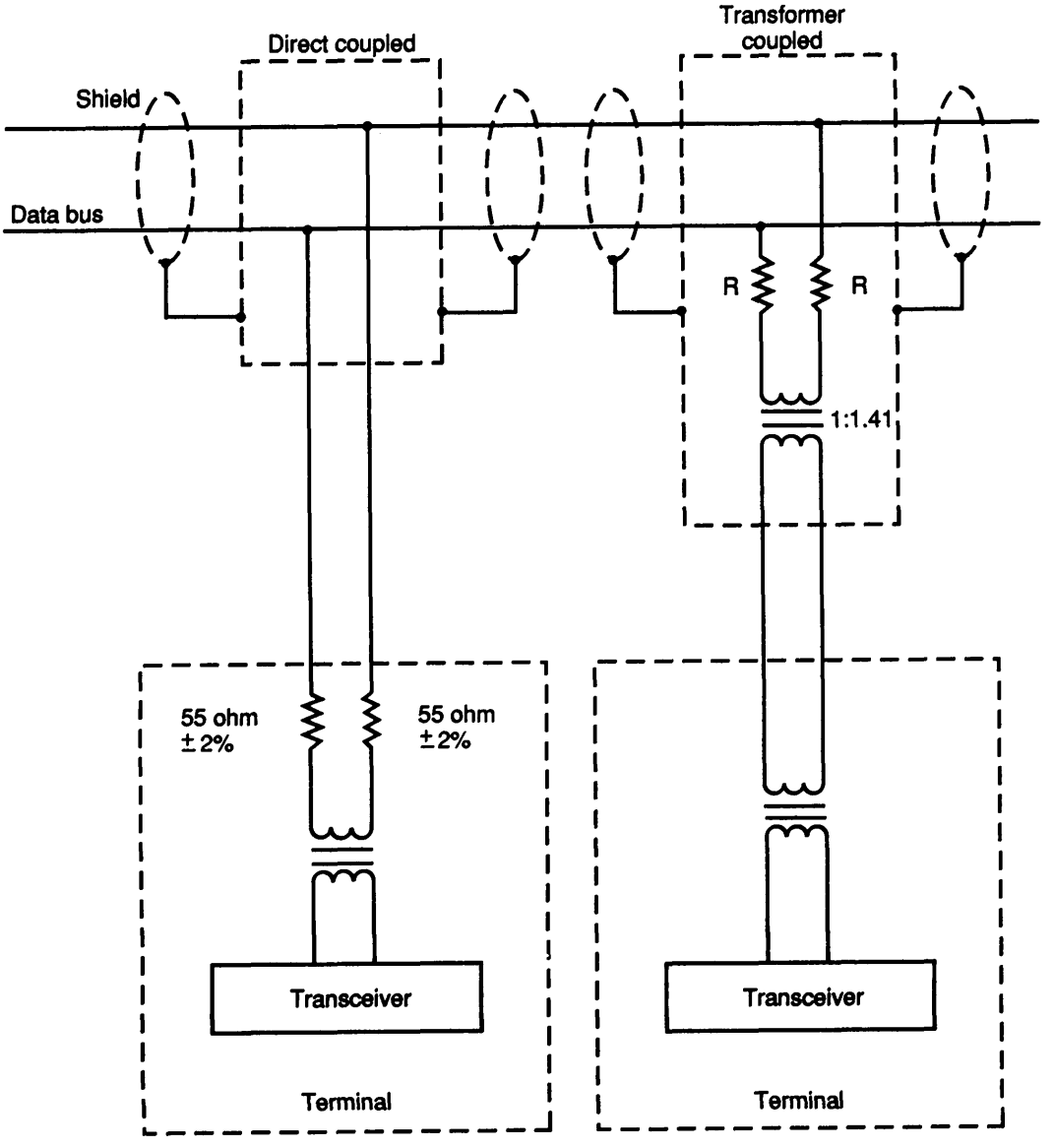
The transformer in the 1553B coupler has a turns ratio of 1:1.41 (see figure 20-10). This ratio, together with the 0.75Z fault isolation resistor provides the correct characteristic impedance for terminating the stub:

$$Z_{stub} = \left(\frac{1}{1.41}\right)^2 (0.75Z_o + 0.75Z_o + 0.5Z_0)$$

The stub capacitance is also effectively decreased by the square of the turns ratio to lessen the loading problem. The 1:1.41 ratio of 1553B is a compromise between stub matching and decreased stub loading. MIL-STD-1553B does not specify connector types.

Notice 2 (30.10.1 and 30.10.2) modify the coupling and shielding requirements.

4.5.1.5.2 Direct coupled stubs. The length of a direct coupled stub should not exceed 1 foot. Refer to 10.5 for comments concerning direct coupled stubs. If a direct coupled stub is used, then the following shall apply.



• Isolation resistors: R = 0.75 Z^*_O ±2%
• Isolation transformer: turns ratio 1:1.41 ±3%
(1-terminal winding)
(1.41-bus winding)

Z_{OC} > 3K-ohm at 75 kHz to 1 MHz
1V rms sine wave

Droop: < 20%
Overshoot/ringing: < +1V
CMR: > 45dB at 1 MHz
} at 27 Vp-p 250 kHz square wave

*Nominal characteristic impedance of bus cable: Z = 70 ohm to 85 ohm at 1 MHz

CMR: Common mode rejection

Figure 20-10. Coupler Characteristics

4.5.1.5.2.1 Fault isolation. An isolation resistor shall be placed in series with each connection to the data bus cable. This resistor shall have a value of 55.0 ohms plus or minus 2.0 percent. The isolation resistors shall be placed within the RT as shown on figure 10.

4.5.1.5.2.2 Cable coupling. All bus-stub junctions shall have continuous shielding which will provide a minimum of 75 percent coverage.

4.5.1.5.2.3 Stub voltage requirements. Every data bus shall be designed such that all stubs at point A of figure 10 shall have a peak-to-peak amplitude, line-to-line within the range of 1.4 and 20.0 V for a transmission by any terminal on the data bus. This shall include the maximum reduction of data bus signal amplitude in the event that one of the terminals has a fault which causes it to reflect a fault impedance of 110 ohms on the data bus. This shall also include the worst case output voltage of the terminals as specified in 4.5.2.1.1.1 and 4.5.2.2.1.1.

4.5.1.5.3 Wiring and cabling for EMC. For purposes of electromagnetic capability (EMC), the wiring and cabling provisions of MIL-E-6051 shall apply.

The coupling network provides bus connections for the transformer-coupled (external coupler) and direct-coupled cases. Isolation resistors of 55 ohms value are included for the direct-coupled connection, and the proper transformer turns ratio is provided when the appropriate bus connection is selected. The turns ratio is different for the transformer-coupled and direct-coupled connections to compensate for the 1.41:1 reduction of signal level in the external coupler. This feature allows a threshold setting that is the same for both bus connections.

Notice 2 (30.10.1 and 30.10.2) modifies the coupling requirement.

4.5.2 Terminal characteristics.

Figures 20-11 and -12 show the interface diagrams and the points where the signal measurement is defined in 1553B. The following discussion will relate some of the rationale for this approach to development of the requirements in 1553B.

4.5.2.1 Terminals with transformer coupled stubs.

4.5.2.1.1 Terminal output characteristics. The following characteristics shall be measured with RL, as shown on figure 12, equal to 70.0 ohms ±2.O percent.

4.5.2.1.1.1 Output levels. The terminal output voltage levels shall be measured using the test configuration shown on figure 12. The terminal output voltage shall be within the range of 18.0 to 27.0 V, peak-to-peak, line-to-line, when measured at point A on figure 12.

The approach taken for 1553B is to specify the terminal output for the two conditions: transformer coupled and direct coupled. This may require that each terminal have two sets of input and output pins for each bus cable connection. Therefore, the 18V to 27V p-p transmitter output applied to the stub and coupler results in a nominal 6V to 9V p-p signal level at the stub-to-bus connection (point B). This range is equivalent to that specified for the direct-coupled case shown in figure 20-12. Test configurations are provided for both direct-coupled and transformer-coupled cases in figure 20-13. See section 50 of this handbook for further discussion.

4.5.2.1.1.2 Output levels. The waveform, when measured at point A on figure 12 shall have zero crossing deviations which are equal to, or less than, 25.0 ns from the ideal crossing point, measured with respect to the previous zero crossing (i.e., .5 ± .025 μs, 1.0 ± .025 μs, 1.5 ± .025 μs, and 2.0 ± .025 μs). The rise and fall time of this waveform shall be from 100.0 to 300.0 ns when measured from levels of 10 to 90 percent of full waveform peak-to-peak, line-to-line,

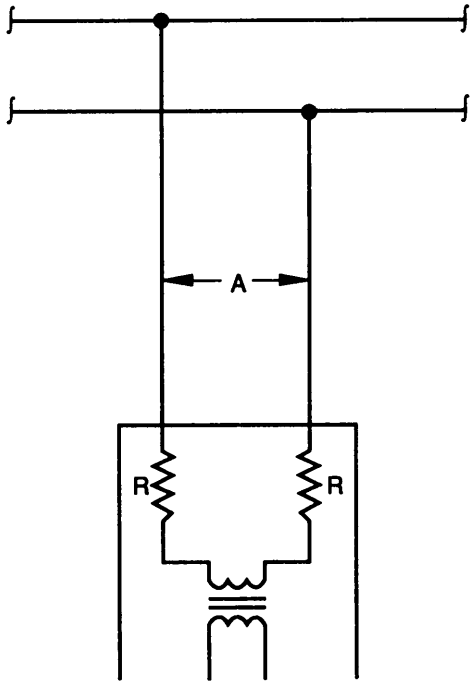
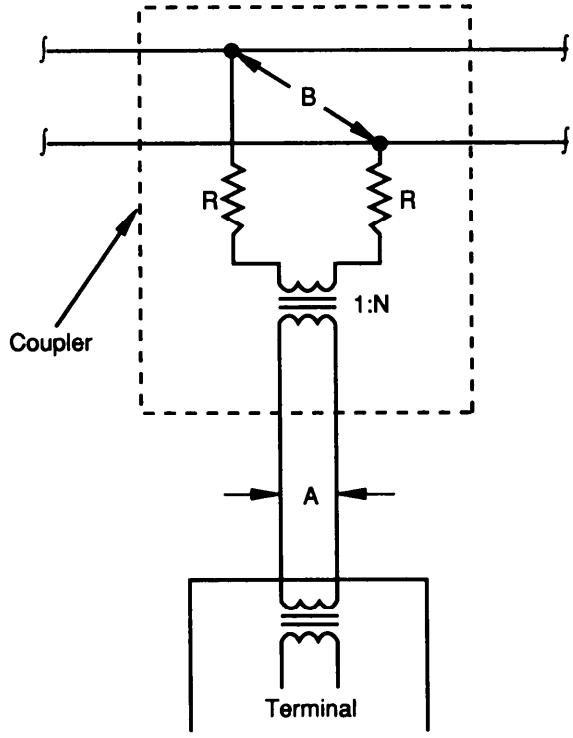


Figure 20-11. Direct-Coupled (Short Stub) MIL-STD-1553B Data Bus Interface



R: Isolation resistor
1:N: Transformer turns ratio

Figure 20-12. Transformer-Coupled (Long Stub) MIL-STD- 1553B Data Bus Inteface

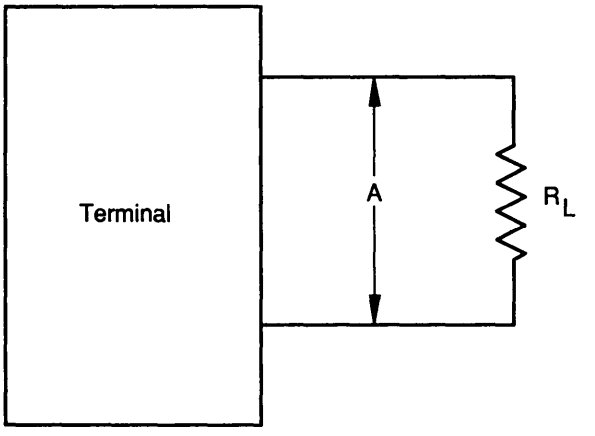


Figure 12 of 1553B. Terminal I/O Characteristics for Transformer-Coupled and Direct Coupled Stubs

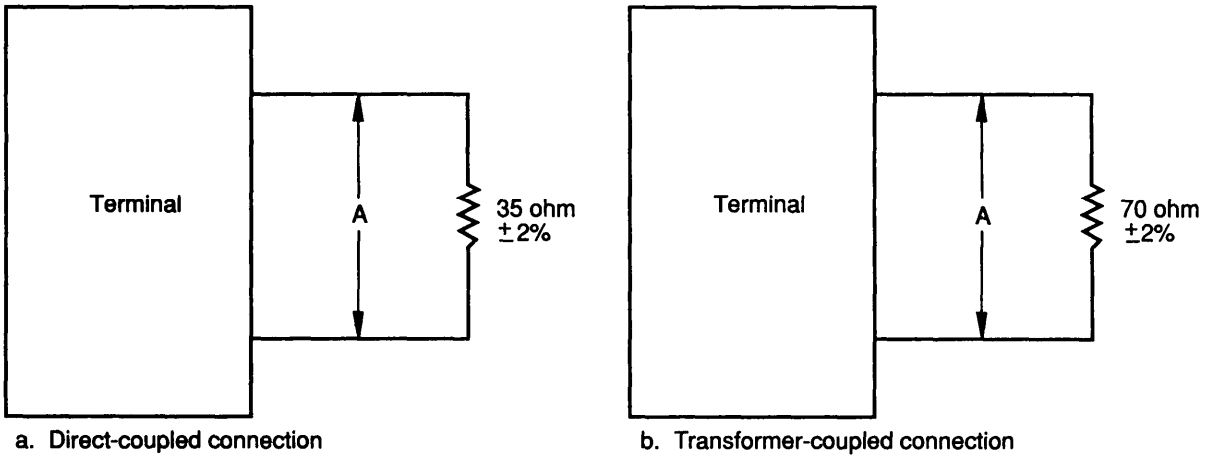


Figure 20-13. Direct-Coupled and Transformer-Coupled Terminal Output Test Configuration

voltage as shown on figure 13. Any distortion of the waveform including overshoot and ringing shall not exceed ± 900.0 millivolts (mV) peak, line-to-line, as measured at point A, figure 12.

The waveform characteristics provide control of the zero-crossing deviations for all possible conditions and establish a limit on distortion. See also section 40 of this handbook.

4.5.2.1.1.3 Output noise. Any noise transmitted when the terminal is receiving or has power removed, shall not exceed a value of 14.0 mV, RMS, line-to-line, as measured at point A, figure 12.

The output rms noise for the transformer-coupled and direct-coupled cases are specified in 1553B (4.5.2.1.1.3 and 4.5.2.2.1.3) and are consistent with the required system performance and practical terminal hardware design. The requirement for low output noise of 14 mV rms, and 5 mV rms when not transmitting, also places

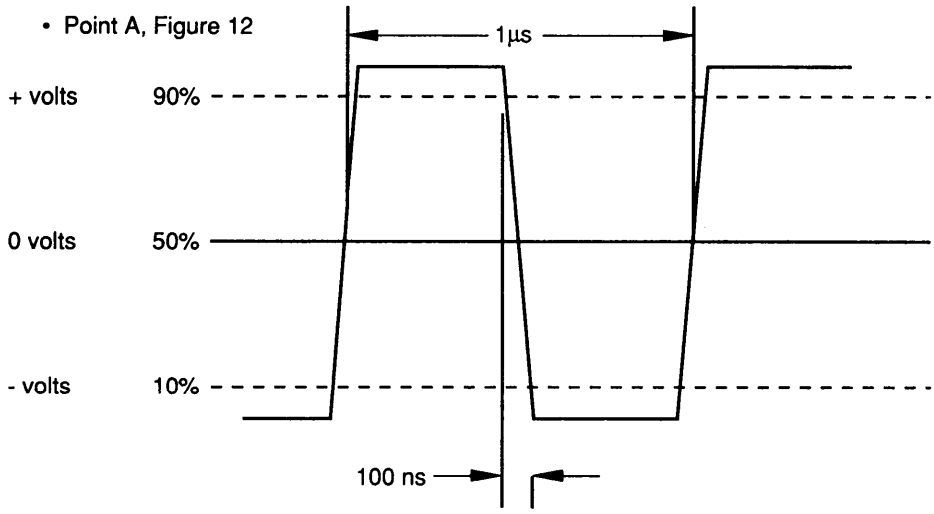


Figure 13 of 1553B. Output Waveform

significant constraints on the length and routing of input and output wiring due to the induced power supply and logic noise generated in the terminal.

4.5.2.1.1.4 Ouput symmetry. From the time beginning 2.5 μs after the mid-bit crossing of the parity bit of the last word transmitted by a terminal, the maximum voltage at point A of figure 12 shall be no greater than ±250.0 mV peak, line-to-line. This shall be tested with the terminal transmitting the maximum number of words it is designed to transmit, up to 33. This test shall be run six times with each word in a contiguous block of words having the same bit pattern. The six word contents that shall be used are 8000_{16}, $7FFF_{16}$, $OOOO_{16}$, $FFFF_{16}$ 5555_{16} and $AAAA_{16}$. The output of the terminal shall be as specified in 4.5.2.1.1.1 and 4.5.2.1.1.2.

An ideal waveform is perfectly balanced so that the signal energy on both sides of the zero (off) level is identical. If the positive or negative energy is not equal, problems can develop in the coupling transformers, and the transmission line can acquire a charge that appears as a tail with overshoot and ringing when transmission is terminated. These considerations require that the symmetry of the transmitted waveform be controlled within practical limits. This is accomplished by specifying the signal level from a time beginning 2.5 us after the midbit zero crossing of the parity bit of the last word in a message transmitted by the terminal under test. The test messages contain the maximum number of words and defined bit patterns.

4.5.2.1.2 Terminal input characteristics. The following characteristics shall be measured independently.

4.5.2.1.2.1 Input waveform compatibility. The terminal shall be capable of receiving and operating with the incoming signals specified herein, and shall accept waveform varying from a square wave to a sine wave with a maximum zero crossing deviation from the ideal with respect to the previous zero crossing of ±150 ns, (i.e., 2.0 ± .15 μs, 1.5 ± .15 μs, 1.0 ± .15 μs, .5 ± .1 5μs). The terminal shall respond to an input signal whose peak-to-peak amplitude, line-to-line, Is within the range of .86 to 14.0 V. The terminal shall not respond to an input signal whose peak-to-peak amplitude, line-to-line, is within the range of 0.0 to .20 V. The voltages are measured at point A on figure 9.

4.5.2.1.2.2 Common mode rejections. Any signals from direct current (DC) to 2.0 MHz, with amplitudes equal to or less than ± 10.0 V peak, line-to-ground, measured at point A on figure 9, shall not degrade the performance of the receiver.

The input voltage specifications reflect the output voltage ranges for the transformer-coupled and direct-coupled connections to the terminal. Terminal required-response and no-response signal levels are specified so that the optimum threshold levels may be selected. It should be noted that the threshold setting has a significant effect on the noise rejection and error rate performance of the receiver. The threshoid setting is above the maximum no-response voltage level and below the minimum response level. Allowing a margin between the specification no-response level and the actual no-response level will improve the noise-rejection performance.

4.5.2.1.2.3 Input impedence. The magnitude of the terminal Input Impedance, when the RT is not transmitting, or has power removed, shall be a minimum of 1000.0 ohms within the frequency range of 75.0 kHz to 1.0 MHz. This impedance is that measured line-to-line at point A on figure 9.

As indicated in the data bus network requirement, input impedance is required to be maintained at a reasonable level to reduce the signal distortion effects when terminals are connected to the bus. Terminal input impedance is determined primarily by the following:

a. **Transformer Impedance-** Maintain inductance required to support low-frequency component of signal while controlling interwinding capacitance for high frequencies.

b. **Terminal wiring capacitance-** Control stray capacitance of wiring from terminal connector to receiver.

c. **Secondary Impedance transformatlon—** For the transformer-coupled case, a transformer with a turns ratio of 1:1.41 is implied. The impedance at the secondary is reflected to the terminal input, reduced by a factor of 2.

The factor of 2 difference in the impedance specified for the transformer-coupled and direct-coupied cases is based primarily on the effect of item c above.

4.5.2.1.2.4 Noise rejection. The terminal shall exhlblt a maximum word error rate of one part In 10^{7}, on all words received by the terminal, after validation checks as specified in 4.4, when operating in the presence of additive white Gaussian noise distributed over a bandwidth of 1.0 kHz to 4.0 MHz at an RMS amplltude of 140 mV. A word error shall include any fault which causes the message error blt to be set in the terminal's status word, or one which causes a terminal to not respond to a valid command. The word error rate shall be measured with a 2.1 V peak-to-peak, line-to-line, Input to the terminal as measured at point A on figure 9. The noise tests shall be run continuously until, for a particular number of failures, the number of words received by the terminal, including both command and data words, exceeds the required number for acceptance of the terminal, or Is less than the required number for rejection of the terminal, as specified in table II. All data words used In the tests shall contain random bit patterns. These bit patterns shall be unique for each data word in a message, and shall change randomly from message to message.

The test conditions of signal and noise specified were selected to produce a corresponding value of word error ratio (WER) that is sufficiently high (10^{-7}) to permit performance verification of a terminal receiver within a reasonable test period. The noise rejection is a figure-of-merit test and can be performed in a normal laboratory environment with a typical test setup as shown in figure 20-14. The verification of detector performance should consider the measurement of both detected and undetected errors.

Externally generated noise can take on many forms with a wide variety of power and frequencies. It is recognized that impulse noise having either random or periodic impulse duration, frequency of occurrence, and burst interval are more typical of noise sources that have major impact on digital data systems. Relay switching is generally regarded as the most severe source of impulse noise. This type of noise defies accepted forms of analysis, such as that performed using an additive white Gaussian (AWG) noise model. Because

Table II of 1553B. Criteria for Acceptance or Rejection of a Terminal for the Noise-Rejection Test

Total words received by terminal (in multiples of 10^7)

No. of errors	Reject (equal or less)	Accept (equal or more)
0	N/A	4.40
1	N/A	5.21
2	N/A	6.02
3	N/A	6.83
4	N/A	7.64
5	N/A	8.45
6	.45	9.27
7	1.26	10.08
8	2.07	10.89
9	2.88	11.70
10	3.69	12.51
11	4.50	13.32
12	5.31	14.13
13	6.12	14.94
14	6.93	15.75
15	7.74	16.56
16	8.55	17.37
17	9.37	18.19
18	10.18	19.00
19	10.99	19.81
20	11.80	20.62
21	12.61	21.43
22	13.42	22.24
23	14.23	23.05
24	15.04	23.86
25	15.85	24.67
26	16.66	25.48
27	17.47	26.29
28	18.29	27.11
29	19.10	27.92
30	19.90	28.73
31	20.72	29.54
32	21.53	30.35
33	22.34	31.16
34	23.15	31.97
35	23.96	32.78
36	24.77	33.00
37	25.58	33.00
38	26.39	33.00
39	27.21	33.00
40	28.02	33.00
41	33.00	N/A

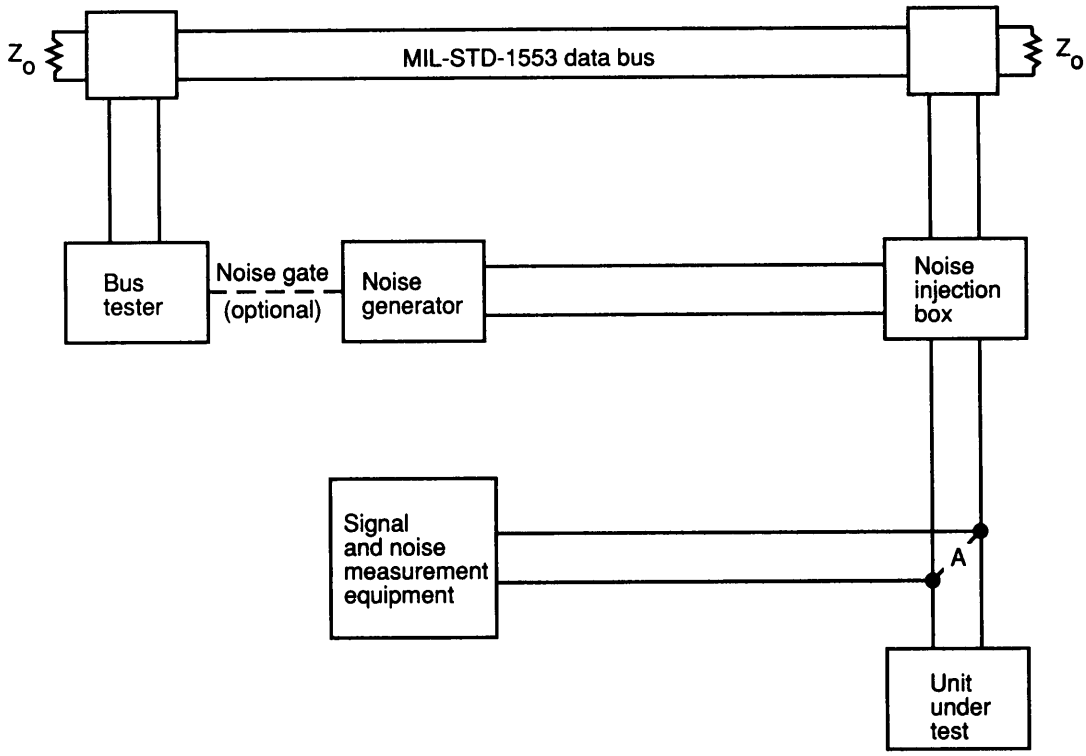


Figure 20-14. Configuration for Noise-Rejection Test

of the difficulty of error performance analysis using the impulsive noise model, a worstcase Gaussian model has been formulated. This model offers an analysis and test tool for evaluating terminal receiver performance considering the effects of impulsive noise. This approach is reflected in the noise rejection test conditions and word error rate versus signal-to-noise ratio (SNR) performance requirements of 1553B (4.5.2.1.2.4 and 4.5.2.2.2.4).

4.5.2.2 Terminals with direct coupled stub.

4.5.2.2.1 Terminal output characteristics. The following characteristics shall be measured with RL, as shown on figure 12, equai to 35.0 ohms ± 2.0 percent.

4.5.2.2.1.1 Output levels. The terminal output voltage levels shall be measured using the test configuration shown on figure 12. The terminal output voltage shall be within the range of 6.0 to 9.0 V, peak-to-peak, line-to-line, when measured at point A on figure 12.

4.5.2.2.1.2 Output waveform. The waveform, when measured at point Aonfigure 12, shall have zero crossing deviations which are equal to, or less than, 25.0 ns from the ideal crossing point, measured with respect to the previous zero crossing (i.e., .5 ± .025 µs, 1.0 ± .025 µs, 1.5 ± .025 µs and 2.0 ± .025 µs). The rise and fail time of this waveform shall be from 100.0 to 300.0 ns when measured from ieveis of 10 to 90 percent of full waveform peak-to-peak, line-to-line, voltage as shown on figure 13. Any distortion of the waveform including overshoot and ringing shall not exceed ± 300.0 mV peak, line-to-line, as measured at point A on figure 12.

4.5.2.2.1.3 Output noise. Any noise transmitted when the terminal is receiving or has power removed, shall not exceed a value of 5.0 mV, RMS, line-to-line, as measured at point A on figure 12.

4.5.2.2.1.4 Output symmetry. From the time beginning 2.5 μs after the mid-bit crossing of the parity bit of the last word transmitted by a terminal, the maximum voltage at point A on figure 12, shall be no greater than ± 90.0 mV peak, line-to-line. This shall be tested with the terminal transmitting the maximum number of words is is designed to transmit, up to 33. This test shall be run six times with each word In a contiguous block of words having the same bit pattern. The six word contents that shall be used are 8000_{16}, $7FFF_{16}$, 0000_{16} $FFFF_{16}$ 5555_{16} and $AAAA_{16}$. The output of the terminal shall be as specified In 4.5.2.2.1.1 and 4.5.2.2.1.2.

4.5.2.2.2 Terminal input characteristics. The following characteristics shall be measured independently.

4.5.2.2.2.1 Input waveform compatibility. The terminal shall be capable of receiving and operating with the incoming signals specified herein, and shall accept waveform varying from a square wave to a sine wave with a maximum zero crossing deviation from the ideal with respect to the previous zero crossing of plus or minus 150 ns, (i.e., 2.0 ±.15 μs 1.5 ±.15 μs, 1.0 ± .15 μs .5 ± .15 μs). The terminal shall respond to an input signal whose peak-to-peak amplitude, line-to-line, is within the range of 1.2 to 20.0 V. The terminal shall not respond to an input signal whose peak-to-peak amplitude, line-to-line, is within the range of 0.0 to .28 V. The voltages are measured at point A on figure 10.

4.5.2.2.2.2 Common mode rejections. Any signals from DC to 2.0 MHz, with amplitudes equal to or less than ± 10.0 volts peak, line-to-ground, measured at point A on figure 10, shall not degrade the performance of the receiver.

4.5.2.2.2.3 Input impedance. The magnitude of the terminal input impedance, when the RT is not transmitting, or has power removed, shall be a minimum of 2000.0 ohms within the frequency range of 75.0 kHz to 1.0 MHz. This impedance is that measured line-to-line at point A on figure 10.

4.2.2.2.4 Noise rejection. The terminal shall exhibit a maximum word error rate of one part in 10^7, on all words received by the terminal, after validation checks as specified in 4.4, when operating in the presence of additive white Gaussian noise distributed over a bandwidth of 1.0 kHz to 4.0 MHz at an RMS amplitude of 200 mV. A word error shall include any fault which causes the message error bit to be set in the terminal's status word, or one which causes a terminal to not respond to a valid command. The word error rate shall be measured with a 3.0 V peak-to-peak, line-to-line, input to the terminal as measured at point A on figure 10. The noise tests shall be run continuously until, for a particular number of failures, the number of words received by the terminal, including both command and data words exceeds the required number for acceptance of the terminal, or is less than the required number for rejection of the terminal, as specified in table ll. All data words used in the tests shall contain random bit patterns. These bit patterns shall be unique for each data word in a message, and shall change randomly from message to message.

4.6 Redundant data bus requirements. If redundant data buses are used, the requirements as specified in the foiiowing shall apply to those data buses.

4.6.1 Electrical isolation. All terminals shall have a minimum of 45 dB isolation between data buses. Isolation here means the ratio in dB between the output voltage on the active data bus and the output voltage on the Inactive data bus. This shall be measured using the test configuration specified In 4.5.2.1.1 or 4.5.2.2.1 for each data bus. Each data bus shall be alternately activated with all measurements being taken at point A on figure 12 for each data bus.

4.6.2 Single event failures. All data buses shall be routed to minimize the possibility that a single event failure to a data bus shall cause the loss of more than that particular data bus.

4.6.3. Dual standby redundant data bus. If a dual redundant data bus Is used, then it shall be a dual standby redundant data bus as specified in the following paragraphs.

4.6.3.1 Data bus activity. Only one data bus can be active at any given time except as specified in 4.6.3.2.

4.6.3.2 Reset data bus transmitter. If while operating on a command, a terminal receives another valid command, from either data bus, it shall reset and respond to the new command on the data bus on which the new command is received. The terminal shall respond to the new command as specified in 4.3.3.8.

The redundant data bus requirements reflect the common practice for use of the dual bus in which one is active and the other is on standby, and it was the intent to restrict the operation of a dual data bus connected to terminals to a one-at-a-time operation. However, provision had to be made for a BC to override one bus to respond on the redundant bus. The requirement for this is in 4.6.3.2, and the reference to 4.3.3.8 is the response time requirement of a RT to a valid command word. See also Notice 2 pen-and-ink changes discussed in 20.2.

APPENDIX

10. General. The following paragraphs in this appendix are presented in order to discuss certain aspects of the standard in a general sense. They are intended to provide a user of the standard more insight into the aspects discussed.

10.1 Redundancy. It is intended that this standard be used to support rather than to supplant the system design process. However, it has been found, through application experience in various aircraft, that the use of a dual standby redundancy technique is very desirable for use in integrating mission avionics. For this reason, this redundancy scheme is defined in 4.6 of this standard. None the less, the system designer should utilize this standard as the needs of a particular application dictate. The use of redundancy, the degree to which it is implemented, and the form which it takes must be determined on an individual application basis. Figures 10.1 and 10.2 illustrate some possible approaches to dual redundancy. These illustrations are not intended to be inclusive, but rather representative. It should be noted that analogous approaches exist for the triple and quad redundant cases.

10.2 Bus controller. The bus controller is a key part of the data bus system. The functions of the bus controller, in addition to the issuance of commands, must include the constant monitoring of the data bus and the traffic on the bus. It is envisioned that most of the routine minute details of bus monitoring (e.g., parity checking, terminal non-response time-out, etc.) will be embodied in hardware, while the algorithms for bus control and decision making will reside in software. It is also envisioned that, in general, the bus controller will be a general purpose airborne computer with a special input/output (I/O) to interface with the data bus. It is of extreme importance in bus controller design that the bus controller be readily able to accommodate terminals of differing protocol's and status word bits used. Equipment designed to MIL-STD-1553A will be in use for a considerable period of time; thus, bus controllers must be capable of adjusting to their differing needs. It is also important to remember that the bus controller will be the focal point for modification and growth within the multiplex system, and thus the software must be written in such a manner as to permit modification with relative ease.

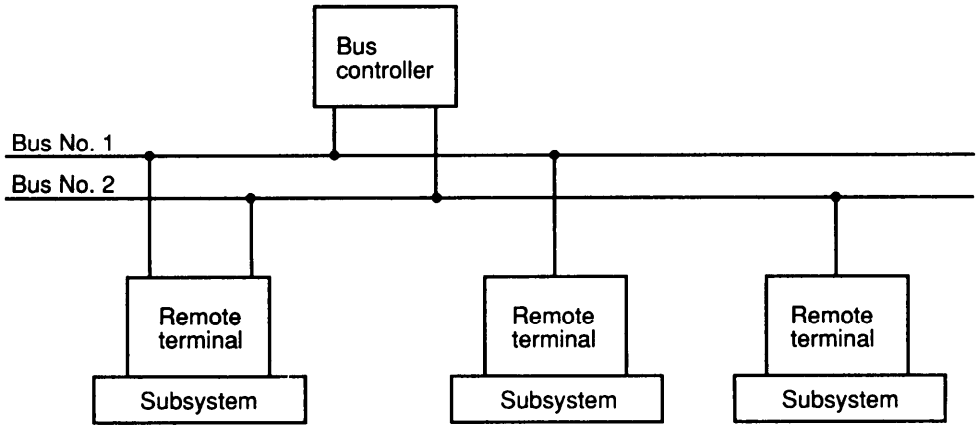
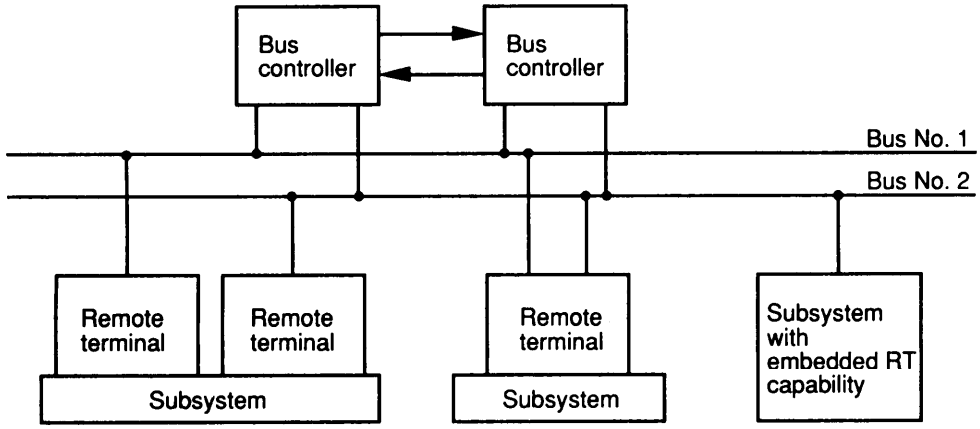


Figure 10.1 of 1553B. Illustration of Possible Redundancy



Note: RT - Remote Terminal

Figure 10.2 of 1553B Illustration of Possible Redundancy

10.3 Multiplex selection criteria. The selection of candidate signals for multiplexing is a function of the particular application involved, and criteria will in general vary from system to system. Obviously, those signals which have bandwidths of 400 Hz or less are prime candidates for inclusion of the bus. It is also obvious that video, audio, and high speed parallel digital signals should be excluded. The area of questionable application is usually between 400 Hz and 3khz bandwidth. The transfer of these signals on the data bus will depend heavily upon the loading of the bus in a particular application. The decision must be based on projected future bus needs as well as the current loading. Another class of signals which in general are not suitable for multiplexing are those which can be typified by a low rate (over a mission) but possessing a high priority or urgency. Examples of such signals might be a nuclear event detector output or a missile launch alarm from a warning receiver. Such signals are usually better left hardwired, but they maybe accommodated by the multiplex system if a direct connection to the bus controller's interrupt hardware is used to trigger a software action in response to the signal.

10.4 High reliability requirements. The use of simple parity for error detection within the multiplex bus system was dictated by a compromise between the need for reliable data transmission, system overhead, and remote terminal simplicity. Theoretical and empirical evidence indicates that an undetected bit error rate of 10^{-12} can be expected from a practical muitiplex system built to this standard. If a particular signal requires a bit error rate which is better than that provided by the parity checking, then it is incumbent upon the system designer to provide the reliability within the constraints of the standard or to not include this signal within the muitiplex bus system. A possible approach in this case would be to have the signal source and sink provide appropriate error detection and correction encoding/decoding and employ extra data words to transfer the information. Another approach wouid be to partition the message, transmit a portion at a time, and then verify (by interrogation) the proper transfer of each segment.

10.5 Stubbing. Stubbing is the method wherein a separate line is connected between the primary data bus line and a terminal. The direct connection of a stub line causes a mismatch which appears on the waveforms. This mismatch can be reduced by filtering at the receiver and by using hi-phase modulation. Stubs are often employed not only as a convenience in bus layout but as a means of coupiing a unit to the line in such a manner that a fault on the stub or terminal will not greatly affect the transmission line operation. In this case, a network is employed in the stub line to provide isolation from the fault. These networks are also used for stubs that are of such length that the mismatch and refiection degrades bus operation. The preferred method of stubbing is to use transformer coupled stubs, as defined in 4.5.1.5.1. This method provides the benefits of DC isolation, increased common mode protection, a doubling of effective stub impedance, and fault isolation for the entire stub and terminal. Direct coupled stubs, as defined in 4.5.1.5.2 of this standard, should be avoided if at all possible. Direct coupled stubs provide no DC isolation or common mode rejection for the terminal external to its subsystem. Further, any shorting fault between the subsystems internal isolation resistors (usually on a circuit board) and the main bus junction will cause failure of that entire bus. It can be expected that when the direct coupled stub length exceeds 1.6 feet, that it will begin to distort the main bus waveforms. Note that this length includes the cable runs internal to a given subsystem.

10.6 Use of broadcast option. The use or a broadcast message as defined in 4.3.3.6.7 of this standard represents a significant departure from the basic philosophy of this standard in that it is a message format which does not provide positive closed-loop control of bus traffic. The system designer is strongly encouraged to solve any design problems through the use of the three basic message formats without resorting to use of the broadcast. If system designers do choose to use the broadcast command, they should carefully consider the potential effects of a missed broadcast message, and the subsequent implications for fault or error recovery design in the remote terminals and bus controllers.

Notice 2 adds a paragraph (10.7) that references related documents.

20.2 COMMENTARY ON NOTICE 2 OF MIL- STD-1553B.

The purpose of Notice 2 to MIL-STD-1553B (referred to as 1553B) was to:

a. Clarify interpretable areas of 1553B.

b. Unify tri-service requirements.

c. Resolve recurring implementation problems at the line replaceable unit (LRU) and system levels.

d. Determine testability.

Notice 2 was the result of compromises as to what level of detail it should include, what should be put in a separate specification, or what should be included in MIL-HDBK-1553. It addresses problems that continue to recur during system integration and testing. It also addresses the need for an increased level of interoperability brought about by the increasing use of Government-furnished equipment (GFE) on a variety of aircraft across the triservices.

Notice 2 was written in two parts:

a. A list of editorial changes, such as deleting words like “aircraft” and “internal,” to increase the applicability of the standard (i.e., shipboard and combat vehicle applications also use 1553B); a change of the title of the bus switching paragraph (4.6.3.2) because the original title had been causing confusion (see 20.2.1).

b. Changes for dual standby-redundant applications of 1553B, based on the knowledge and experience gained since the release of 1553B in 1978, and reflecting good system engineering design practices that may be applied to applications other than dual standby-redundant buses (see 20.2.2).

20.2.1 Commentary on Notice 2 pen-and-ink changes

Page i

Delete title and substitute: DIGITAL TIME DIVISION COMMAND/RESPONSE MULTIPLEX DATA BUS”.

Page ii

Delete title and substitute: “Digital Time Division Command/Response Multipiex Data Bus”.

Page 1

Paragraph 1.1, second line: Delete “on aircraft”.

Paragraph 1.2, third line: Delete “an aircraft” and substitute “a”.

The intent of these changes was to increase the applicability of MIL-STD-1553 to applications other than aircraft.

Page 3

Paragraph 3.11, first line, after “Bus controller”: Insert “(BC)”.

Paragraph 3.12, first line, after “Bus monitor”: Insert “(BM)”.

This is an editorial change to ensure that the acronyms were defined at the beginning of the standard.

Page 21

Paragraph 4.4.3.1, add: “No combination of RT address bits T/R bit, subaddress/mode bits, and data word count/mode code bits of a command word shall result in invalid transmissions by the RT. Subsequent valid commands shall be properly responded to by the RT.

Not all RTs have the capability of monitoring for illegal commands, an option specified in paragraph 4.4.3.4 of MIL-STD-1553. This addition to paragraph 4.4.3.1 provides designers with a specific requirement

governing the RT response to the receipt of an undetected illegal command or a command addressed to another RT, events that have caused RTs to fail and/or transmit invalid data on the bus. Additionally, it requires that the RT be able to recover from the receipt of either type of command and respond properly to subsequent valid commands.

Page 30

Paragraph 4.6.3.2, first line: Delete "Reset data bus transmitter's and substitute "Superseding valid commands".

Paragraph 4.6.3.2, second line: Delete "from either data bus" and substitute 'from the other data bus".

The original intent of this paragraph was to specify the response, for an RT connected to a dual standby-redundant data bus, when the RT received a valid command while simultaneously processing a valid command received from the other data bus. The intent here is to clarify the wording, particularly in the paragraph title.

Page 31

Paragraph 10.2, eighth line: Delete "airborne".

The intent of this change was to increase the applicability of MIL-STD-1553 to applications other than aircraft.

2.0.2.2 Commentary on Notice 2 text revisions.

DIGITAL TIME DIVISION COMMAND/RESPONSE MULTIPLEX DATA BUS

Notice 2 changed the title of MIL-STD-1553B by deleting the reference to aircraft. This increases its applicability to uses other than aircraft.

FOREWORD

This standard contains requirements for a digital time division command/response multiplex data bus for use in systems integration. Even with the use of this standard, differences may exist between muitipiex data buses in different system applications due to particular appiication requirements and the designer options allowed in this standard. The system designer must recognize this fact and design the multiplex bus controller hardware and software to accommodate such differences. These designer selected options must exist to allow the necessary flexibility in the design of specific multiplex systems in order to provide for the control mechanism, architectural redundancy, degradation concept and traffic patterns peculiar to the specific application requirements. Appendix, Section 30 selects those options which shall be required and further restricts certain portions of the standard for the use in all dual standby redundant applications for the Army, Navy, and Air Force.

The foreword was updated to reflect deletion of the references to aircraft and aircraft systems in the standard and to define the scope of new section 30.

10.7 Other related documents. Several documents exist which are related to this standard. MIL-HDBK-1553 describes implementation practices for this standard and other related data. This standard is embodied in or referenced by the following international documents: NATO STANAG 3838, ASCC Air Standard 50/2, and UK DEF STAN 00-18 (PART 2)/Issue 1.

20. REFERENCED DOCUMENTS.

Not applicable.

In Notice 1 to MIL-STD-1553B (referred to as 1553B), section 20, General, the intent was to "select those options which shall be required and to further restrict certain portions of the standard for use in Air Force avionics." Notice 2 supersedes Notice 1 as of the date of issue.

30. GENERAL REQUIREMENTS.

30.1 Option selection. This section of the appendix shall select those options required to further define portions of the standard to enhance tri-service interoperability. References in parentheses are to paragraphs in standard which are affected.

The necessity for an increased emphasis on triservices standardization of 1553B interfaces became evident as more and more subsystems began to be used across triservices applications as the basic input and output communications interface. Without coordination of these interfaces, subsystems developed by one service were incompatible with those developed by another service. The intent of this section of the standard, in general, is to specify the minimum set of 1553B options required by the Army, Navy, and Air Force.

30.2 Appplication. Section 30 of this appendix shall apply to all dual standby redundant applications for the Army, Navy, and Air Force. All Air Force aircraft internal avionics applications shall be dual standby redundant, except where safety critical or flight critical requirements dictate a higher level of redundancy.

The scope of this section was limited to triservices dual standby-redundant data bus applications, which encompasses a large majority of the current and foreseen applications. This section, based on extensive past experience and lessons learned during system integration and test, should help designers avoid common problems encountered on past programs. Additionally, selective use of this section for applications that are not dual standby-redundant should be a basic design consideration.

30.3 Unique address (4.3.3.5.1.2). All remote terminals shall be capable of being assigned any unique address from decimai address O (00000) through decimal address 30 (11110). The address shall be established through an external connector, which is part of the system wiring and connects to the remote terminal. Changing the unique address of a remote terminal shall not require the physical modification or manipulation of any part of the remote terminal. The remote terminal shall, as a minimum, determine and validate its address during power-up conditions. No single point failure shall cause a terminal to validate a false address. The remote terminal shall not respond to any messages if it has determined its unique address is not valid.

There have been persistent problems with RT designs in which the five-bit RT address was either fixed internal to the subsystem or only one or two of the address bits could be externally programmed. None of these techniques allow easy migration of a subsystem among different systems in which, typically, RT addresses differ. The intent of the unique address requirement is to enhance interoperability by maintaining a single box in the supply inventory for multiple applications and by having the capability of selecting any RT address through an external connector on the box.

The requirement for rejection of a false address implies a parity method (or other means) of verifying that the address provided to it by the external programming connector is valid. The RT is required to reject all messages that fail address validation.

30.4 Mode codes (4.3.3.5.1.7).

30.4.1 Subaddress/mode (4.3.3.5.1.4). An RT shall have the capability to respond to mode codes with both subaddress/mode of 00000 and 11111. Bus controllers shall have the capability to issue mode commands with both subaddress/mode of 00000 and 11111. The subaddress/mode of 00000 and 11111 shall not convey different information.

Requiring the RT to implement both mode code indicators provides for maximum commonality among systems that range from pre-1553B designs through designs that incorporate 1553B and Notice 1. In addition, note the emphasis on the point that the same function must be performed by the RT, independent of whether the mode code indicator is 00000 or 11111.

30.4.2 Required mode codes (4.3.3.5.1.7).

30.4.2.1 Reset remote terminal required mode codes. An RT shall implement the following mode codes as a minimum:

Mode Code	Function
00010	Transmit status word
00100	Transmitter shutdown
00101	Override transmitter shutdown
01000	Reset remote terminal

Triservices and industry discussions identified a minimum set of mode commands that are required in each equipment specification. The standardization of the minimum set of mode commands will ease the task of data bus management by providing a minimal capability to perform error recovery (transmit status), system protection (transmitter shutdown and override), and initialization (reset).

30.4.2.2 Bus controller required mode codes. The bus controller shall have the capability to implement all of the mode codes as defined in 4.3.3.5.1.7. For Air Force applications, the dynamic bus control mode command shall never be issued by the bus controller.

Requiring the BC to have the capability of implementing all mode commands defined in 1553B provides the most flexibility for the system designer. However, the Air Force will not allow use of dynamic bus control because it may result in increased system complexity, system design and debug problems, and the problems associated with various types of hardware failure modes for each of the terminals that can assume control of the bus.

30.4.3 Reset remote terminal (4.3.3.5.1.7.9). An RT receiving the reset remote terminal mode code shall respond with a status word as specified in 4.3.3.5.1.7.9 and then reset. While the RT is being reset, the RT shall respond to a valid command with any of the following: no response on either data bus, status word transmitted with the busy bit set, or normal response. If any data is transmitted from the RT while it is being reset, the information content of the data shall be valid. An RT receiving this mode code shall complete the reset function within 5.0 milliseconds following transmission of the status word specified in 4.3.3.5.1.7.9. The time shall be measured from the mid-bit zero crossing of the parity bit of the status word to the mid-sync zero crossing of the command word at point A on figures 9 and 10.

Past system problems with this mode code have centered around the definition of “reset to a power-up initialized state” and how long it is acceptable for an RT to be offline or busy while performing this function. The definition for the reset function cannot be specified in a generic document such as a standard, but it must be left to the RT designer as to what hardware circuitry and software need to be reset in that particular application. However, from a systems viewpoint, the main requirement that this paragraph provides is that the RT must complete the reset function within 5 ms. During this 5 ms, very few restrictions are placed on the

RT response to valid oommands. This 5-ms time was seleoted to have minimal negative impact on system designs while providing a practical upper time limit for RT designs.

30.4.4 Initiate RT self-test (4.3.3.5.1.7.4). If the initiate self-test mode command is implemented In the RT, then the RT receiving the initiate self-teat mode code shall respond with a status word as specified in 4.3.3.5.1.7.4 and then initiate the RT self-teat function. Subsequent valid commands may terminate the self-test function. While the RT self-test is in progress, the RT shall respond to a valid command with any of the following: no response on either data bus, status word transmitted with the busy bit set, or normal response. If any data is transmitted from the RT while it is in self-test, the information content of the data shall be valid. An RT receiving this mode code shall complete the self-test functlon and have the results of the self-teat available within 100.0 milliseconds following transmisson of the status word specified In 4.3.3.5.1.7.4. The time shall be measured from the mld-bit zero crossing of the parity bit of the status word to the mld-sync zero crossing of the command word at point A on figures 9 and 10.

Past system problems with this mode code involve the state of the RT while the self-test function is being performed. The definition and scope of the self-test function cannot be specified in a generic dooument such as a standard, but must be left to the RT designer as to what hardware circuitry and software requires testing in the particular design. However, from a systems viewpoint, the main requirement that this paragraph provides is that the RT must have completed the self-test functlon within 100 ms and that the RT response to valid commands while the self-test functlon is being accomplished is clearly specified. This 100-ms time was selected to have minimal negative impact on system designs while providing a practical upper time limit for RT design.

30.5 Status word bits (4.3.3.5.3).

30.5.1 Information content. The status word transmitted by an RT shall contain valid information at all times, e.g., following RT power up, during initialization, and during normal operation.

RT designs exist In which the status word register has the terminal flag bit set or contains random data after power-up. This condltion is unacceptable in systems that poll the status of the RT and use that response to determine system health and, subsequently, maintenance actions. The intent of this paragraph is to ensure that the status word always contains valid information.

30.5.2 Status bit requirements (4.3.3.5.3). An RT shall Implement the status bits as follows:

Message error bit (4.3.3.5.3.3) - Required

Instrumentation bit (4.3.3.5.3.4) - Always logic zero

Service request bit (4.3.3.5.3.5) - Optional

Reserved status bits (4.3.3.5.3.6) - Always logic zero

Broadcast command received bit (4.3.3.5.3.7) - If the RT implements the broadcast option, then this bit shall be required.

Busy bit (4.3.3.5.3.8) - As required by 30.5.3

Subsystem flag bit (4.3.3.5.3.9) - If an associated subsystem has the capability for self-test, then this bit shall be required.

Dynamic bus control acceptance bit (4.3.3.5.3.10) - If the RT implements the dynamic bus control function, then this bit shall be required.

Terminal flag bit (4.3.3.5.3.11) - If an RT has the capability for self-test, then this bit shall be required.

This paragraph is intended to clarify conditions of use for each of the status bits. The most notable additions to the original standard are to define when the subsystem flag bit and the terminal flag bit must be implemented. RT designs exist that incorporate a subsystem self-test such that, upon detection of a fault, there is no indication to the BC of the problem. The requirements for these two bits has a philosophy similar to the original philosophy for the broadcast command received bit and the dynamic bus control acceptance bit.

30.5.3 Busy bit (4.3.3.5.3.8). The existence of busy conditions is discouraged. However, any busy condition, in the RT or the subsystem interface that would affect communication over the bus shall be conveyed via the busy bit. Busy conditions, and thus the setting of the busy bit, shall occur only as a result of particular commands/messages sent to an RT. Thus for a non-failed RT, the bus controller can, with prior knowledge of the remote terminal characteristics, determine when the remote terminal can become busy and when it will not be busy. However, the RT may also set the busy bit (in addition to setting the terminal flag bit or subsystem flag bit) as a result of failure/fault conditions within the RT/subsystem.

Many problems have occurred during system integration due to an RT responding as busy in an apparently unpredictable fashion. This also increases the complexity of the BC software, especially when the unpredictable busy responses occur within the error recovery procedures or occur differently for RTs within the same system design. The intent of this paragraph is to limit the use of the busy condition to specific, definable events (such as the receipt of a hypothetical "subsystem self-test 1“ command) and to associate with each event a predefine maximum length of time the busy condition will exist. Two specific conditions allow for setting the busy bit:

a. The RT is busy as a result of a particular command or message received over the data bus.

b. The RT is busy as a result of an RT or subsystem fault or failure.

These conditions should be specified in the interface control document (lCD) for that RT.

30.6 Broadcast (4.3.3.6.7). The only broadcast commands allowed to be transmitted on the data bus by the bus controller shall be the broadcast mode commands identified in table 1. The broadcast option may be implemented in remote terminals. However, if implemented, the RT shall be capable of distinguishing between a broadcast and a non-broadcast message to the same subaddress for non-mode command messages. The RT address of 11111 is still reserved for broadcast and shall not be used for any other purpose.

This paragraph was a compromise for triservices commonalty. The key restriction is that system designs cannot use the broadcast message format for data transfer. The intent of the paragraph is to limit the use of broadcast to situations such as resetting or synchronizing all RTs within a system, simultaneously, through use of the broadcast mode command message formats.

RT designers are still left with the option of implementing or not implementing the broadcast formats in an RT design. If the RT designer implements the broadcast option, the design must protect against corrupting data when the RT receives an inadvertent broadcast command (or a command the RT thinks is a broadcast command) to an address that is not associated with a mode code. In other words, the nonbroadcast data stored at a particular subaddress cannot be overwritten by a broadcast command.

30.7 Data wrap-around (4.3.3.5.1.4). Remote terminals shall provide a receive subaddress to which one to N data words of any bit pattern can be received. Remote terminals shall provide a transmit subaddress from which a minimum of N data words can be transmitted. N is equal to the maximum word count from the set of all messages defined for the RT. A valid receive message to the data wrap-around receive subaddress followed by a valid transmit command to the data wrap-around transmit subaddress, with the same word count and without any intervening valid commands to that RT, shall cause the RT to respond with each data word having the same bit pattern as the corresponding received data word. A data wrap-around receive and transmit subaddress of 30 (11110) is desired.

This paragraph is a new requirement in the standard. Its purpose is to provide an inexpensive and effective mechanism for determining data path integrity for the key elements of the RT, as well as for testing a multiplex system. There are certain parts of an RT, especially the front-end electronics that interface directly with the bus, that cannot be tested with the terminal self-test function. This wrap test capability will provide an additional level of testability while validation testing during operation of the system and at the depot.

The intent of the paragraph is to provide sufficient storage within the RT and/or subsystem to accept the longest message the RT is designed to handle. For example, if the operational message table or ICD for the RT has a maximum of nine data words in any receive message and twelve data words in any transmit message, then the RT must be designed to wrapup to a maximum of twelve data words. Note that the receive and transmit subaddresses may be different and that the maximum word count may be RT specific.

30.8 Message formats (4.3.3.6) Remote terminals shall, as a minimum, implement the following non-broadcast message formats as defined in 4.3.3.6: RT to BC transfers, BC to RT transfers, RT to RT transfers (receive and transmit), and mode command without data word transfers. For non-broadcast messages, the RT shall not distinguish between data received during a BC to RT transfer or data received during a RT to RT transfer (receive) to the same subsaddress. The RT shall not distinguish between data to be transmitted during an RT to BC transfer or data to be transmitted during an RT to RT transfer (transmit) from the same subaddress. Bus controllers shall have the capability to issue all message formats defined in 4.3.3.6.

The intent of this paragraph is to maximize the flexibility within an RT, while at the same time providing the system designer the capability of using the optimum set of message formats for the particular application. In the past, some RTs have not implemented RT-to-RT message formats, thus requiring the system designer to find another method of transferring the data from one RT to another, at times at the expense of overall system throughput. Additionally, the paragraph requires that data transferred to the same subaddress within an RT be identical in format and content, whether transferred either BC-to-RT or RT-to-RT. For example, if an RT has defined subaddress 10, word count of 12 to receive navigation data, then the RT must be able to receive those 12 words into subaddress 10 from either the BC (in a BC-to-RT transfer) or one or more RTs (in an RT-to-RT transfer). If the first data word is defined to be altitude, then it will be altitude for both types of transfers.

30.9 RT to RT validation (4.3.3.9). For RT to RT transfers, in addition to the validation criteria specified in 4.4.3.6, if a valid receive command is received by the RT and the first data word is received after 57.0 plus or minus 3.0 microseconds, the RT shall consider the message invalid and respond as specified in 4.3.3.6. The time shall be measured from the mid-bit zero crossing of the parity bit of the receive command to the mid-sync zero crossing of the expected data word at point A as shown on figures 9 and 10. It is recommended that the receiving RT of an RT to RT transfer verify the proper occurrence of the transmit command word and status word as specified in 4.3.3.6.3.

Problems have been encountered where the receiving RT in an RT-to-RT transfer will not time out when no data words are received from the transmitting RT. Instead, the receiving RT will pickup the data words from

the next message. The intent of this paragraph is to impose limits on the length of time a receiving RT can wait before it will no longer accept data words. The lower limit of 54 us is equivalent to 20 μs for the transmit command word plus 14 μs for the BC no response timeout, plus 20μs for the transmitting RT status word. The upper bound of 60 μs simply provides a reasonable timeout window.

30.10 Electrical characteristics (4.5.).

30.10.1 Cable shielding (4.5.1.1). The cable shield shall provide a minimum of 90.0 percent coverage.

Due to potential EMI radiation, shielding was increased from 75% to 90% coverage.

30.10.2 Shielding (4.5.1). All cable to connector junctions, cable terminations, and bus-stub junctions shall have continuous 360 degree shielding which shall provide a minimum of 75.0 percent coverage.

This paragraph returns the 1553B, Notice 1, paragraph 20.5 requirement back to the original 1553B requirement. The small physical area of the connector-to-cable junction does not require the increased EMI protection that Notice 1 required.

30.10.3 Connector polarity. For applications that use concentric connectors or inserts for each bus, the center pin of the connector or insert shall be used for the high (positive) Manchester hi-phase signal. The inner ring shall be used for the low (negative) Manchester hi-phase signal.

This is a new requirement based on the increased use of stand alone concentric connectors and triaxial inserts in multipin connectors. This ensures that RTs from two different vendors will not have the signal polarities reversed in the connector.

30.10.4 Characteristic impedance (4.5.1.2). The actual (not nominal) characteristic impedance of the data bus cable shall be within the range of 70.0 ohms to 85.0 ohms at a sinusoidal frequency of 1.0 megahertz.

This is the same requirement as 1553B, Notice 1, paragraph 20.4.2, in which the actual cable impedance was specified instead impedance. MIL-STD-1553B specifies the cable impedance of a given production lot from the manufacturer, while this paragraph requires that the actual piece of cable used in a system must meet the impedance requirements to limit waveform distortions and reflections of the terminated transmission line.

30.10.5 Stub coupling (4.5.1.5). For Navy applications, each terminal shall have both transformer and direct coupled stub connections externally available. For Navy systems using these terminals, either transformer or direct coupled connections may be used. For Army and Air Force applications, each terminal shall have transformer coupled stub connections, but may also have direct coupled stub connections. For Army and Air Force systems, only transformer coupled stub connections shall be used. Unused terminal connections shall have a minimum of 75 percent shielding coverage.

This paragraph reflects a triservices compromise due to different established practices that have evolved in each of the services in the implementation of 1553B. The common point is that all RTs must have transformer-coupled connectors. Note however, that in RTs with triservices application, both transformer-coupled and direct-coupled connections will be required on the RT.

3.10.6 Power on/off noise. A terminal shall limit any spurious output during a power-up or power-down, sequence. The maximum allowable output noise amplitude shall be ±250 mV peak, line-to-line for transformer coupled stubs and ±90 mV peak, line-to-line for direct coupled stubs, measured at point A of figure 12.

This is a new requirement to limit the uncontrolled, unrequested output from the terminal during power cycling. In the past, some RTs have even transmitted a complete 1553B word or multiple words during power cycling. This problem will increase as more elaborate power management capability is incorporated into the systems. Also, stores applications may encounter this problem because, typically, not all the stores are powered at the same time. The amplitude values were derived from the output symmetry paragraphs of 1553B and analyzed for practicality by several transceiver manufacturers.

SECTION 20 INDEX

SECTION 30

TERMINAL/SYSTEM SPECIFICATION CONSIDERATIONS

CONTENTS

FIGURES

TABLES

30. TERMINAL/SYSTEM DOCUMENTATION CONSIDERATIONS

This section presents examples and considerations for writing specifications for equipment and Multiplex Interface Control Documents (MICDs) for systems that interface with MIL-STD-1553B. Section 30.4 covers remote terminal (RT), bus controller (BC), and bus monitor (BM) specifications. Section 30.5 covers system MICDs.

30.1 Introduction

The basic electrical characteristics and protocol (or system management) for a multiplex data bus are contained in MIL-STD-1553B. The standard allows for design flexibility by providing options in areas such as data word and message formats, coupling techniques, and architectural configurations. This section (section 30 of MIL-HDBK-1553) provides information to aid in writing MIL-STD-1553B equipment and system documentation. It provides example paragraphs, each of which is followed by a discussion of its contents and other options available to the writer. Also included are references to the appropriate paragraphs of MIL-STD-1553B in which these topics are discussed; commentary for these paragraphs can be found in Section 20 of the handbook. This section is intended to be used as a guideline when writing documentation for MIL-STD-1553B equipment or systems.

30.2 Scope

This section includes documentation considerations for MIL-STD-1553B equipment and systems.

The examples (RT, BC, BM, and MICD), if extracted as a whole, are not meant to constitute a complete, consistent document. Rather, each individual example paragraph is provided to highlight the options available within MIL-STD-1553B and provide guidance in the development of a document. This section of the handbook should be used as a guideline to develop documentation that is consistent with the mission requirements for the particular equipment or system.

30.3 Definitions

Definitions of terms used in this section are listed in section 120 of this handbook.

30.4 Equipment specifications

Example specifications for RTs, BCS, and BMs are found in 30.4.1, 30.4.2, and 30.4.3, respectively. Whenever there are MIL-STD-1553B references relevant to specification paragraphs, they are included in parenthesis at the end of the specification paragraphs. These examples include only the 1553B requirements; other system dependent design requirements, such as, physical dimensions, thermal, vibration, etc. must be added to complete the specification.

30.4.1 Remote terminal (RT) example specification. The example specification provided below assume that the RT is embedded within a subsystem and will be interfaced to a MIL-STD-1553B dual standby-redundant data bus. The following paragraphs might be suitable for inclusion as specification performance requirements. These paragraphs are not recommended to be included as is, but should be modified as appropriate for the specific design.

SCOPE

APPLICABLE DOCUMENTS

Government documents

Specifications, standards, and handbooks

MILITARY STANDARDS

MIL-STD-1553B Digital Time Division Command/Response Multiplex Data Bus.

MIL-HDBK-1553A Multiplex Applications Handbook.

Non-Government Documents

COMMERCIAL STANDARDS

Society of Automotive Engineers, AS 4112 Production Test Plan for the Aircraft Internal Time Division Command/Response Multiplex Data Bus Remote Terminals.

The documentation listed above is recommended for inclusion in all RT specifications. Sections of the handbook should be identified as guidance or for contract compliance. For example, RT validation test plans (Section 100) and parameter formats (Section 80) sections should be considered for inclusion as contract compliance. Additional pertinent documentation is described in 10.7 of MIL-STD-1553B.

REQUIREMENTS

Design

Digital interface. The subsystem shall implement an embedded, serial digital interface which shall be utilized to transfer control and status information, as well as data to and from the subsystem.

This general requirement should be included for all RTs that are to be embedded in a subsystem. A similar requirement should be specified if the RT is being designed to service multiple subsystems.

Function. The digitai interface shall function in accordance with the MIL-STD-1553B requirements for a remote terminal (RT) (4.4.3).

This general requirement should be included in all RT specifications and should invoke the latest version of MIL-STD-1553B. If any Government-furnished equipment or contractor-furnished equipment to be provided does not meet the latest version of MIL-STD-1553B, then the version and notice to which the equipment was designed should be explicitly specified.

Address programming. The RT address shall be programmable through seven pins provided on an external connector. Five pins shall define the RT address. The sixth pin shall be used as parity for the RT address. The seventh pin shall be a return line and be used to program the address and parity pins to logic zero. An open address or parity pin shall be a logic one. The RT address shall be established in the wiring (4.3.3.5.1.2 and 30.3).

A specific method of implementing a unique RT address should be specified. The method of providing the address to the RT is not stated in MIL-STD-1553B. However, Notice 2 to MIL-STD-1553B (paragraph 30.3) imposes requirements on the RT addressing technique.

Data bus interface. The RT shall use a dual standby-redundant interface in accordance with MIL-STD-1553B (4.6 and 30.2).

This general requirement should be included in the specifications for all RTs that implement dual standby-redundant architectures. A similar requirement should be imposed on RTs that implement other architecture.

Data bus connectors. Two physically separate connectors that meet the requirements of MIL-STD-1553B shall be provided on the RT interface to the data bus (4.5.1.5.3).

The connector requirement should be specified for an RT that interfaces with a dual standby-redundant data bus. A similar requirement should be specified for RTs that interface with buses other than dual standby-redundant. The data buses may be connected by pins within a larger connector. If the subsystem is a store (e.g., missile, pod, etc.), the connector requirements of MIL-STD-1760 maybe applied.

Message format. The RT, as a minimum, shall implement the following nonbroadcast and broadcast message formats, as specified in 4.3.3.6 of MIL-STD-1553B: RT-to-BC transfers, BC-to-RT transfers, RT-to-RT transfers (receive and transmit), and mode command without data word (4.3.3.6 and 30.8).

Notice 2 to 1533B requires that the specified non-broadcast message formats be implemented in an RT. The specification should include a statement as to whether or not broadcast message formats should be implemented.

Subaddress assignments. Decimal subaddresses 16 (10000) through 30 (11110) shall be used first for subaddress assignments. Only after this selection of subaddresses has been depleted for this system may decimal subaddresses 1 (00001) through 15 (01111) be used.

This aids in utilization of the instrumentation bit.

Variable messaae blocks. The RT shall be capable of transmitting a subset of any message defined for it. These subsets shall consist of messages with word counts varying from one to the maximum word count defined for the particular message.

This specification provides for tailoring message transmissions to system requirements.

Mode codes. The RT shall respond to mode code commands from a BC as specified in MIL-STD-1553B and table 30-I (table I, 4.3.3.5.1.7, and 30.4.2.1).

Table 30-1. Remote Terminal Mode Code Requirements

T/R Bit	Mode code	Function	Associated data word	Broadcast command allowed	Required by Notioe 2
1	00000	Dynamic bus control	No	No	No
1	00001	Synchronize	No	Yes	No
1	00010	Transmit status word	No	Yes	Yes
1	00011	initiate self-test	No	Yes	No
1	00100	Transmitter shutdown	No	Yes	Yes
1	00101	Override transmitter shutdown	No	Yes	Yes
1	00110	Inhibit terminal ftag bit	No	Yes	No
1	00111	Override inhibit terminal flag bit	No	Yes	No
1	01000	Reset remote terminal	No	Yes	Yes
1	1000O	Transmit vector word	Yes	No	No
0	10001	Synchronize	Yes	Yes	No
1	10010	Transmit last oommand	Yes	No	No
0	10011	Transmit BIT word	Yes	No	No
0	10100	selected transmitter shutdown	Yes	Yes	No
0	10101	Override selected transmitter shutdown	Yes	Yes	No

The mode codes required by Notice 2 must be a capability for all RTs. The dynamic bus control mode code is required if the RT implements dynamic bus control. Note that the following mode codes, if implemented, have predefine responses: dynamic bus control, inhibit terminal flag, override inhibit terminal flag bit, and transmit last command. Also, implementation of the transmit vector word mode code (normally in conjunction with the service request bit) is recommended for RTs that implement time- critical asynchronous functions that require aperiodic service by the BC. The selected transmitter shutdown (10100) and override- selected transmitter shutdown(10101) mode codes should be specified in RTs designed for system architectures that employ a minimum of triple redundancy. Table 30-I is extracted from table I of 1553B and should be included in the specification.

Reset remote terminal. The RTshall implement this command as specified in MIL-STD-1553B and shall complete the reset function within 5.0 ms. While being reset, the RT shall not respond to messages sent to it on either bus (4.3.3.5.1.7.9 and 30.4.3).

The RT reset capability should be specified, including timing and unique RT reset period response requirements.

Initiate self-test. The RT shall implement this command as specified in MIL-STD-1553B and shall have the results of the self-test available within 100.0 ms. While the self-test is in progress, the RTshall respond by transmitting a status word with the busy bit set (4.3.3.5.1.7.4, 30.4.4).

if the initiate self-test mode command is required by the specification, the timing and unique RT response also should be specified. This is not the self-test of the associated subsystem.

Status flags. The RT shaii be capabie of responding with status information and shall implement status flags as specified in MIL-STD-1553B and table 30-II (4.3.3.5.3, and 30.5.2).

Table 30-11. Remote Terminal Status Flag Requirements

Bit time	Status bit	Requirement
9	Message error bit	Required (Notice 2)
10	Instrumentation bit	Always logic zero
11	SeNice request bit	Optional
12-14	Reserved status bits	Always logic zero
15	Broadcast command received bit	Conditionally required
16	Busy bit	Optional. If used, restricted
17	Subsystem flag bit	Conditionally required
18	Dynamic bus control acceptance	Conditionally required
19	Terminal flag bit	Conditionally required

The status bits required by Notice 2 to MIL-STD-15536 should be included for all RTs. If the unit containing the RT implements broadcast, terminal or associated subsystem self-test, or dynamic bus control, then the corresponding status bits must be specified. The busy bit may only be used in pre-defined circumstances. Also, implementation of the service request bit (typically in conjunction with the transmit vector word mode code) is recommended for RTs that implement time-critical asynchronous functions requiring aperiodic service by the BC. Details regarding the set and use of bits must be included in the individual paragraphs.

Busy bit. The use of this bit by the RT is optional and, if used, restricted (4.3.3.5.3.8 and 30.5.3).

Any condition in the RT or subsystem, that will cause the busy bit to be set, affecting communications over the data bus, should be specified. An example is a magnetic tape recorder system up-to-speed indication. The duration of the busy condition should also be specified when that condition results from receipt of particular commands or messages by the RT. Notice 2 to MIL-STD-1553B requires that specific, predictable conditions be defined that determine when the RT will set the busy bit.

Terminal flag bit. A terminal flag shall be used that does not discriminate between the two channels of a dual standby-redundant RT (4.3.3.5.3.11).

Specifying the use of this bit is equivalent to specifying that the RT has implemented self-test. Optional mode codes, such as Inhibit Terminal Flag Bit, override Terminal Flag Bit, and Transmit BIT Word should be considered when use of the Terminal Flag is specified.

Sample consistency. Messages transmitted over the data bus shall contain only mutually consistent samples of information. Different words used to transmit multiple precision parameters, updated at the same rate, shall all be members of the same sample set. Suitable buffering and transmission control logic shall be provided to prevent transmission of a partially updated message that would contain mutually inconsistent data.

This requirement should be included in any specification for an RT that has multiple, time-dependent data words to transmit that could be updated while the data are being transmitted on the bus.

Data format. Digital data shall be transmitted in a format compatible with the word and message formats specified in MIL-STD-1553B. The development of data words and message formats shall be in accordance with the guidelines in section 80 of MIL-HDBK-1553. Any invalid data transmitted over the data bus shall be indicated as invalid within the same message the data appears (4.3.3.5 and 4.3.3.6).

This general requirement for message and data word formats should be included for all RTs. The guidelines found in section 80 of this handbook provide for necessary standardization of these formats.

Illegal commands. The RT shall be designed to recognize the illegal commands as identified in table 30-x.x.x. The RT shall respond to these commands as required by MIL-STD-1553B (4.4.3.4).

Table 30-x.x.x. Illegal commands. (specified by procuring agency)

The illegal commands identified shall include, as a minimum, those mode codes which are not reserved and which are not implemented by the RT. In addition, the table may include those command words which the RT is not designed or programmed to operate with.

It should be noted that some RTs are not capable of monitoring for these command words due to the complexity of the circuitry required to identify an illegal command within the MIL-STD-1553B timing constraints. However, should the RT function be so critical that the receipt of an unimplemented command is not tolerable, this specification should be revised accordingly.

Data wrap-around subaddress. The RT shall implement a data wrap-around capability and shall use a data wrap-around receive and transmit subaddress of 30 (11110) (30.7).

Notice 2 to MIL-STD-1553B requires RTs to provide a data wraparound capability. This paragraph invokes that capability and specifies the subaddress desired by Notice 2.

Design goals. Care should be taken in the RT design to allow for growth and flexibility. Considerations shouid be given to providing spare subaddresses (both transmit and receive) and data words within used subaddresses.

This requirement provides for future growth of the RT.

Stub coupling. The RT shall have transformer-coupled stub connections as specified in MIL-STD-1553B. Direct-coupled stubs connections, as specified in MIL-STD-1553B, may be provided in addition to the transformer-coupied stub connections (4.5.1.5 and 30.10.5).

This general requirement must be included in all RT specifications. If direct-coupled stubs are required (they may be for Navy applications), the specification should be changed accordingly.

General. The requirements of MIL-STD-1553B shall be implemented for an RT without exception unless otherwise agreed to in writing by the procuring activity.

This general requirement should be included in all RT specifications.

Data requirements. A muitiplex interface control document (MICD) describing the RT interface with the MIL-STD-1553B multiplex data bus shall be prepared and submitted to the Government in accordance with the contract data requirements.

This requirement provides for the delivery of the interface documentation required to provide for life cycle maintenance of the RT.

QUALITY ASSURANCE PROVISIONS

Methods of Inspection

Interfacs testing. The RT shall be tested in accordance with section 100, RT Validation Test Pian, of MIL-HDBK-1553. Production units shall be tested in accordance with SAE RT Production Test Plan AS 4112. An RT Test Pian (data item DI-T-3702A) and an RT Validation Test Report shall be provided (data item DI-T-5247).

This general requirement, which provides for validation testing and production testing, should be included in all RT specifications. The data items cited are suitable for all DOD agencies.

NOTES

Data requirements. When this specification is used in an acquisition that incorporates a contract data requirements list (CDRL) (DD form 1423), the data requirements identified in the following list shall be developed as specified by an approved data item description (DID) (DD form 1664).

Para. no.	Data requirements	Applicable DID no.	Options
	Muitiplex Interface Control Document	DI-MISC-60343	———

The data requirements shall be delivered in accordance with the approved CDRL incorporated into the contract. When the provisions of DOD FAR supplement, part 27, subpart 27.410-6, are invoked and the DD form 1423 is not used, the data requirements specified in the list shall be delivered by the contractor in accordance with contract or purchase order requirements. Deliverable data required by this specification are also cited in the list.

This requirement provides for the delivery of an MICD prepared in accordance with an Army DID. Similar DIDs, consistent with the data word and message preparation formats in section 80 of this handbook, should be specified to meet Navy and Air Force requirements.

30.4.2 Bus controller (BC) example specification.

The example paragraphs provided below assume that the BC will be a bus controller on a MIL-STD-1553B dual standby-redundant data bus. The following paragraphs might be suitable for inclusion as specification performance requirements. These paragraphs are not recommended to be included as is, but should be modified as appropriate for the specific design.

SCOPE

APPLICABLE DOCUMENTS

Government documents
Specifications, standards, and handbooks

MILITARY STANDARDS

MIL-STD-1553B Digital Time Division Command/Response Multiplex Data Bus.
MIL-HDBK-1553A Multiplex Applications Handbook.

Non-Government Documents

COMMERCIAL STANDARDS

Society of Automotive Engineers

AS 4113 Validation Test Plan for the Aircraft Internal Time Division Command/ Response Multiplex Data Bus Controllers.

AS 4114 Production Test Plan for the Aircraft Internal Time Division Command/ Response Multiplex Data Bus Controllers.

The documentation listed above is recommended for inclusion in all BC specifications. Additional pertinent documentation is described in paragraph 10.7 of MIL-STD-1553B.

REQUIREMENTS

Design

Digital Interface. The bus controller (BC) shall implement an embedded, high speed digital interface that shall provide the capability to initiate transfers over the MIL-STD-1553B multiplex data bus.

This general requirement should be included for all BCs.

Data bus interface. The BC shall use a dual standby-redundant interface in accordance with MIL-STD-1553B (4.4.2).

This general requirement should be included in the specifications for all BCs that implement both dual standby-redundant architectures and other architectures and should invoke the latest version of MIL-STD-1553B. If any Government-furnished equipment or contractor-furnished equipment to be provided does not meet the

latest version of MIL-STD-1553B, then the version and notice to which the equipment was designed should be explicitly specified.

Function. The digital interface shall function in accordance with the MIL-STD-1553B requirements for a Bus Controller (BC). (4.4.2)

This general requirement should be included in all BC specifications invoking the latest version of MIL-STD-1553B. If either Government Furnished Equipment or Contractor Furnished Equipment is to be provided which does not meet the latest version of MIL-STD-1553B, then the version and notice to which the equipment was designed should be explicitly specified.

Address programming. If an address is assigned to the BC, the BC address shall be programmable through seven pins provided on an external connector. Five pins shall define the BC address. The sixth pin shall be used as parity for the BC address. The seventh pin shall be a return line and be used to program the address and parity pins to logic zero. An open address or parity pin shall be a logic one. The BC address shall be established in the wiring (4.3.3.5.1.2 and 30.3).

ABC must be assigned an address only when it has the capability to act as an RT. If required, a specific method of implementing a unique BC address should be specified. The method of providing the address to the BC is not stated in MIL-STD-1553B. However, if an address is assigned to a BC, then the requirements of Notice 2 to MIL-STD-1553B (paragraph 30.3), imposed for the RT addressing technique, should be applied.

Data bus connectors. Two physically separate connectors that meet the requirements of MIL-STD-1553B shall be provided on the BC interface to the data bus (4.5.1.5.3).

The above requirement should be specified for a BC. The requirement is for a BC on a dual standby-redundant data bus. A similar requirement should be specified for BCs on other than dual standby-redundant buses. The data buses may be connected by pins within a larger connector.

Message formats. The BC shall be capable of issuing all message formats, nonbroadcast and broadcast, as specified in MIL-STD-1553B (4.3.3.6 and 30.8).

This general requirement must be included in all BC specifications.

Mode codes. The BC shall be capable of issuing and transmitting the nonbroadcast and broadcast mode code commands specified in MIL-STD-1553B and table 30411 (table I, 4.3.3.5.1.7, and 30.4.2.1).

Notice 2 requires that all assigned mode codes be implemented in all BCs. Note that the following mode codes have pre-defined responses: dynamic bus control, inhibit terminal flag, override inhibit terminal flag bit, and transmit last command.

Status flags. The BC shall be capable of processing RT status information as specified in MIL-STD-1553B and table 30-IV (4.3.3.5.3).

Processing requirements for status bits should be specified for the BC.

RT addressing. The BC shall implement the capability of addressing 31 RTs within the remote terminal address range 00000 through 11110, inclusive. Remote terminal address 11111 shall be implemented and shall be reserved for broadcast information transfers as specified in MIL-STD-1553B (4.3.3.5.1.2 and 30.8).

Table 30-111. BC Mode Code Requirements

T/R bit	Mode code	Function	Associated data word	Broadcast command allowed	Required
1	00000	Dynamic bus control	No	No	No
1	00001	Synchronize	No	Yes	No
1	00010	Transmit status word	No	Yes	Yes
1	00011	Initiate self-test	No	Yes	No
1	00100	Transmitter shutdown	No	Yes	Yes
1	00101	Override transmitter shutdown	No	Yes	Yes
1	00110	Inhibit terminal flag bit	No	Yes	Yes
1	00111	Override inhibit terminal flag bit	No	Yes	Yes
1	01000	Reset remote terminal	No	Yes	Yes
1	10000	Transmit vector word	Yes	No	Yes
0	10001	Synchronize	Yes	Yes	Yes
1	10010	Transmit last command	Yes	No	No
1	10011	Transmit BIT word	Yes	No	No
0	10100	Selected transmitter shutdown	Yes	Yes	Yes
1	10101	Override selected transmitter shutdown	Yes	Yes	Yes

Table 30-IV. BC Status Flag Requirements

Bit time	Status bit	Requirement
9	Message error bit	Required
10	Instrumentation bit	Always logic zero
11	Service request bit	Required
12-14	Reserved status bits	Always logic zero
15	Broadcast command received bit	Required
16	Busy bit	Required
17	Subsystem flag bit	Required
18	Dynamic bus control acceptance bit	Required
19	Terminal flag bit	Required

This general requirement should be included in all BC specifications to allow for future system growth and to ensure that the BC is capable of addressing all RTs.

Sample consistency. Messages transmitted over the data bus shall contain only mutually consistent samples of information. Different words used to transmit muitiple precision parameters, updated at the same rate, shall all be members of the same sample set. SuiTable buffering and transmission control logic shall be provided to prevent transmission of a partiaiiy updated message that wouid contain mutually inconsistent data.

This requirement should be included in any specification fora BC that has multiple, time-dependent data words to transmit that could be updated while the data are being transmitted on the bus. This includes a BC that initiates such data words, as well as receives, processes and/or reformats, and retransmits such data words.

Data format. Digital data shall be transmitted in a format compatible with the word and message formats specified in MIL-STD-1553B. Data words and message formats shall be developed in accordance with the guidelines in section 80 of MIL-HDBK-1553. Any invalid data transmitted over the data bus shall be indicated as invalid within the same message in which the data appear (4.3.3.5 and 4.3.3.6).

This general requirement for message and data formats should be included for all BCs. The second and third sentences, particularly, should be included in the specification of any BC that initiates or reformats messages for transmission on the data bus. The guidelines found in section 80 of this handbook provide for necessary standardization of these formats.

Data wrap-around test. The BC shall implement the capability to perform data wraparound tests (30.7).

This requirement provides for the capability of performing real-time testing of the MIL-STD-1553B data communications interface. It should be included in all BC specifications.

Stub coupling. The BC shall have transformer-coupled stub connections as specified in MIL-STD-1553B. Direct coupled stub connections, as specified in MIL-STD-1553B, may be provided in addition to transformer-coupled connections (4.5.1.5 and 30.10.5).

This general requirement should be included in all BC specifications. If direct-coupled stubs are required (as they may be for Navy applications), the specification should be changed accordingly.

General. The requirements of MIL-STD-1553B shall be implemented for a BC, without exception, unless otherwise agreed to in writing by the procuring activity. If the BC has the capability of functioning as a RT or BM, then the RT or BM requirements of MIL-STD-1553B shall be implemented, without exception, unless otherwise agreed to in writing by the procuring activity (4.4.3 and 4.4.4).

This general requirement should be included in all BC specifications. The second sentence should be included in the specification of any BC that is required to perform as either an RT or a BM.

Data requirements. A multiplex interface control document (MICD) describing the BC interface with the MIL-STD-1553B multiplex data bus shaii be prepared and submitted to the Government in accordance with the contract data requirements.

This requirement provides for delivery of the interface documentation required to provide for life cycle maintenance of the BC.

QUALITY ASSURANCE PROVISIONS

Methods of Inspection

Interface testing The BC shall be tested in accordance with AS 4113. Production units shall be tested in accordance with AS 4114.

This general requirement, which provides for validation testing and production testing, should be included in all BC specifications.

NOTES

Data requirements. When this specification is used in an acquisition that incorporates a contract data requirements list (CDRL) (DD form 1423), the data requirements identified in the following list shall be developed as specified by an approved data item description (DID) (DD form 1664).

Paragraph no.	Data requirements	Applicable DID no.	Options
	Multiplex interface Control document	DI-MISC-80343	———

The data requirements shall be delivered in accordance with the approved CDRL incorporated into the contract. When the provisions of DOD FAR supplement, part 27, subpart 27.410-6, are invoked and the DD form 1423 is not used, the data requirements specified in the list shall be delivered by the contractor in accordance with contract or purchase order requirements. Deliverable data required by this specification are also cited in the list.

This requirement provides for the delivery of an MICD prepared in accordance with an Army DID. Similar DIDs, consistent with the data word and message presentation formats in section 80 of this handbook, should be specified to meet Navy and Air Force requirements.

30.4.3 Bus monitor (BM) example specification. The example paragraphs provided below assume that the BM will be a bus monitor on a MIL-STD-1553B dual standby-redundant data bus. The following paragraphs might be suitable for inclusion as specification performance requirements. These paragraphs are not recommended to be included as is but should be modified as appropriate for the specific design.

SCOPE

APPLICABLE DOCUMENTS

Government documents

Specifications, standards, and handbooks

MILITARY STANDARDS

MIL-STD-1553B Digital Time Division Command/Response Multiplex Data Bus.

MIL-HDBK-1553A Multiplex Applications Handbook

Non-government documents

COMMERCIAL STANDARDS

Society of Automotive Engineers, AS 4115, Test Plan for the Digital Internal Time Division Command/Response Muitipiex Data Bus System.

The documentation listed above is recommended for inclusion in all BM specifications. Additional pertinent documentation is described in paragraph 10.7 of MIL-STD-1553B.

REQUIREMENTS

Design

Digital interface. The bus monitor (BM) shall implement an embedded, high-speed digital interface that shall be Dcapable of monitoring transfers over the MIL-STD-1553B muitiplex data bus.

This general requirement should be included for all BMs.

Data bus interface. The BM shall use a dual standby-redundant interface in accordance with MIL-STD-1553B.

This general requirement should be included for all BMs that require dual standby-redundant interfaces. A similar requirement should be specified if the BM is being designed to support other than dual standby-redundant interfaces.

Function. The digital interface shall function in accordance with the MIL-STD-1553B requirements for a BM (4.4.4).

This general requirement should be included in the specifications for all BMs and should invoke the latest version of MIL-STD-1553B. If any Government-furnished equipment or contractor-furnished equipment to be provided does not meet the latest version of MIL-STD-1553B, then the version and notice to which the equipment was designed should be explicitly specified.

Data bus connectors. Two physically separate connectors, meeting the requirements of MIL-STD-1553B, shall be provided on the BM interface to the data bus (4.5.1.5.3).

This requirement should be specified for a BM on a dual standby-redundant data bus. A similar requirement should be specified for BMs on buses other than dual standby-redundant.

Stub coupling. The BM shall have transformer-coupled stub connections as specified in MIL-STD-1553B. Direct-coupled stub connections, as specified in MIL-STD-1553B, may be used in addition to the transformer-coupled stub connections (4.5.1.5 and 30.10.5).

This general requirement should be included in all BM specifications. If direct-coupled stubs are required (as they are for Navy applications), the specification should be changed accordingly.

General. The requirements of MIL-STD-1553B shall be implemented for a BM, without exception, unless otherwise agreed to in writing by the procuring activity (4.4.4).

This general requirement should be included in all BM specifications.

QUALITY ASSURANCE PROVISIONS

Use paragraphs similar to those for bus controller quality assurance, paragraph 30.4.2 above.

NOTES

Data requirements

Use paragraphs similar to those for bus controller data requirements, paragraph 30.4.2 above.

30.5 System mulltiplex interface control document example

Integrated, multiplexed systems are the rule, rather than the exception, in today's system. Yet, the development of documentation, which is essential to the understanding and use of the system, often becomes a secondary consideration. The Multiplex Intertace Control Document (MICD) is, in concert with specifications described in Section 30.4, an integral part of the system documentation, providing the protocol and information transfer requirements necessary to properly perform the integration function.

The MICD is used to define the electrical and physical interfaces related to information transfer over the MIL-STD-1553B data bus. It documents the system protocol implementation and structure, defines message blocks, identifies transfer and update rates, details message and data word interrelationships, and specifies whether the optional features in MIL-STD-1553B are to be implemented. It documents the message traffic on the MIL-STD-1553B bus in a format which encourages the use of standardized data word and message formats described in Section 80. Data Item Description DI-MISC-80343, developed specifically for MIL-STD-1553 systems, contains the format and content preparation instructions for an MICD.

30.5.1 System MICD example. The following text provides typical examples of MICD paragraphs which can be modified, based on specific system performance requirements, to develop a system MICD. These paragraphs are not recommended for inclusion in a system MICD as written; they should be modified as appropriate to reflect the specific system design.

SCOPE

APPLICABLE DOCUMENTS

MILITARY STANDARDS

MIL-STD-1553B Digital Time Division Command/Response Multiplex Data Bus.

MIL-HDBK-1553A Multiplex Applications Handbook.

The documentation listed above is recommended for inclusion in all system MICDs. Additionally, all applicable military and commercial terminal specifications, the system specification, and ail applicable subsystem MICDs should be listed.

A system MICD should describe the functions of each of the subsystems which are integrated via the multiplex bus. This description is not intended to provide a comprehensive explanation of the operation of each subsystem, but to acquaint the user of the system MICD with the general operation of each subsystem and how it interacts with other system elements. Detailed subsystem descriptions, whether contained in technical manuals and/or subsystem MICDs, should be referenced in the "Applicable Documents", of the system MICD. The following paragraph would be used to further describe the system:

Subsystem Connected to Data Bus. The subsystems that are connected to the data bus shall be as shown in table 30-V.

Table 30-V. Subsystems Connected to Data Bus

Item	Qty per system	Type
Remote Terminal A	1	RT-XXXX/XXX-XXX
•	•	ž
•	ž	ž
•	•	ž
•	ž	ž
Remote Terminal N	1	RT-XXXX/XXX-XXX
Bus Controller A	1	BC-XXXX/XXX-XXX
Bus Controller B	1	BC-XXXX/XXX-XXX
Bus Monitor A	1	BM-XXXX/XXX-XXX

All the terminals that are to makeup the system should be listed in this table.

30.5.1.2 Physical Characteristics.

This section of the system MICD defines the physical or electrical characteristics of the MIL-STD-1553 bus system, particularly those characteristics that are beyond the scope of the standard. Typical example paragraphs are presented below.

Digital Interface. The system shall implement embedded, serial digital interfaces which shall be utilized for control, status, and data transfers.

This general requirement should be included for all MIL-STD-15536 systems.

Function. All of the digitai interfaces within the system shall function in accordance with the MIL-STD-1553B requirements for Remote Terminals (RTs), Bus Controllers (BCs), or Bus Monitors (BMs), as appropriate. (4.4.2, 4.4.3, and 4.4.4)

This general requirement should be included in all system MICDs, invoking the latest version of MIL-STD-1553B. If either Government Furnished Equipment or Contractor Furnished Equipment is to be provided which does not meet the latest version of MIL-STD-15536, then the version and notice to which the equipment was designed should be identified.

General. The requirements of MIL-STD-1553B shall be implemented for the system, without exception, unless otherwise agreed to in writing by the procuring activity.

This general requirements should be included in all System MICDs.

Data Bus Topology. The system shall utilize a single level bus topology with a dual, standby-redundant MIL-STD-1553B data bus, as shown in figure 30-1.

This general requirement should be included and illustrated for all systems that use a single level topology with a dual, standby-redundant data bus. A similar requirement should be included and illustrated for systems utilizing single level topologies with other redundancy requirements. Multiple level topologies require

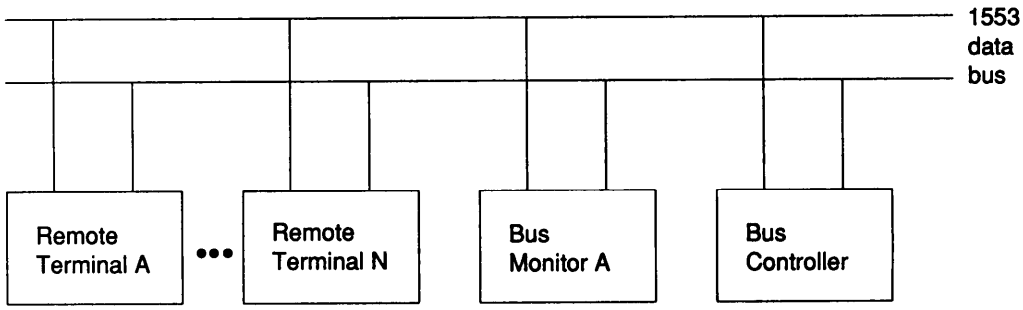


Figure 30-1. System Configuration - Normal Operation

additional detail. An example of this would be a weapon system which utilizes a series of single level bus topologies, each handling a different function and operating independently of the others, but with equivalent levels of control. In this case, the MICD should include the function of each bus, the terminals connected to each bus, and any communication between any of the buses.

Redundancy. The redundant buses shall be physically separated from one another, and shall not be routed within the same wire bundles except at the point of entry Into an RT, BC, or BM. A backup bus controller, which operates as either an RT or a bus monitor under normal operating conditions, shall be provided to assume control of the bus in the event of failure of the primary bus controller. The backup bus controller shall be physically separated from the primary bus controller.

This requirement is designed to ensure that the survivability requirements of the system are met. These requirements, in turn, influence the selection of data bus topology and control methods.

Data bus connectors. Two physically separate connectors, meeting the requirements of MIL-STD-1553B, shall be provided on each interface to system terminals. All terminal addresses shall be programmable through seven pins provided on a third external connector. Five pins shall define the address. The sixth pin shall be used as parity for the address. Odd parity shall be used. There shall be no response to any message if the address parity is not valid. The seventh pin shall be a return line and be used to program the address and parity pins to logic zero. An open open address or parity pin shall be a logic one. The address shall reestablished in the system wiring. (4.3.3.5.1.2, 4.5.1.5.3, 30.3)

This requirement should be included for all systems that utilize a dual-redundant data bus. A similar requirement should be included for systems that utilize buses other than dual-redundant. The specific method used to implement unique addresses should be described. The method of providing the address to a terminal is not stated in MIL-STD-1553B. However, Notice 2 to MIL-STD-1553B (paragraph 30.3) imposes requirements on the addressing technique. If it is necessary to assign an address to a BC, then these requirements apply equally to it.

Terminal Address Assignments. The terminal address assignments for the system shall be as listed in table 30-VI.

The definition of the terminal addresses should be included in all system MICDs. In general, lower numbered addresses should be assigned first (except for 00000), with higher numbered addresses reserved for future system growth.

Stub coupling. The system shall have transformer coupled stub connections as specified in MIL-STD-1553B. (4.5.1.5, 30.10.5)

Table 30-VI Terminal Address Assignments

Terminal address	Terminal
00000	Reserved
00001	Bus Controller A (primary)
00010	Bus Controller B (back-up)
00011	Remote Terminal A
ž	•
ž	•
•	
XXXXX	Remote Terminal N
•	Reserved
ž	•
•	•
11111	Reserved

This general requirement should be included in all system MICDs. If direct coupled stubs are required, as they are for Navy applications, the MICD should be changed accordingly.

> **System Security. The system data bus shall be an all BLACK bus; only encrypted or unclassified signals shall be transmitted over it. No terminal that handles unencrypted classified signals shall be connected directly to the bus. The system shall include TEMPEST design to prevent compromising emanations from by-passing the encryption circuitry.**

This paragraph describes the system security architecture. Other possible architectures are discussed in paragraph 60.2.3.6 of this handbook.

30.5.1.3 Protocol. The protocol section of a system MICD defines the specific MIL-STD-1553B protocol features, such as message formats, mode codes, and status flags, and specifies their implementation within the system. In situations where terminal capabilities differ, such as an RT without the capability to respond to a Transmit Vector Word mode command, the MICD should provide terminal specific requirements. In developing the system protocol, data on the following is identified for each subsystem, and should be included in the system MICD.

a. Condition which sets the option status word bits (busy, service request, subsystem flag, terminal flag).

b. Mode code conditions.

c. Specific conditions for generation of mode code commands and required responses to these.

d. Illegal command detection (what is legal for the box and what actions are taken for illegal commands).

e. Timing limits associated with the mode codes (i.e., actual length of time needed to reset or perform self test).

f. Discretes to be monitored and a detailed operation of each (e.g., 'on-line' or BC/BBC).

g. Specific power up initialization sequence including required messages or programming (e.g., data loads, parameter initialization, operational controls, degraded mode, etc.).

h. Maximum power uptime until 'on-line', including sequence (e.g., no response, followed by busy, followed by normal).

i. Aperiodic messages (if any) must be identified and the mechanism (such as Transmit Vector Word Mode Code) defined to allow the subsystem to transmit the message.

j. Message timing constraints, sequencing, transfer rates, and interaction (if any) with the busy bit.

k. Subsystem self-test procedures (internal, data wraparound, BIT, etc.).

l. Data coherence, data validity, and sample consistency procedures.

m. Service request procedures (command sequence or vector word definitions).

n. Unique shutdown requirements.

o. Unique or subsystem specific message strings (loading, mass transfer, sequence of messages, etc.).

P. Validity bits (usage, rules for setting, interaction with data).

q. Operational characteristics during "shutdown" transmitter mode code (i.e., is the terminal still capable of receiving and processing data from the bus).

Additionally, system operating characteristics such as the following should be included in the system MICD.

a. Bus controller response to status bits.

b. Mode code conditions.

c. Message restrictions or data transformation (units or coordinate system) requirements.

d. Message timing restraints, sequencing, transfer rates, and interaction (if any) with the busy bit.

e. System self-test procedures.

f. Specific polling procedures for monitoring bus and terminal health.

9. Modes of operation and specific procedures associated with each (e.g., built-in-test, initialization, normal and degraded operation, maintenance, or priority operation).

h. Data resolution requirements, not to exceed subsystem capabilities.

Typical example protocol paragraphs are as follows:

> **Information Transfer Formats. The system shall implement the following non-broadcast message formats, as specified in paragraph 4.3.3.6 of MIL-STD-1553B: RT to BC transfers, BC to RT transfers, RT to RT transfers (receive and transmit), and mode command without data word transfers. in addition, the system shall implement the broadcast synchronize mode command (with and without data word). (4.3.3.6, 30.8)**

The information transfer formats to be implemented in the system should be described in all system MICDs. Notice 2 to MIL-STD-1553B requires that remote terminals implement, as a minimum, the non-broadcast information transfer formats defined in the example paragraph above, and that BCs have the capability to issue all information transfer formats.

Message Traffic - Normal Operation. The message traffic for the system under normal operating conditions should be as shown In figure 30-2.

This type of description of normal message traffic flow should be included in all system MICDs. Also see paragraph 30.5.7 of this section. A description of degraded and backup modes of operation (if any) should also be included in the system MICD.

Mode Codes. The system protocol shall implement mode commands as specified in table 30-VII and paragraph 4.3.3.5.1.7 of MIL-STD-1553B (4.3.3.5.1.7, 30.4.2.1, table 1)

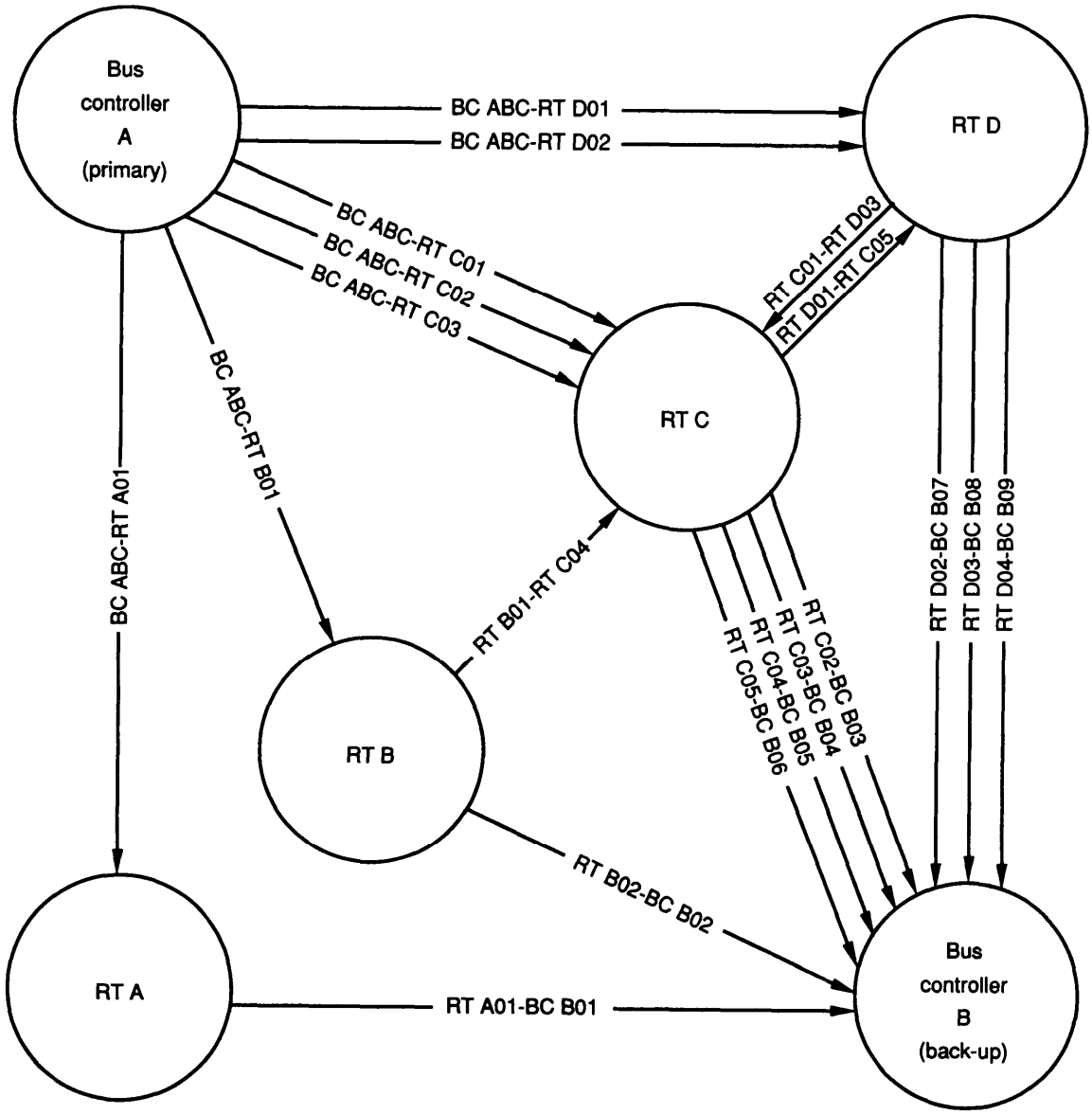


Figure 30-2. Message Flow Diagram - Normal Operation

Table 30-VII. System Mode Codes

T/R BIT	Mode code	Function	Associated data word	Broadcast command allowed	Implemented
1	00000	Dynamic bus control	No	No	No
1	00001	Synchronize	No	Yes	No
1	00010	Transmit status word	No	No	Yes
1	00011	Initiate self test	No	Yes	No
1	00100	Transmitter shutdown	No	Yes	Yes
1	00101	Override transmitter shutdown	No	Yes	Yes
1	00110	Inhibit terminal flag bit	No	Yes	No
1	00111	Override inhibit terminal flag bit	No	Yes	No
1	01000	Reset remote terminal	No	Yes	Yes
1	10000	Transmit vector word	Yes	No	Yes
0	10001	Synchronize	Yes	Yes	No
1	10010	Transmit last command	Yes	No	No
1	10011	Transmit BIT word	Yes	No	No
0	10100	Selected transmitter shutdown	Yes	Yes	No
0	10101	Override selected transmitter shutdown	Yes	Yes	No

Table 30-VII reflects the system mode code implementation. It may also be necessary to specify the mode code requirements on an RT by RT basis. The system should implement the Notice 2 required mode codes, where subsystem capabilities permit. Note that the following mode codes have predefine responses, if implemented: Dynamic Bus Control, Inhibit Terminal Flag Bit, Override Inhibit Terminal Flag Bit, and Transmit Last Command. Also, implementation of the Transmit Vector Word mode code (normally in conjunction with the service request bit) is recommended for RTs that implement time critical asynchronous functions requiring aperiodic service by the BC. The Selected Transmitter Shutdown (00100)and Override Selected Transmitter Shutdown (00101) mode codes should be specified in RTs designed for system architectures that employ a minimum of triple redundancy. Specific information on the mode commands can be found in section 60.3.1.3.

Dynamic Bus Control. The system shall not implement the Dynamic Bus Control mode code.

This mode code is used, together with the Dynamic Bus Control Acceptance Bit of the status word, to pass control from one BC to another in a “Nonstationary Master” scheme of bus control. If required for system operation, the MICD should specify the BCs allowed to accept control of the bus and control requirements (such as timing, priorities, and frequency of bus control exchange).

Synchronize (without data word). The system shall implement the Synchronize (without data word) mode code.

If this mode code is used, the MICD should reflect which terminals will respond to it and should functionally specify the synchronization type (such as time, message table, or minor or major cycle indication synchronization) required to occur.

Transmit Status Word. The system shall implement the Transmit Status Word mode code. This mode code shall be used to retrieve the status word from an RT, when the RT fails to transmit a status word in response to a non-broadcast message or following the transmission of a broadcast message. If the status word reveals a message error, terminal error recovery

processing procedures shall be initiated. Transmission of this mode command to each broadcast-capable RT shall be initiated within 150.0 milliseconds following the transmission of each broadcast command, with all transmission occurring within the same minor frame. If any status word does not have the Broadcast Received bit set, terminal error recovery processing procedures shall be initiated.

This mode code is required by Notice 2 for implementation in all RTs. If it is to be used by the system protocol, an appropriate specification should be provided.

Initiate Self Test. The system shall implement this command as specified in 4.3.3.5.1.7.4 of MIL-STD-1553B. Results of the self test shall be available within 100.0 milliseconds. If a failed terminal is identified, terminal error recovery processing procedures shall be initiated. (4.3.3.5.1.7.4, 30.4.4)

If the Initiate Self Test mode command is specified as required, the timing requirement and unique RT responses, as well as the system protocol response, should be included in the MICD.

Transmitter Shutdown. The system shall implement the Transmitter Shutdown mode code as specified in MIL-STD-1553B. It shall be used to shutdown any transmitter designated as failed by the BC.

This mode code is required by Notice 2 for implementation in all RTs. If it is to be used by the system protocol, an appropriate specification should be provided. This mode code is only used in dual redundant systems. It will cause an RT to disable the transmitter associated with the alternate bus from which this command is received.

Override Transmitter Shutdown. The system shall implement the Override Transmitter Shutdown mode code as specified by MIL-STD-1553B.

This mode code is required by Notice 2 for implementation in all RTs. If it is to be used by the system protocol, an appropriate specification should be provided. This mode code is only used in dual redundant systems. It will cause an RT to enable the transmitter associated with the alternate bus, which was previously disabled using the Transmitter Shutdown mode code.

Override Terminal Flag Bit. The system shall not implement the Inhibit Terminal Flag Bit mode code.

If this mode code is used, the MICD should reflect which terminals will respond to it and the conditions under which it is to be transmitted.

Override Inhibit Terminal Flag Bit. The system shall not implement the Override Inhibit Terminal Flag Bit mode code.

If this mode code is used, the MICD should reflect which terminals will respond to it and the conditions under which it is to be transmitted.

Reset Remote Terminal. The system shall implement this command as specified in 4.3.3.5.1.7.9 of MIL-STD-1553B. This mode code shall be issued to all RTs to initiate bus operation (power-up) and may be used in terminal error recovery procedures for a failed RT. (4.3.3.5.1.7.9, 30.4.3)

This mode code is required by Notice 2 for implementation in all RTs. If it is to be used by the system protocol, an appropriate specification should be provided.

Transmit Vector Word. The system shall implement the Transmit Vector Word mode code, to be used in conjunction with the Service Request Bit of the status word, to identify specific aperiodic service requests from the system RTs. The Transmit Vector Word mode code shall be issued within the same minor frame in which the service request was received by the BC.

If this mode code is used, the MICD should reflect which terminals will respond to it and the conditions under which it is to be transmitted. It is typically used in conjunction with the Service Request bit in the status word to signal a service (such as an aperiodic message transfer) required by an RT.

Synchronize (with data word). The system shall not implement the Synchronize (with data word) mode code.

If this mode code is used, the MICD should reflect which terminals will respond to it and should functionally specify the synchronization type (such as time, message table, or minor or major cycle indication synchronization) required to occur.

Transmit Last Command. The system shall implement the Transmit Last Command mode code. This mode code shall be used in the error recovery process.

If this mode code is used, the MICD should specify the conditions under which it is to be transmitted.

Transmit BIT Word. The system shall implement the Transmit BIT Word mode code. As a minimum, all RTs shall provide a Go/No-Go indication. This mode code shall be transmitted to an RT not less than 100 milliseconds after transmission of an initiate Self-Test mode code.

If this mode code is used, the MICD should reflect which terminals will respond to it and should functionally specify the contents of the BIT response and the timing.

Selected Transmitter Shutdown. The system shall not implement the Selected Transmitter Shutdown mode code.

This mode code is not required for dual-redundant systems. Should system redundancy be triple-redundant or greater, this mode code should be used in place of the Transmitter Shutdown mode code.

Override Selected Transmitter Shutdown. The system shall not implement the Override Seiected Transmitter Shutdown mode code.

This mode code is not required for dual-redundant systems. Should system redundancy be triple-redundant or greater, this mode code should be used in place of the Override Transmitter Shutdown mode code.

Undefined mode code. The system shail process an undefined mode code as an illegal command. (4.4.3.4)

Table I of MIL-STD-1553 lists assigned and reserved mode codes. Processing of all other T/R bit/mode code combinations should be specified.

Illegal Commands. The system shall be designed to recognize the illegal commands identified in table 30-VIII. The system shall respond to these commands as required by MIL-STD-1553B. (4.4.3.4)

The illegal commands identified shall include, as a minimum, those mode codes which are reserved and unimplemented. In addition, the table may include those messages which the system is not designed or programmed to operate with.

Table 30-VIII Illegal Commands

Address	Illegal commands	
	Subaddress/mode code field	Mode code number
All	00000, 11111	00000, 00001 01001 to 01111 10100, 10101
00011	000111 to 11101	10110 to 11111
01000	00010, 00100, 01110, 10010, 11000, 11101	N/A N/A

It should be noted that some RTs are not capable of monitoring for illegal commands due to the complexity of the circuitry required to identify an illegal command within the MIL-STD-1553B timing constraints. The BC should be designed so that it can not transmit an illegal command.

Status flags. The system shall implement status bits as specified In table 30-IX and MIL-STD-1553B. (4.3.3.5.3, 30.5.2)

Table 30-IX. System Status Bits

Bit time	Status bit	Requirement
9	Message error bit	Required
10	Instrumentation bit	Always logic zero
11	Service request bit	Required
12-14	Reserved status bits	Always logic zero
15	Broadcast command received bit	Required
16	Busy bit	Required
17	Subsystem flag bit	Required
18	Dynamic bus control acceptance	Always logic zero
19	Terminal flag bit	Required

Table 30-IX reflects the status bits implemented within the system. It may also be necessary to specify the status bit requirements on an RT by RT basis. The system should implement the Notice 2 required status bits, where subsystem capabilities permit. If an RT implements broadcast, self test, or dynamic bus control, then the corresponding status bits should also be specified. The busy bit may only be used in pre-defined circumstances. Also, implementation of the service request bit (typically in conjunction with the Transmit Vector Word mode code) is recommended for RTs that implement time critical asynchronous functions requiring aperiodic service by the BC. Detailed information on the status bits can be found in sections 60.3.1.3 and 60.3.4.4.

Message Error Bit. The system shall implement processing for the Message Error Bit of the status word as specified by MIL-STD-1553B. An indication of a message error shall initiate terminal error recovery processing.

The MICD should specify the processing to be accomplished in the event of an error indication.

Instrumentation Bit. The system shall not implement processing for the Instrumentation Bit of the status word. It shall always be set to zero.

If this status bit is used, subaddresses for the system RTs must be limited to 00000 through 01111. This should be listed in the MICD. Also, the RTs should have the capability to differentiate between the command word and status word through the use of the instrumentation bit.

Service Request Bit. The system shall implement the Service Request Bit of the status word, to be used in conjunction with the Transmit Vector Word mode command to identify specific aperiodic service requests from system RTs. A service request from an RT shall be acted upon within the same minor frame in which the request was received by the BC. The Service Request Bit shall not be used to identify service requests for periodic message transmissions.

If this status bit is used, the MICD should specify whether use of the Transmit Vector Word mode code is implemented, the type of messages for which its use is appropriate, and the time frame in which the request must be acknowledged.

Broadcast Command Received Bit. The system shall implement processing to verify that the Broadcast Command Received Bit of the status word is set following receipt by an RT of a broadcast message.

If this status bit is used, the MICD should specify the system processing required to support implementation of this status flag.

Busy Bit. The system shall implement processing in the event that an RT sets the Busy Bit of the status word. The busy bit shall be set only upon the failure of the RT and/or the associated subsystem, or if data cannot be transferred to or from the subsystem. if a busy condition occurs, system processing shall be determined on an RT-by-RT basis. (4.3.3.5.3.8, 30.5.3)

Any busy condition in the RT or subsystem that will cause the busy bit to be set, affecting communications over the data bus, should be identified. The duration of the busy condition should also be specified, when that condition results from the receipt of particular commands and/or messages by the RT. Notice 2 to MIL-STD-1553B request that specific, predictable conditions be defined that determine when the RT will set the busy bit. The system protocol could treat all busy conditions identically or could be tailored to the peculiarities of each RT.

Subsystem Flag. The system shail implement processing in the event that an RT sets the Subsystem Flag Bit of the status word. if the bit is set, system reconfiguration processing shall be initiated.

If this status bit is used, the MICD should specify the system reconfiguration processing procedure required to maintain a specified operational capability.

Dynamic Bus Control Acceptance Bit. The system shall not implement processing for the Dynamic Bus Control Acceptance Bit of the status word. it shall always be set to zero.

If this status bit is used, the MICD should specify the procedures required to implement dynamic bus control, including the message sequences, timing, and terminal error recovery processing procedures.

Terminal Flag Bit. The system shall implement the Terminal Flag Bit of the status word. The BC, upon receipt of a set terminal flag bit in a status word, shall initiate error recovery processing for the indicated RT channel (4.3.3.5.3.11).

Alternatively, a single terminal flag could be used that does not discriminate between the two channels of a dual redundant RT.

Data Bus Control. Sole control of information transfer on the data bus shall reside with the primary bus controller, which shall initiate all transmissions. In the event of failure of the primary bus controller, the backup bus controller shall automatically assume sole control of information transfer on the data bus.

This general requirement is applicable to all systems that use the "Stationary Master" concept of bus control, with a primary and backup bus controller. A similar requirement should be specified on any system that utilizes any other form of the "Stationary Master" bus control concept. The "Nonstationary Master" bus control concept, where control of the bus is shared among two or more terminals, requires a more detailed specification, including a listing of all potential bus controllers and criteria to determine when control should pass from one BC to the next. Specification of the method of passing bus control from BC to BC, such as the use of the Dynamic Bus Control mode code and the Dynamic Bus Control Acceptance Bit in the status word, should also be included when this bus control concept is utilized.

Positive Response. All communications over the data bus shall be restricted to the transfer modes described in paragraph 4.3.3.6 of MIL-STD-1553B. All information transferred shall be addressed to a specific terminal; in no case shall any terminal to which data are not specifically addressed, except a bus monitor, make use of those data. Bus controllers shall monitor the bus for the purpose of error recovery processing. This mode of operation shall ensure that a positive response is received for all error-free information transfers, thus ensuring that the bus controllers can properly monitor system status.

This specification ensures that all information transfer on the data bus complies with the commandhesponse protocol established by MIL-STD-1553B.

Frame Structure. The frame structure of the multiplex data bus shall consist of a major frame of 160 milliseconds in duration which shall be composed of eight minor frames of 20 milliseconds in duration. Within each minor frame, all data to be transmitted at a 50-Hz rate shall be transmitted at the beginning of the frame. During each odd-numbered minor frame, following the transmission of the 50-Hz data, all 25-Hz data transfer shall occur. During minor frames 4 and 8, following transmission of the 50-Hz data, all 12.5-Hz data transmissions shall occur. All 6.25-Hz data transmissions shall occur during minor frames 2 and 6, in order to evenly distribute the 6.25-Hz data load.

The frame structure of a system should be specified, including major and minor frame time, and transfers to occur in each of the frames. The specified structure shouid accommodate the maximum update rates required for time critical messages, while at the same time providing an adequate schedule reserve for error recovery procedures, system synchronization, aperiodic message traffic, and system growth.

Data format. Digital data shall be transmitted in a format compatible with the word and message formats specified in paragraphs 4.3.3.5 and 4.3.3.6, respectively, of MIL-STD-1553B. The development of data words and message formats shall be in accordance with the guidelines in Section 80 of MIL-HDBK-1553A. Any invalid data transmitted over the data bus shall be indicated as invalid within the same message as the data appears. (4.3.3.5, 4.3.3.6)

This general requirement for message and data word formats should be included for all systems. The guidelines found in Section 80 of this handbook provide for necessary standardization of these formats.

Sample Consistency. Messages transmitted over the data bus shall contain only mutually consistent samples of information. Different words used to transmit muitiple precision parameters, updated at the same rate, shall all be members of the same sample set. Suitable buffering and transmission control logic shall be provided to prevent transmission of a partially updated message that would contain mutually inconsistent data.

This requirement should be included in any MICD for a system that has multiple, time dependent data words to transmit that could be updated while the data is being transmitted on the bus.

Variable Message Blocks. All terminals in the system shall be capable of transmitting a subset of any message defined for it. These subsets shall consist of messages with word counts varying from 1 to the maximum word count defined for the particular message.

This specification provides for tailoring message transmissions to system requirements.

Power Up and Power Down. During power up initialization or power down periods, all RTs in the system shall respond to a valid command in one of the following three ways: RT off-line (no response on the data bus), status word transmitted with the busy bit set, or normaL response. if any data or status words are transmitted from the RTs, the information content of the data or status words must be valid. Simliarly, if any data are received by the RT and passed onto the subsystem, the information content of the data words must be valid.

The response of all the RTs in the system during power up and power down should be specified.

Error Recovery.

Terminal Error Recovery. Upon determination that terminal error recovery processing is required, the active bus controller shall determine if a retry has been accomplished. If a retry has not been accomplished, the command sequence which resulted in the error shall be reinitiated. if a retry has already been accomplished, the active bus controller shall attempt to reinitiate the command sequence on the alternate bus. Once the active bus controller has established error-free communications with the terminai over the alternate bus, the active bus controller shall set the terminal status on the main bus to "terminal failed", and all subsequent communications involving the failed terminal shall occur via the alternate bus.

When an error is detected on the alternate bus, an attempt shall be made by the active bus controller to communicate via the main bus. If errors continue to be detected on both buses, communications will be attempted alternately between the main and alternate buses until communication is inhibited manually or by program control.

Bus Controller Error Recoverv Processing. Upon determination that the active bus controller has failed, the backup bus controller shall assume control of the bus within 100 microseconds of the detection of the failure. The backup bus controller shall resume processing at the beginning of the minor frame during which the failure was detected.

These requirements provide for handling of detected errors. MIL-STD-1553B allows the system designer to select the specific course of action to be taken if errors are detected. The system response to detected errors should be specified in detail.

System Growth Provisions. The system design should allow for growth and flexibility. Consideration should be given to providing spare subaddresses (both transmit and receive), spare data words within used subaddresses, spare frame time in the major and minor frames, and spare capability in the system BC and RTs.

This paragraph provides for the future growth of the system. The growth provisions of the system should be described in detail in a system MICD.

Data Wrap-Around Subaddresses. The system shall impiement a data wrap-around capability and shall reserve a data wrap-around receive and transmit subaddress of 30 (11110). (30.7)

Notice 2 to MIL-STD-1553B requires RTs to provide a subaddress to support the data wrap-around requirement. This paragraph invokes that capability and specifies the subaddress "desired" by Notice 2.

30.5.1.4 Interface Diagram. This section of the system MICD provides an overview of the system data bus interface via a series of functional block diagrams. Each terminal in the system is separately depicted, along with all data bus interfaces to that terminal.

Message Functional Interface Diagrams. Message functional interface diagrams for each system terminal are shown in figures 30-3 through 30-X.

30.5.1.5 System Conventions This section of the MICD describes all conventions specific to the system, such as coordinate systems.

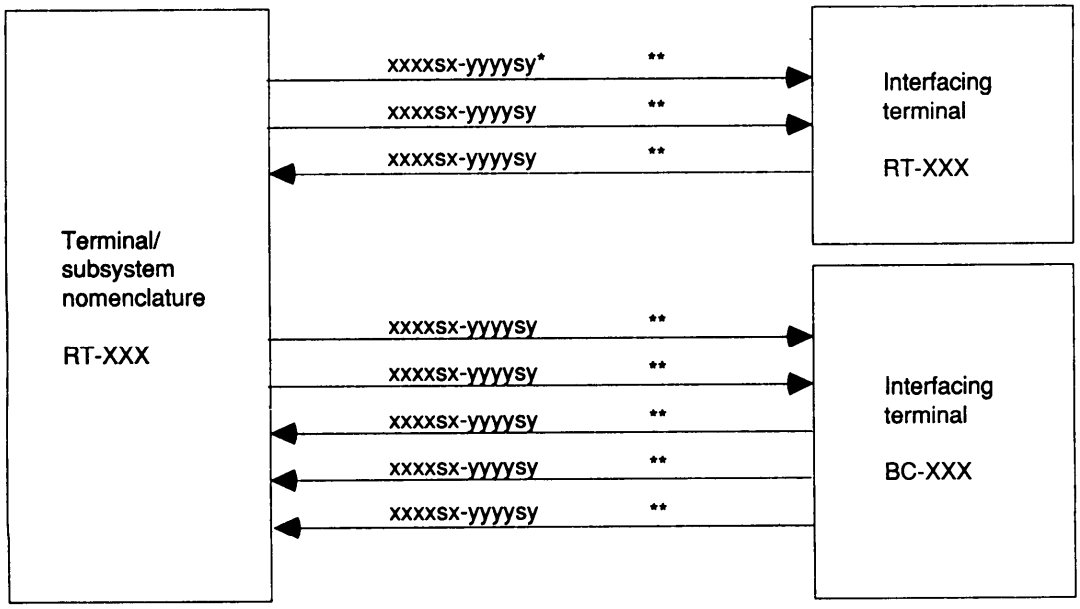


Figure 30-3 Through 30-X. Example Message Functional Interface Diagram

30.5.1.6 Message Descriptions. This section of the system MICD is divided into two subsections, Receive Messages and Transmit Messages, with the messages within each subsection ordered by alphabetizing the message ID (sorting on source and source subaddress within the message ID). Each subsection includes the subset of the RT's entire message set that is required for system operation. A particular RT may have the capability to receive or transmit additional messages which are not represented within the set required by the system - such messages would not appear in the system MICD. Each message is described by a message format ICD presentation sheet, as described in Section 80, followed by a complete set of data word format ICD presentation sheets which detail each word in the message, including the command word(s), data word(s), and status word(s), as appropriate.

30.5.2 MICD Data Base. The MICD Data Base is a tool designed to assist the user in creating, updating, and storing MIL-STD-1553B MICDs. It can be accessed via telecommunications, allowing the user access to files containing the standard data word and message presentation sheets, which can be copied into the user area and customized to the particular system or subsystem being described. An Optical Character Read (0.C.R) capability is also available, which allows the user to scan existing documents into the database file. Once an MICD exists in the data base, it can be viewed by all users, but only updated by users with proper authorization.

For further details, including information on how to access the data base, contact:

U.S. Army Aviation Systems Command (AVSCOM)
Life Cycle Software Engineering Office
Avionics Division (AMSAV-WE)
Building 2525
Fort Monmouth, NJ 07703-5000

SECTION 30 INDEX

SECTION 40

MEDIA DESIGN

CONTENTS

Paragraph

FIGURES

40. MEDIA DESIGN

40.1 INTRODUCTION. A MIL-STD-1553B system consists of remote terminals (RTs), bus controllers (BCs), bus monitors (BMs) and the media that interconnect the terminals. Section 50 discusses the requirements and considerations associated with terminal design. This section discusses the design requirements and considerations for interconnecting the terminals. The basic medium for MIL-STD-1553B (referred to as 1553B in this discussion) communications is two-conductor, twisted, shielded, jacketed transmission cable. Along with the cable, there are transformers, resistors, and connectors that make up the set of media available to the designer. These media are assembled to forma properly terminated bus with terminal connection ports called stubs. This is the bus network.

The most important network aspect is its ability to transmit data waveforms with minimal distortion. This aspect is the waveform quality and is discussed in paragraph 40.9. The purpose of section 40 is to give the reader the knowledge to design and build a MIL-STD-1553B bus network that will workorto analyze one that already exists. This will be done by providing the tools necessary to simulate or model the bus networks to determine waveform quality. Topology effects on waveform or quality will also be discussed, along with how to minimize distortion. Models will be discussed using ideal transmission line theory and will be extended to include losses and other real effects on voltage waveform quality.

Paragraphs 40.3, 40.4 and 40.5 provide a description of MIL-STD-1553B networks, the waveform type used and the components that make up the network. They are intended to give the reader a basic understanding of what a network is and the type of coding used. Paragraphs 40.6, 40.7 and 40.9 are a discussion on distortion sources, rules for evaluating a network and waveform quality. These are included to show causes and calculation of distortion as well as its effects on waveform quality. Most of the material in these sections assumes a background in transmission linetheory. Paragraph 40.8 discusses network simulation. Paragraph 40.10, which sets out the design guidelines, is written in nontechnical language. The design guidelines are for the network designer who is seeking a brief set of suggestions that will aid in designing a network that will have the least likelihood of problems.

Note that, throughout section 40, paragraph numbers in parentheses refer to MIL-STD-1553B, dated 21 September 1978. Wherever Notices 1 and 2 to MIL-STD-1553B apply, they are referred to explicitly at the point of reference.

DEFINITIONS.

1553, 1553A, and 1553B-These numbers will be used throughout the remainder of this section in place of MIL-STD-1553 (any version), MIL-STD-1553A, and MIL-STD-1553B, respectively.

Bus- The term bus is used when talking about the network in general. For this discussion, it is used to refer to the part of the network that is terminated in its characteristic impedance and to which stubs are attached (see figures 40-1 and 40-2).

Characteristic impedance—Z_0-The characteristic impedance of the cable used to build the network is referred to as Z_0. It is usually specified at a certain frequency (1.0 MHz in 1553B, paragraph 4.5.1.2). Z_0 is approximately equal to the square root of L/C, where L is the inductance per unit length of the cable and C is the capacitance per unit length of the cable.

Bus coupler— The circuit which is used to couple signals between the main bus cable and transformer coupled stub cables. A single stub bus coupler consists of a transformer, two isolation resistors, and a shielded enclosure. Multiple stub bus couplers are also commercially available.

Dispersion- Dispersion is transmission line effects on lossy transmission lines on propagating waveforms. It is a result of frequency-dependent velocity and frequency-dependent attenuation which distorts the propagating wave.

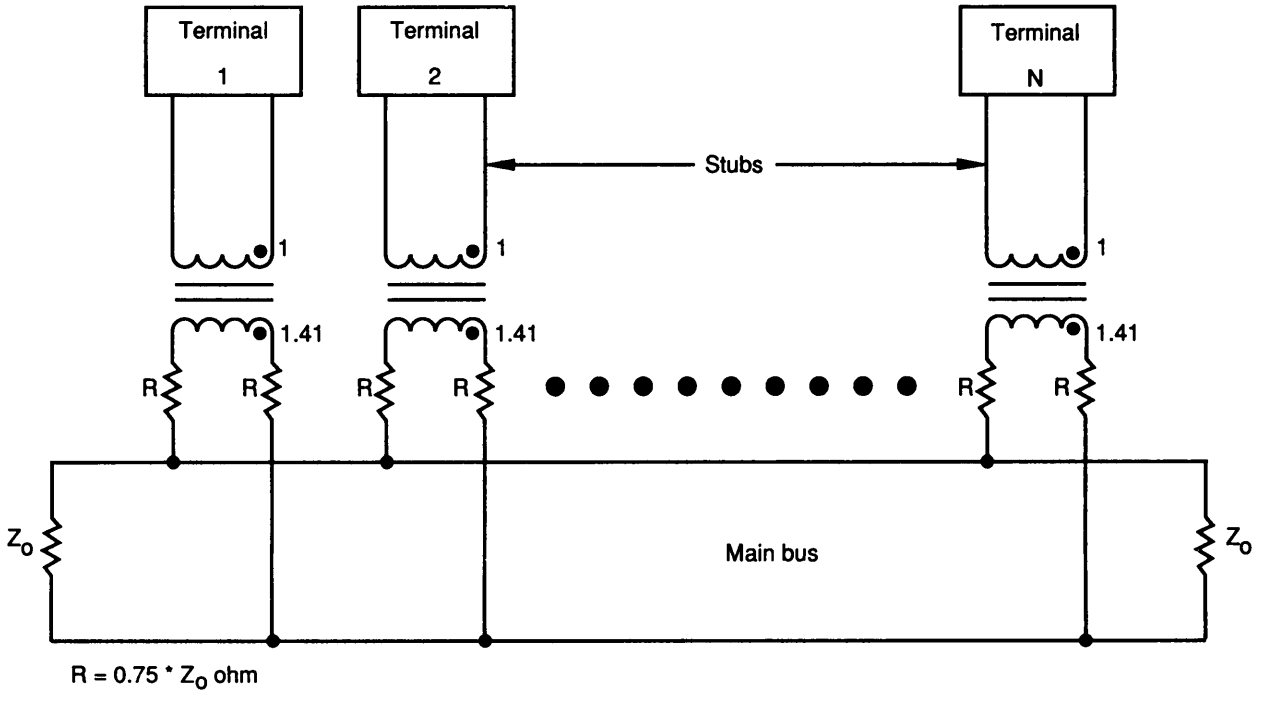


Figure 40-1. Transformer-CoupledNetwork(Bus)

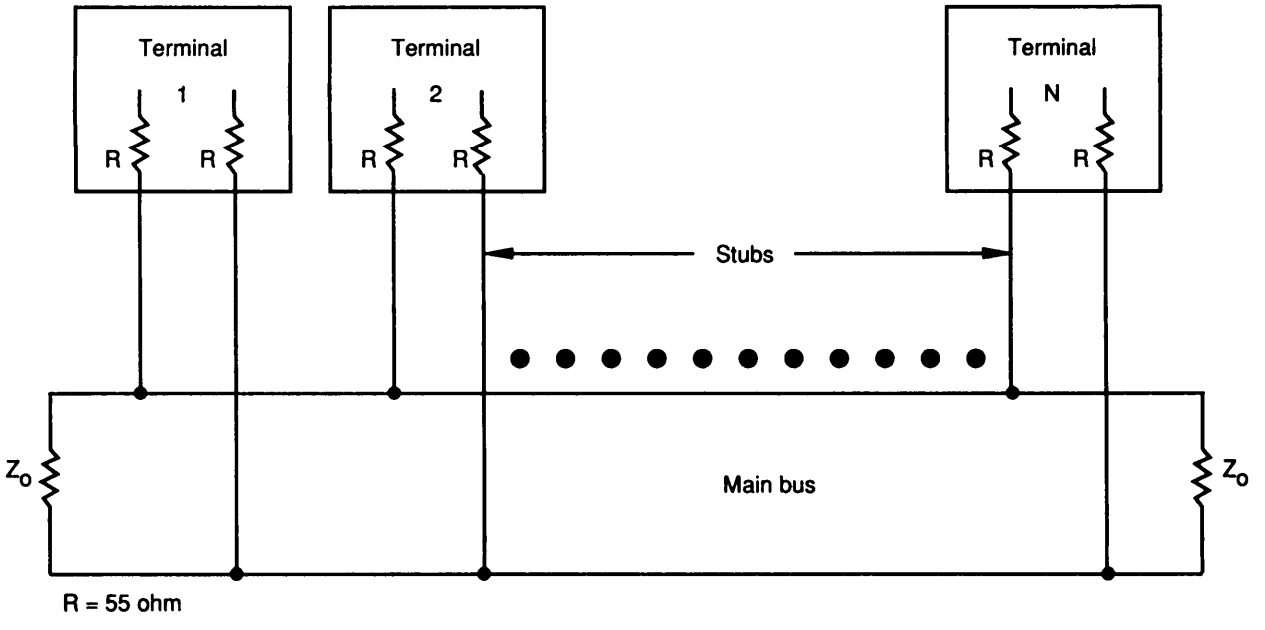


Figure 40-2. Direct-Coupled Network (Bus)

Droop-The exponential decay of voltage across an inductor is called droop.

Fundamental waveform—in this document, the fundamental waveform is defined as the original impinging waveform, the waveform transmitted.

ISI -Intersymbol interference (ISI) is the effect seen where a waveform is distorted by passing it through a network which either has less bandwidth than the signal, or is dispersive.

Lossy -in the context of lossytransmission line, the term lossy acknowledges the fact that transmission lines do not have infinite bandwidth and contribute to frequency shaping of a propagating pulse above and beyond ideal reflective effects.

Main bus -in this discussion, main bus is another term used when referring to the bus part of the network (see figures 40-1 and 40-2).

Network -A network is a collection of connectors, cable, transformers, and resistors used to connect a group of terminals so they can communicate. The term is used interchangeably with the word bus.

Reflection coefficient -The ratio of the voltage wave reflected back toward the source over the duplicate phrase incident voltage wave at an impedance discontinuity (referred to in this document by its abbreviation CR). The value of the reflection coefficient will be between -1 and +1. This is a complex term and will be limited to values within the unit circle.

Stub -The terminal connection to the main bus. It is usually kept as short as possible to minimize distortion, and it maybe either director transformer coupled (see figures 40-1 and 40-2).

Terminal -A transmitter or receiver connected to the end of a stub is called a terminal.

Twisted, shielded pair -A twisted, shielded pair of wires is used to interconnect the elements of a network (transformers, resistors and connectors). It is the primary constituent of the network and is commonly referred to as cable.

Transmission coefficient -The ratio of the voltage wave transmitted beyond an impedance discontinuity over the incident voltage wave (referred to as CT in this document). It is a number between 0 nd 2.

Waveform quality —Waveform quality refers to the amount of distortion with which a waveform arrives at the receiver.

40.3 NETWORK DESCRIPTION. Asystemthat uses 1553B requires separate terminals because of practical limits on the ability to consolidate functions. The functional and physical parameters of each terminal, as well as the system and subsystems serviced, determine where each terminal must be located. This dictates where conductors run between terminals to permit data transfer and system operation and has led to development of data transmission systems. The network consists of the connectors, couplers, resistors, and wires or cables (twisted, shielded pairs) that connect all terminals that communicate with each other.

The typical bus network has a main bus cable with attached stub cables. The bus is a properly terminated transmission line that, except for cable losses, does not cause any distortion in the waveforms on the bus. Waveform distortion caused by cable losses is proportional to bus length and is not significant for short networks. Stubs are used to connect terminals to the main bus. When connected, stubs load the main bus, reducing the impedance below its characteristic value. This causes reflections that are a form of distortion. The two primary sources of distortion in a 1553B network are reflections and dispersion. Reflections come from attaching bus couplers and stubs to the bus, and dispersion comes from the lossy effect of the cable.

40.3.1 Stub types. The 1553B standard allows for the use of either transformer-or direct-coupled stubs. Paragraphs 4.5.1.5.1 through 4.5.1.5.1.4 define the requirements for transformer-coupled stubs and

paragraphs 4.5.1.5.2 through 4.5.1.5.2.3 define requirements for direct-coupled stubs. Figures 40-1 and -2 illustrate typical transformer-coupled and direct-coupled networks, respectively. Note that the isolation resistors for the direct-coupled stub are located within the terminal (paragraph 50.5.5 discusses these resistors in detail).

The appendix to 1553B, paragraph 10.5, recommends that direct-coupled stubs be "avoided if at all possible." The preferred method is to use transformer-coupled stubs. However, for Navy applications, Notice 2, paragraph 30.10.5, requires that the terminals have both transformer- and direct-coupled stub connections externally available. Even though the Navy requires both types of connections, "for Army and Air Force Systems, only transformer-coupled stub connections may be used." This Notice 2 requirement does not preclude both types of stub connections from being incorporated in terminals designed for the Army or Air Force.

40.3.2 Redundancy. Terminals on redundant bus networks must be isolated from each other by 45 dB (4.6.1). Based on this, discussions in section 40 consider only a single network. Networks that makeup a redundant set must be evaluated individually.

40.4 MANCHESTER-ENCODED WAVEFORMS. The coding format used in 1553B communications is Manchester II hi-phase level coding. It is a differential format determined by positive and negative voltages between the two wires that make up the twisted pair. When there is no signal, there is no differential voltage. This type of coding works on the basis of zero-crossing detection (i.e., the information is contained in the directions of zero crossings that occur at 1 -us intervals, giving a 1 -MHz bit rate). Each valid Manchester bit has a 0.5-us positive portion and a 0.5-us negative portion.

40.4.1 Sync waveform. For the following discussion, refer to figures 40-3 and 40-4. To designate the beginning of a word, an invalid portion of 1553B Manchester coding is sent; this is called the sync (short for synchronize). The sync is made up of two 1.5-us periods (one-and-a-half bit times), one high and the other low. For the sync at the beginning of a command word or status word, the high period comes first followed

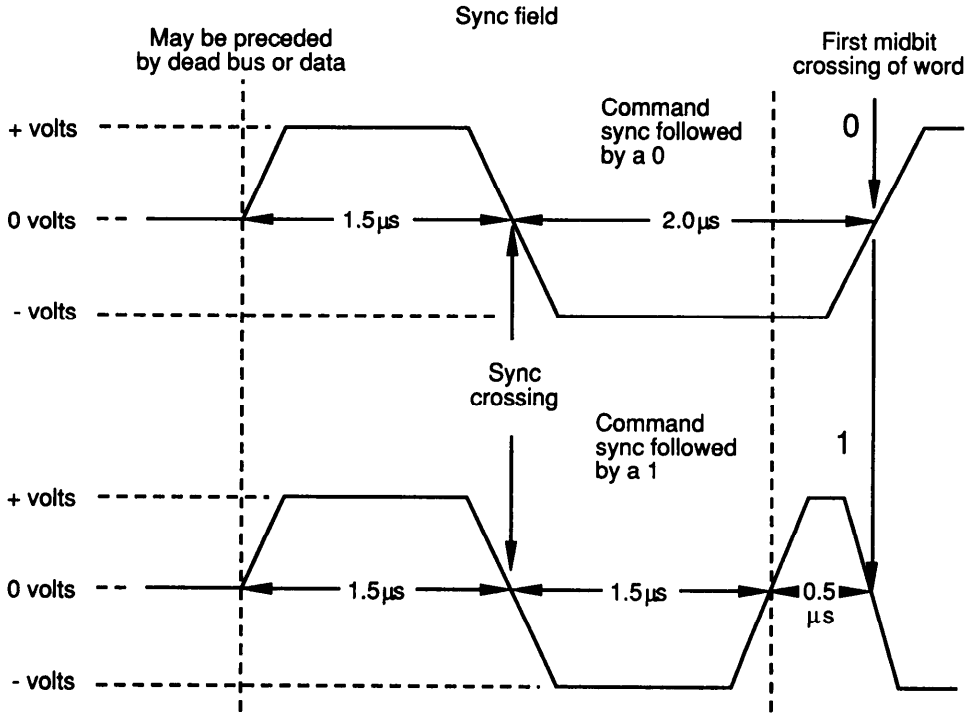


Figure 40-3. Command Status Sync

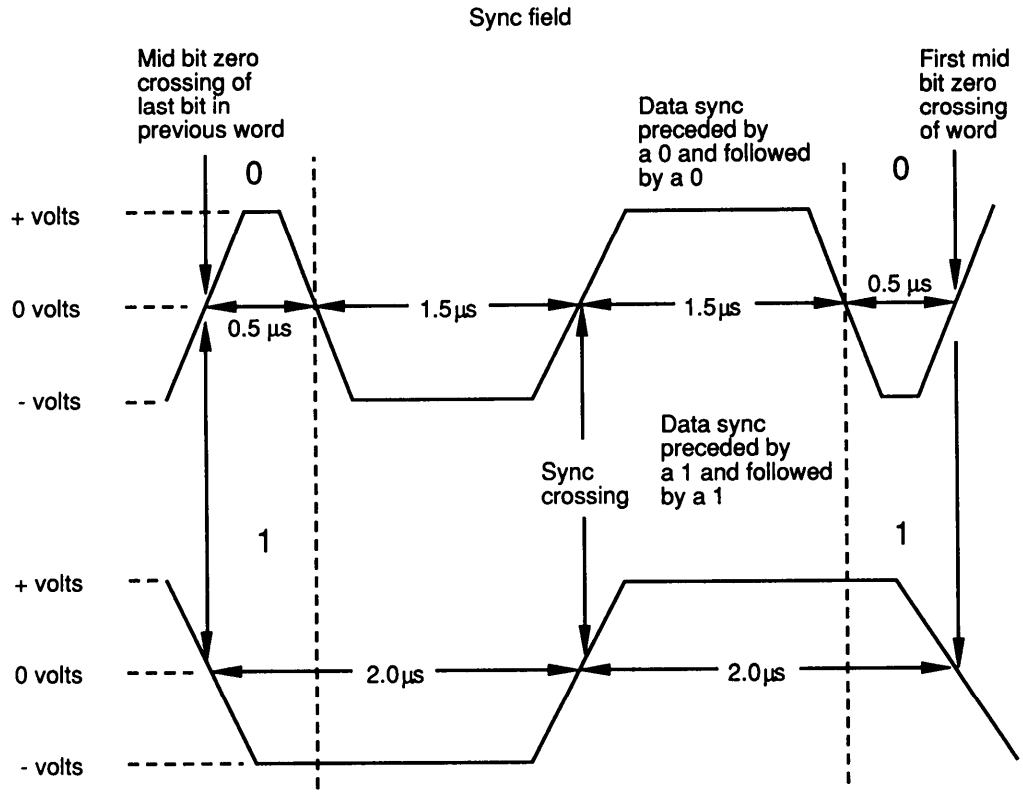


Figure 40-4. Data Sync

by the low period (figure 40-3). The sync at the beginning of a data word is its inverse (figure 40-4). The Manchester code of the sync is considered invalid because there is not a transition within a bit time (1 us). The fundamental frequency of the sync is one third that of the nominal 1 MHz or 333 kHz. When the half bit that is just before or after the sync is the same sign as the adjacent portion of the sync, a 2-us high (or low) period occurs. The fundamental frequency of this portion is 250 kHz.

The 1553B waveforms are asynchronous; that is to say, the terminals in the system have their own clocks and are not synchronized with the bus waveforms at the beginning of a message. To correctly decode data, a terminal must derive the clocking of the received signal. The term sync is used for this purpose. The sync crossing provides the reference from which a receiver-decoder determines the time when the midbit zero crossings of the word will take place. The first midbit zero crossing happens 2.0 us after the sync crossing; subsequent midbit zero crossings occur at intervals of 1.0 us thereafter until the end of the word.

40.4.2 Data bit waveforms. For the following discussion, refer to figures 40-5 and 40-6. According to 1553B, transitions from low to high indicate a zero, and transitions from high to low indicate a one. The mid bit transitions occur normally atone microsecond intervals for a bit rate of 1M bits per second (Mb/s). The name of these transitions is “midbit crossing.” Between bits of the same sense, there are always transitions that occur in the opposite direction of the midbit crossing, these are called “bit edge crossings.”

Sequences of bits of the same sense are said to be “in-phase bits” because they are made up of two consecutive 1-us portions of a trapezoidal 1-MHz wave and have a fundamental frequency of 1 MHz (figure 40-5). A bit that follows one of opposite sense causes a phase change (figure 40-6). This is because the midbit zero crossing is in the opposite direction from the previous, constituting a phase change of 180 degrees, hence, the name “hi-phase”. When a one follows a zero (or a zero follows a one), the waveform will be high (or low) for 1 us. This is a phase change and there is no bit edge crossing. The fundamental frequency for

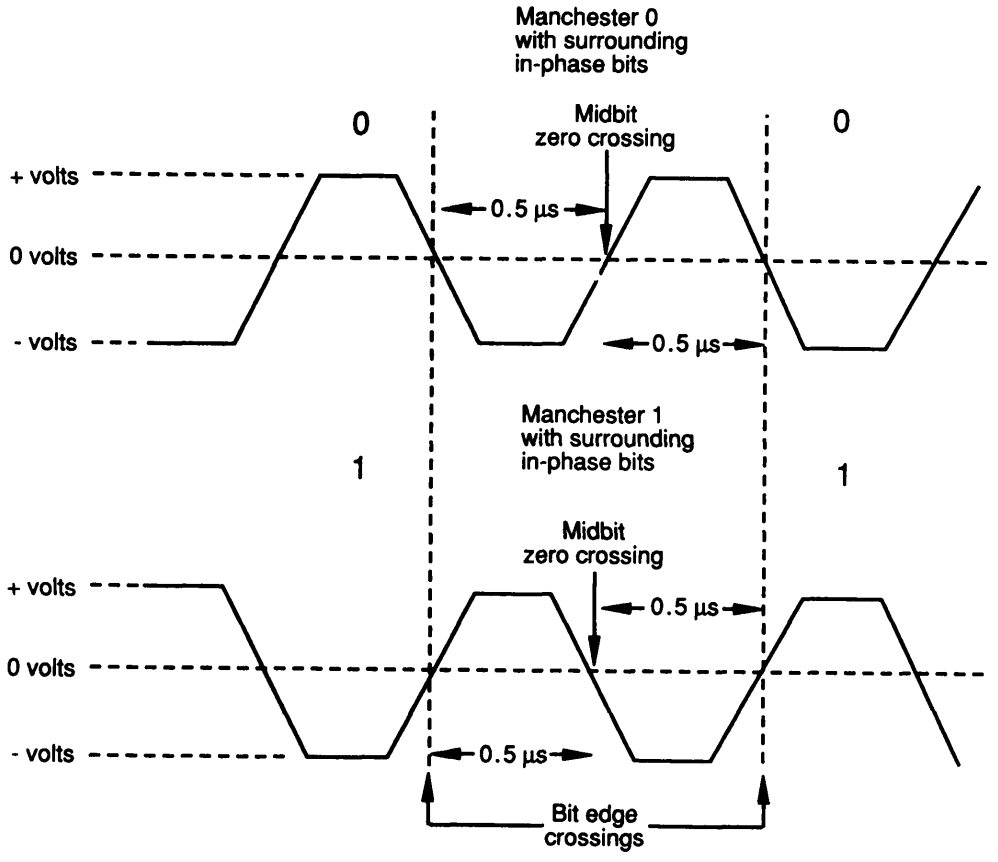


Figure 40-5. In-Phase Bits

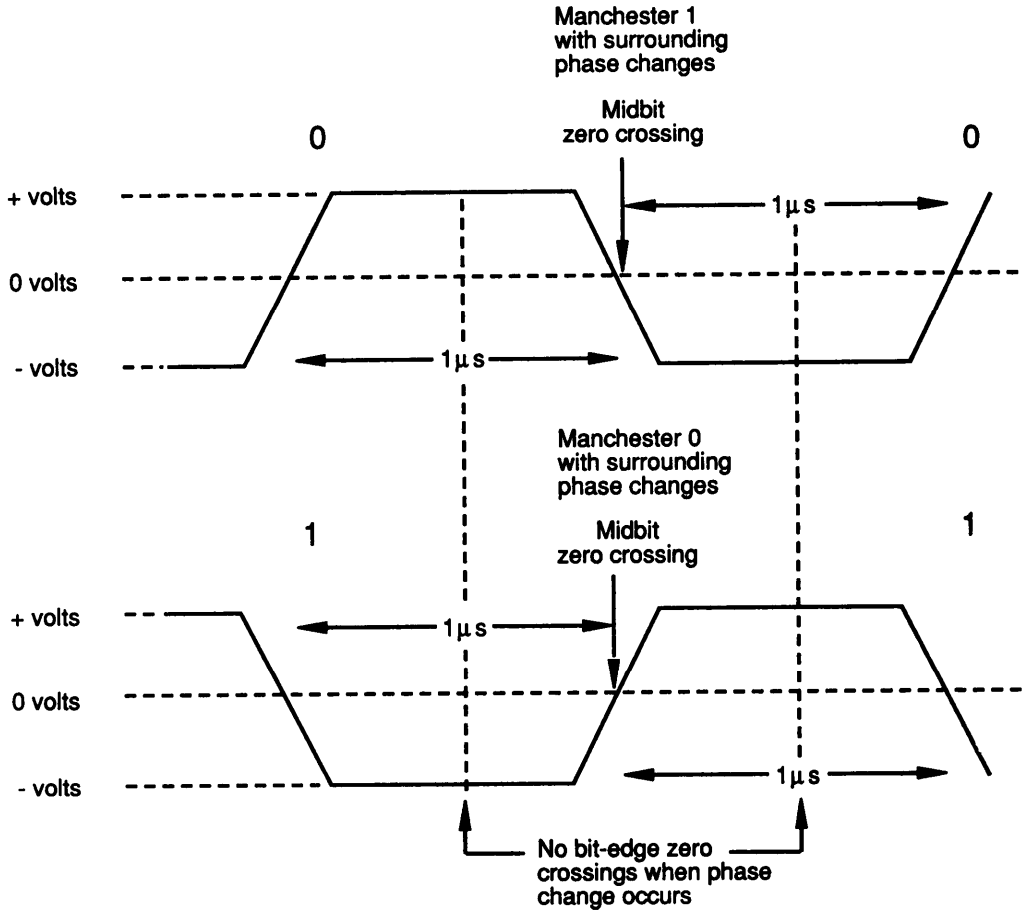


Figure 40-6. *Bits With Surrounding Phase Changes*

this portion of the waveform is 500 kHz, not 1 MHz.

40.4.3 Frequency distribution of MIL-STD-1553B-encoded waveforms. MIL-STD-1553B states that the rise and fall times of waveform transitions (from 10% to 90%) shall be between 100 and 300 nanoseconds (4.5.2.1.1.2 and 4.5.2.2.1.2). This results in a trapezoidal waveform. Specifying a minimum rise and fall time limits the amount of energy at high frequencies. The Fourier components of both a square wave and a trapezoidal wave are shown in figure 40-7. Note that the higherfrequency components of the trapezoidal wave get smaller much quicker than those of the square wave. The following is a comparison of the frequency content of a repeating square wave and repeating trapezoidal shaped wave:

a. If the rise and fall time (transition time) is very small (assume less than 1 nanosecond), 93.4 % of the power is at frequencies less than 6 MHz. At the desired transmission rate of 1 MHz, there is 81 % of the power.

b. If the transition time of this same signal is 150 nanoseconds, more than 99% of its energy is at frequencies less than 6 MHz. The percentage of energy at 1 MHz is 94%.

Increasing the transition time of the waveform reduces the high-frequency harmonics. To reduce the low-frequency content, 1553B waveforms are balanced. Balanced waveforms have a volt-time-product that is equal to zero. Another way of looking at this is that the area of the waveform above 0V is equal to the area of the waveform below 0V. Balanced 1553B waveforms have little low-frequency energy; in a perfectly balanced waveform, there is zero energy at DC.

Networks designed to meet 1553B requirements are band limited. The pass region is approximately from 75 kHz to 1 MHz (depending on the network), and frequencies outside this range will be attenuated. The dominant factors controlling the low-frequency response of the network are the primary inductances of the coupling transformers and terminal isolation transformers. Small inductances cause more low-frequency attenuation. Stub length and placement are the dominant factors in determining high-frequency attenuation. Uneven attenuation of frequency components contributes to pulse distortion that increases the possibility of transmission error. Therefore, controlling the frequency content of the transmitted wave reduces the transmission distortion across the network.

40.4.4 Noise margin of Manchester-encoded waveforms. An additional advantage of the bipolar Manchester waveforms is that the noise margin for a given amount of transmitted power is twice that of a nonbipolar (monopolar) signal. This is explained as follows:

a. The noise margin of a bipolar signal is the sum of two pulse heights: positive and negative. A signal with a noise margin (and amplitude) of 2V has a +1 V pulse and a -1 V pulse for each bit transmitted. Its power is proportional to the amplitudes of its pulses squared, so its power is 1 V squared.

b. To get this same margin (2V) with a monopolarsignal, its pulses need an amplitude of 2V. The monopolar pulses have power that is also proportional to their amplitude squared, or 4V squared. However, monopolar signals will be high only half of the time because a high level (a one) is equally as likely as a low level (a zero). Therefore, the monopolar signals will have transmitted power that is equal to 2V squared. This is twice the power of the bipolar signal.

40.4.5 Advantages of Manchester bi-phase coding. In his textbook “Modern Digital and Analog Communications Systems” (CBS College Publishing, 1983), B.P. Lathi lists five desirable properties for a bus coding system:

a. **Adequate timing content** —it should be possible to extract timing or clock information from the signal.

b. **Efficiency** -For a given bandwidth and transmitted power, the code should have the least errors probability practicable (i.e., the most immunity to channel noise and ISI).

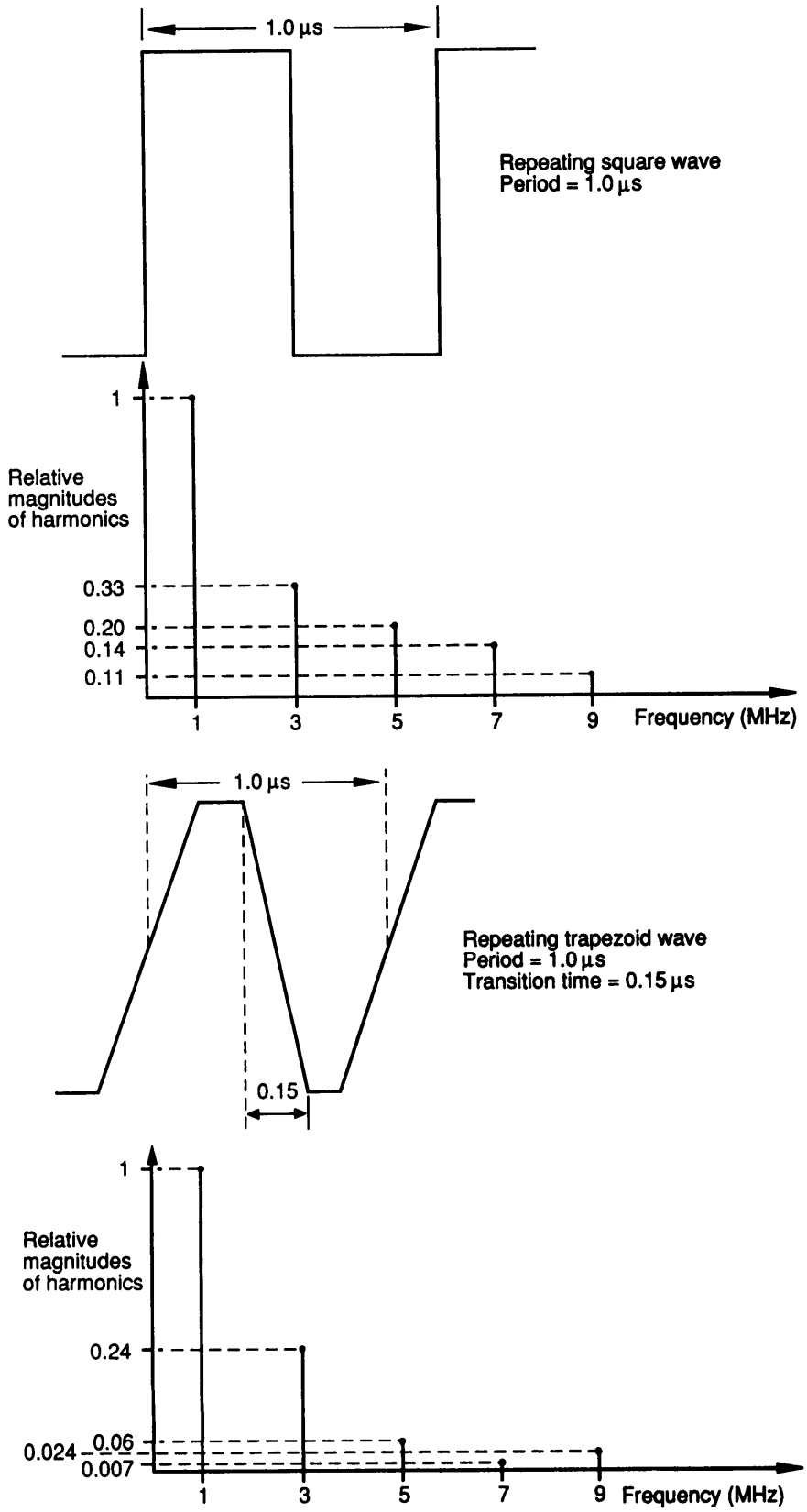


Figure 40-7. Harmonics of Square Wave Versus Trapezoid Wave

c. **Error detection and correction capability** -It should be possible to detect and, preferably correct, errors. In the Manchester hi-phase case, for example, a single error will cause a Manchester violation and can be detected easily.

d. **Favorable frequency content** -The signal frequency spectrum should match the channel frequency response. For example, if a channel has high attenuation at lower frequencies, the signal spectrum should have a small amount of energy in this range to avoid excessive signal distortion.

e. **Transparency** -It should be possible to correctly transmit a digital signal regardless of the pattern of ones and zeros. The code is transparent if every possible sequence of the data bits can be decoded correctly.

Manchester hi-phase coding per 1553B meets the intent of these properties as follows:

Property a, adequate timing content, is met because each sync pulse provides a fresh timing reference point. With each new word, clocks should be desynchronized thus reducing the requirement on long-term clock stability. Additionally, the midbit zero crossings area source for a 1-MHz clock (excluding distortion). This provides timing content.

Property b, efficiency, is rather qualitative. It is, however, sufficient to say that, because the 1553B signal is bipolar, its noise immunity for a given amount of transmitted power makes it quite efficient. Also, because the midbit zero crossings (as opposed to the levels) are used to convey the bit information, there is less time near the threshold and therefore less probability of noise or distortive interference. Assuming sufficient amplitude, only the timing of the zero crossing is important to accurately decode the information from the received waveform.

Property c, error detection and correction capability, is met by the fact that, for a Manchester bit to be valid, it must have half of its time high and half low. If this is violated, or there is so much distortion that the “half-high half-low” ratio is badly skewed, it is easily detectable and can be declared invalid. On the other hand, if the distortion is not excessive, a “smart” decoder is able to determine what the proper value of the bit is supposed to be. This gives Manchester coding a waveform error detection and some limited error correction characteristics.

Property d, favorable frequency content, is met because 1553B waveforms have frequency contents that match the band pass nature of the typical network. Low frequencies are minimized because the signal is balanced. Due to the specified transition time, the amount of high-frequency energy is also minimized.

Property e, transparency, is met for the same reasons that property d is met. Because there is a fresh timing reference for every word (in the sync), all possible bit combinations in a word are decodable. Additionally, each bit is differentiable from previous and subsequent bits because the midbit zero crossing provides timing and positive detection capability. Therefore, the format is transparent.

40.4.6 Transmitted waveforms. MIL-STD-1553B defines terminal output waveform quality in paragraphs 4.5.2.1.1 and 4.5.2.2.1. The specification is defined for the condition when the terminal is driving a resistive load of 70 ohms ±2% for transformer-coupled terminals and 35 ohms ±2% for direct-coupled terminals.

Transformer-coupled terminals require output waveform qualities such as:

a. Output amplitude of 18V to 27V peak-to-peak (4.5.2.1.1.1).

b. Zero crossing within ±25 nanoseconds of nominal, the rise and fall times of the waveform between 100 and 300 ns, and any distortion of the waveform, including overshoot and ringing, not to exceed ±900 mV peak (4.5.2.1.1.2).

Direct-coupled terminals require output waveform qualities such as these:

a. Output amplitude of 6.0V to 9.0V peak-to-peak (4.5.2.2.1.1).

b. Zero crossing within ±25 nanoseconds of nominal, the output rise and fall times of the waveform between 100 and 300-nanoseconds, and any distortion of the waveform, including overshoot and ringing, not to exceed ±300 mV (4.5.2.2.1.2).

There is a relationship between the output characteristics of direct-coupled and transformer-coupled terminals. The zero-crossing accuracy for the two is identical, as are the rise and fall times. Additionally, the output amplitude and the overshoot and ringing requirements are exactly three times greater for the transformer-coupled terminal than forthedirect-coupled terminal. There is a reason for this direct relationship. Due to attenuation across the isolation resistors, only one third of the voltage amplitude transmitted on a transformer-coupled stub propagates onto the main bus (see 40.6.2.4). All of the voltage amplitude transmitted on adirect-coupled stub propagates onto the bus (see 40.6.2.4). Therefore, both transformer- and direct-coupled stubs produce main bus voltages with the same characteristics.

When a terminal is connected to a network, waveforms will be different because the impedance seen by the terminal will not be exactly 70 or 35 ohms and it most certainly will not be completely resistive. The stub load driven by the transmitter is typically resistive and capacitive and causes distortion that is dependent on transmitter output impedance characteristics. Also note, in the transformer coupled case, that the leakage inductance of the coupling transformer will also contribute to overshoot and ringing. Most commercially available devices are designed to work in this environment and will show l“htle distortion at the transmitter output. Section 50 discusses various transmitter types.

40.4.7 Received waveform. The quality of the waveform that aterminai must receive and interpret correctiy is aiso defined in 1553B. Paragraphs 4.5.2.1.2.1 and 4.5.2.2.2.1 specify thevoitage range to which a terminal must respond: 0.86V to 14.0V peak-to-peak for a transformer-coupied terminal and 1.2V to 20.0V peak-to-peak for a direct-coupled terminal. Terminals of both kinds are required to correctly decode received waveforms with up to ±150 nanoseconds of zero-crossing distortion in them. The shape of the received signal may vary from a sine wave to a square wave.

Zero-crossing distortion is defined as the amount of deviation from ideal (with respect to the previous zero crossing) that sync, bit edge, or midbit crossings may exhibit. These crossings are nominaily 0.5, 1.0,1.5, or 2.0 us apart depending on which part of the word is looked at and the data pattern. Paragraphs 40.7.2.3 through 40.7.2.6 and 40.8 discuss the sources of zero-crossing distortion.

40.4.8 Network distortion. Paragraphs 40.4.6 and 40.4.7 defined the absolute limits of distortion that the network may cause and the system function. it may not distort an output waveform any more than it will prevent this waveform from meeting the input requirements. Quantifying the effect of the network on transmitted waveforms wiil be discussed in paragraph 40.7.

40.5 DATA BUS COMPONENTS

40.5.1 Cable. Paragraph 4.5.1.1 of 1553B says the cable shield shali provide a minimum of 75% coverage. Notice 1 to 1553B increased the shielding requirement from 75% to 90% for Air Force applications (Notice 1, 20.4.1), and Notice 2 made 90% shielding coverage a triservice requirement (Notice 2, 30.10.2). The characteristic impedance of the cable shall be within the range of 70.0 to 85.0 ohms at a sinusoidal frequency of 1.0 MHz (4.5.1.2). Notice 2 to 1553B also tightened up the language and stated that, “the actual (not nominal) characteristic impedance of the data bus cable shall be within the range of 70.0 ohms to 85.0 ohms at a sinusoidal frequency of 1.0 MHz” (Notice 2,30.1 0.4). At 1.0 MHz, the cable power loss shall not exceed 1.5 dB per 100 ft. (4.5.1.3).

40.5.2 Terminating resistor. The two ends of the data bus shail be terminated with a resistor equal to the selected cable nominal characteristic impedance (Z_0) ±2% (4.5.1 .4). This means that the nominal value for the cable must be obtained (presumably from the manufacturer) and the terminating resistor selected accordingly.

40.5.3 Stub-coupling transformer. Paragraphs 4.5.1.5.1.1, 4.5.1.5.1.1.1, 4.5.1.5.1.1.2, and 4.5.1.5.1.1.3 define the requirements for the stub-coupling transformer. In summary, they state that the transformer turns ratio must be 1:1.41 ±3% (polarity and turns ratio as shown in figure 40-1). It is also required that:

a. Input impedance on the bus side shall be greater than 3000 ohms over the frequency range of 75.0 kHz to 1.0 MHz (4.5.1.5.1.1.1).

b. Output droop shall be less than 20% and that overshoot and ringing shall be Iess than ±1 V (4.5.1.5.1.1 .2).

c. Common-mode rejection ratio must be greater than 45 dB at 1.0 MHz (4.5.1.5.1.1.3).

Note that once a transformer is installed in a bus coupler, it may not be possible to directly verify its compliance with requirements. Since the coupler may contain isolation resistors or may have several transformers connected in parallel (as in the case of a multi-port coupler), the test circuit is not the same as that called out in the test. The difference in circuits must be considered when evaluating couplers.

40.5.4 Fault-isolation resistors. Fault-isolation resistors are placed in series with each stub connection to the data bus. For the direct-coupled stub, as described above, these resistors are located in the terminal and must have a value of 55 ohms ±2% (4.5.1.5.2.1). For transformer-coupled stubs, the resistors are inserted at the coupler between the transformer and the bus, as near to the bus as possible. The resistors for the transformer coupled case must be 0.75 times the characteristic impedance ±2% (4.5.1 .5.1 .2). Thus, for a direct-coupled terminal, if a fault occurs such that there is a short on the terminal side of the fault-isolation resistors, an impedance of 110 ohms will be connected to the bus. For a transformer-coupled stub, if a fault occurs such that there is a short at the terminal or on the stub, an impedance of 1.5 times Z_0 will be connected to the bus. An obvious advantage in the way the transformer-coupled case is connected is that the whole stub (including the terminai) is fault isolated. In the direct-coupled case only the terminal is isolated, a short on the stub cable would short out the bus and render it useless. Greater bus vulnerability is a prominent factor in the restriction of direct coupled stubs to one foot in length (4.5.1.5.2).

40.5.5 Connectors. MIL-STD-1553B does not specify the type of connector used to interconnect cables that make up a network. Notice 2, paragraph 30.10.3, however, specifies that,"for applications that use concentric connectors or inserts for each bus, the center pin of the connector or insert shall be used for the high (positive) Manchester hi-phase signal. The inner ring shall be used for the low (negative) Manchester hi-phase signal." There are currently two types of connectors in general use. The first is the multipin connector that comes in various styles including circular, rectangular, and rack and panel. The second type is the discrete concentric triaxial design.

40.5.5.1 Multipin connectors. The multipin connector allows the designer to interconnect the bus or stub lines and additional power and signal lines through a single input-output device.

The traditional method of taking a twisted, shielded pair through a multipin connector is to strip back the braid for a convenient distance (several inches is not uncommon), and untwist the pair. Standard power contacts are then crimped onto the conductors or the pair is soldered onto discrete contacts. The braid is then grounded to the shell or taken through its own contact. This technique requires prudent pin placement and wire routing near the connector to prevent EMI problems arising from adjacent conductors. Though this method is popular for practical reasons, it is discouraged. By removing the braid and untwisting the wires, the network is highly exposed to coupled energy.

The best method for carrying the bus through a multipin connector is to use a triaxial contact. Contacts of this design terminate the twisted pair coaxially and terminate the braid through 360 degrees with nearly 100% coverage.

40.5.5.2 Discrete connectors. Discrete connectors come in various styles with the two most popular being threaded and bayonet. Each of these styles have advantages and disadvantages.

Threaded connectors. An advantage of threaded discrete connectors is that they have a straightforward design that is easy to mate and demate in a wide range of environments. Several designs are available from different vendors but they are not necessarily intermateable.

The two main disadvantages of the threaded design are(1) the need to safety wire the connector for shock and vibration and (2) on some designs, the lack of polarizing or keying to prevent incorrect mating. Safety wiring of connectors is required on many systems especially those subject to high vibration during normal operation. Helicopters are prime examples of high shock and vibration applications that require the use of safety wire to prevent the connector halves from partial demating during flight operation thereby causing intermittent or complete opening of the bus. However, it is often required that the terminal be located in such away that access to the connectors is severely limited. This leads to blind mating of the connector pair and the virtual impossibility of safety wiring the connectors.

Bayonet connectors. To solve some of the shortcomings of the threaded connector, several vendors offer bayonet designs with keying and polarizing capabilities that do not require the use of safety wire for most applications. Two cautions: (1) not all available designs are intermateable and (2) not all available connectors can support the number of keyings required for some systems.

Because these connectors are designed with two, three, and four lug engagement, they can withstand severe shock and vibration without use of safety wire on the connector plug. This allows the connector to be located in less accessible areas of a vehicle.

40.6 SOURCES OF DISTORATION. MIL-STD-1553B defines the bus network to a main bus cable to which stubs are attached and terminals are connected to the stubs. It is desired that the parameters of this network be such that voltage waveforms arrive at different terminals with the least amount of distortion. The major parameters affecting waveform quality are bus length, number of stubs, and locations and lengthsof the stubs. This is the topology. Effects of this topology on waveforms can be approximated by considering a lossless transmission line.

40.6.1 Main bus distortion sources. Typically, most of the length of the network is made up of the main bus. The main bus is a twisted, shielded pair of wires with a characteristic impedance of 70 to 85 ohms (4.5.1 .2). The bus is terminated with a resistor at each end whose value is the characteristic impedance ±2% (4.5.1 .4). Because the main bus is terminated in its characteristic impedance, it has no reflections at either end. As a first approximation, the main bus looks like an infinitely long, loss less transmission line with no signal distortion and only an associated time delay.

Typical propagation delay for the type of cable used in 1553B is 1.6 nanoseconds/ft. Thus, there is a delay between transmission of a waveform and its arrival at either a receiver or an impedance discontinuity on the bus. This delay time is proportional to the distance propagated. Different transmitter-receiver pairs are separated by different lengths of main bus, so they have different propagation times between them. Also, the waveshape is different at the receivers for different transmitter-receiver pairs because reflections will be delayed by amounts that vary with location.

The end-to-end propagation delay for a 100-ft. bus is 160 nanoseconds, which is equal to the average rise time of a 1553B signal. When a signal's propagation delay time is more than 50% of the rise or fall time it is necessary to consider transmission line effects. Because 1553B propagation delays maybe much greater than the rise and fall times, transmission line effects must be considered.

40.6.2 Stub distortion sources. To connect a terminal to the bus, a twisted, shielded pair must be run from a terminal to the nearest and most convenient point on the main bus. The connecting cable is called a stub. As was mentioned in paragraph 40.3.1, there are two classes of stubs: direct and transformer coupled. A direct-coupled stub is connected directly to the main bus (see figure 40-2). A transformer-coupled stub, on the other hand, is connected to the bus with a transformer and two fault-isolation resistors (see figure 40-1).

For the purposes of analysis, in both cases the stub cable is assumed to have the same characteristic impedance as that used for the main bus, even though the impedance is allowed to vary between 70 and 85 ohms. To minimize distortion, it is strongly recommended that all of the cable should have the same nominal characteristic impedance. The cable used throughout the bus and stubs should have the same manufacturers part number.

40.6.2.1 Time domain analysis of stubs. The analysis undertaken here, which keeps track of reflections and time delay is dependent on the cable used and for this discussion has been chosen to be 1.6 ns for every foot traveled by the signal. The advantages of time domain analysis are that it is relatively straightforward in application and fairly intuitive in origin.

Effects of stubs. As mentioned in paragraph 40.6.1, when a waveform is transmitted, there is a time delay between its transmission and its arrival at a point of interest on the network. The time delay is proportional to the distance between the transmitter and the point of interest. The amount of delay is 1.6 nanoseconds for every foot traveled by the signal.

If an impedance which is equal to the characteristic cable impedance is encountered, no reflection occurs because the impedance "looks" like a line of infinite length. If an impedance is encountered that does not equal the characteristic impedance of the line, this is called an 'impedance discontinuity" and a reflection occurs. If the impedance encountered is less than the characteristic impedance, a negative reflection occurs; if the encountered impedance is larger than the characteristic impedance, a positive reflection occurs. In both cases, the transmitted voltage (the voltage that propagates from the discontinuity) is the sum of the incident and reflected voltages. The amount of reflection at a junction is specified by the formula:

$$CR = \frac{Z_L - Z_0}{Z_L + Z_0}$$

where:

CR= reflection coefficient
Z_0 = fundamental line impedance
Z_L = encountered impedance.

It should be noted that the Z_L seen on 1553B buses is always less than Z_0 because it is equal to the cable impedance in parallel with the stub impedance. This is because stubs are connected across the bus in a shunt fashion. The value of CR may be between -1 and +1. The equation for the transmission coefficient (CT) is:

$$CT=1+CR$$

CT times the incident voltage is the voltage that propagates beyond from the impedance discontinuity. Both CR and CT are constants of proportionality. That is, they multiply the incident waveform amplitude to produce the resulting reflected or transmitted wave. If a 1 V wave encounters an impedance discontinuity that has a reflection coefficient of-0.5 (and thus a transmission coefficient of +0.5), a negative reflection will result. The amplitude of the reflection will be -0.5V and will add to the impinging waveform to produce a net voltage of +0.5V, which will continue beyond the impedance discontinuity. Note that voltages on both sides of the discontinuity are equal.

The effect of each type of stub will now be examined in terms of reflection and transmission coefficients.

A shunt impedance occurs wherever a stub is connected because, from other points on the bus, the point of connection is a parallel combination of the stub impedance and the continuing main bus impedance. This produces a lower impedance than the characteristic impedance (see figures 40-8 and 40-9; note that the symbol "//" means the parallel combination of two impedances, e.g., $Z_0//Z_0=Z_0/2$). This will cause negative reflections of impinging waveforms to occur on the main bus.

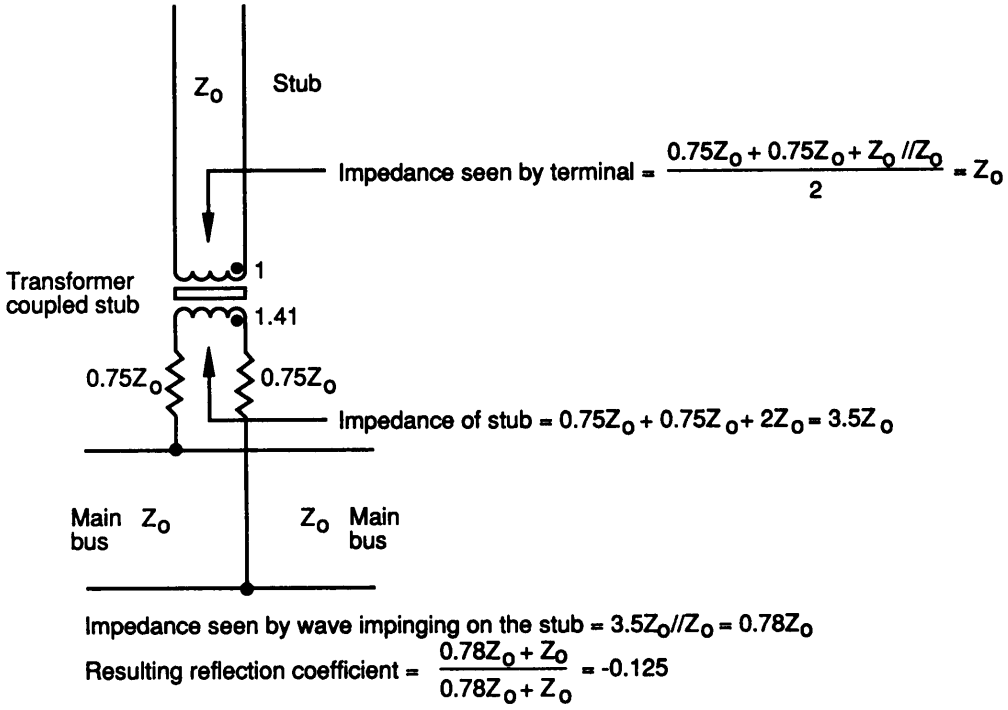


Figure 40-8. Impedance Calculation for Transformer-Coupled Stub

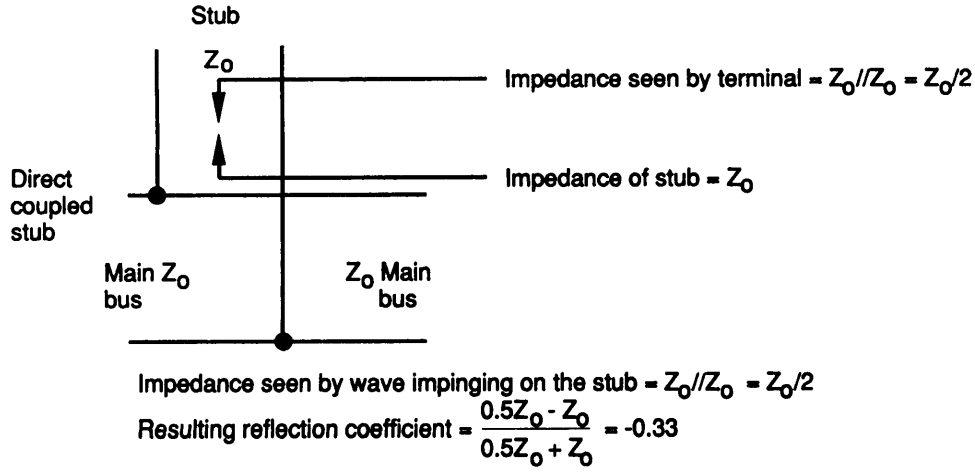


Figure 40-9. Impedance Calculation for Direct-Coupled Stub

In addition, a waveform (with amplitude determined by the amplitude of the waveform impinging on the stub connection and the value of CT) will proceed up the stub from the main bus to the terminal, which presents an impedance much greater than the characteristic impedance. This will result in a substantial positive reflection at the end of the stub (having a value close to +1). The reflection will then propagate down the stub toward the bus and add to the bus voltage according to the value of CT seen from the point of view of the stub. After the transient on the stub is gone, the bus waveform is affected only by the value of the terminal impedance. Assuming that the impedance of the terminal is high (above the specified minimums), positive reflections from stub ends will typically almost cancel out the negative reflections caused by the presence of the stub in the first place when viewed from the main bus.

With the previous considerations in mind, the following can be inferred:

a. Connecting a stub to the bus reduces the bus waveform amplitude.

b. For the time it takes for a waveform to propagate to the end of the stub and back to the bus, the characteristic impedance of the stub cable determines how much effect the stub has on the bus waveform.

c. The amount of time that the transient exists on the stub is proportional to the length of the stub.

d. After the voltage transients on the stub die out, the effect of the stub on the bus waveform is determined by the terminal input impedance.

Direct-coupled stubs. A direct-coupled stub connection is simply a parallel connection of two lines that have the same characteristic impedance. For the following discussion, refer to figures 40-9 and 40-10. A wave propagating along the main bus sees the stub connection as an impedance of half the line impedance (the main line and stub in parallel). Thus,

$$CR = -0.33 \text{ and } CT = 0.67.$$

Thus, when a 3V (for instance) propagating step function encounters a stub, a 2.0V signal will propagate up the stub and beyond the junction. The reflected voltage will be -1 .0V (which, when added to the 3.0V impinging wave, will also equal 2.0V). The voltage transmitted beyond the junction will be absorbed by the terminating resistor that, for this discussion, is assumed to be matched to the characteristic cable impedance. The voltage transmitted up the stub will reflect off the end of the stub with a CR close to +1 (but is actually dependent on the value of Z_o and the input impedance of the terminal). The reflection will then propagate back down the stub and encounter the junction of the stub and main bus (this time from the stub point of view). The coefficients of reflection and transmission are the same as those seen by the initial wave. Thus, 1.3V (3.0 x0.67 x 0.67) will propagate onto the bus and -0.66 (3.0 x 0.67 x -0.33) will be reflected back onto the end of the stub.

The process of reflection, transmission, and re-reflection, etc., will then continue until ail of the transient energy has been absorbed by the terminating resistors. Once reflections die out, the voltage on one direct-coupled stub is equal to the voltage on all other direct-coupled stubs (ignoring losses).

It is important to note that the effect a stub has on the fundamental waveform depends on the rise (fall) time of the waveform with respect to the stub length. If the time of propagation from the bus junction of a stub to the end of the stub and back is equal to or greater than the rise time of the fundamental waveform, maximum distortion will occur. This is because the reflection off the end of the stub will not get back to the bus until after the waveform has finished transitioning, therefore the amplitude of the reflection will be maximum. For a stub with a delay that is a certain percentage of the transition time, its reflection distortion will be that same percentage of maximum. For a 1553B waveform, the minimum rise time is 100 nanoseconds. This is equal to the propagation along 63 ft. Maximum distortion will occur on stubs with greater than half that value (or 31.5 ft.). The shorter the stub, the less it will distort the fundamental. This effect applies to both direct- and transformer-coupled stubs.

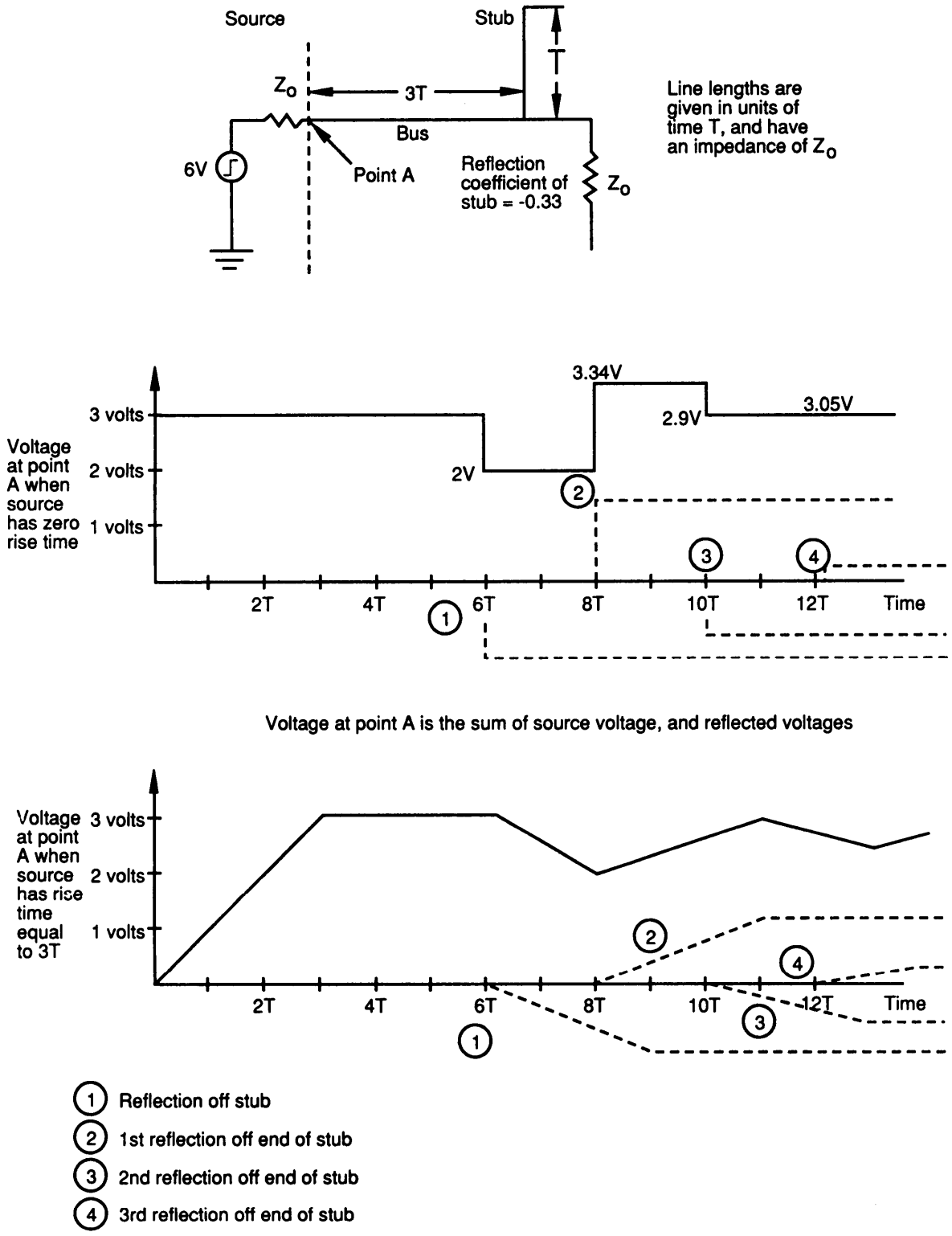


Figure 40-10. Reflective Distortion Caused by a Direct-Ccoupled Stub(Lossless Case)

Because direct-coupled stubs must be less than one foot (4.5.1.5.2), the input impedance of the terminal will dominate their effect on the bus waveform. The input impedance of a direct-coupled terminal is required to be greater than 2000 ohms (4.5.2.2.2.3).

Typically, there is an isolation transformer on the input of the direct-coupled terminal that dominates its input characteristics (see section 50). Because the impedance of a transformer is frequency dependent, the terminal will, in addition to loading the bus, shape the bus waveforms. This shaping contributes to distortion. See paragraph 40.6.4.2, which discusses how transformers interact with bus waveforms.

Transformer-coupled stubs. Transformer-coupled stubs are more complex because they involve both a transformer with a 1:1.41 turns ratio and two isolation resistors. For this discussion, refer to figures 40-8 and 40-11. The impedance that the stub presents to the bus is the series combination of the isolation resistors (two resistors of 0.75 x Z_o ohms) and the impedance of the stub cable transformed through the 1:1.41 turns ratio of the coupling transformer (2 x Z_o). This gives a value of

$$2 \times 0.75 \times Z_o + 2 \times Z_o = 3.5 \times Z_o$$

The stub impedance in parallel with the bus impedance gives a value of $0.78 \times Z_o$, which is a mismatch. This mismatch causes a negative reflection on the bus with a magnitude of 0.125 times the value of the impinging wavefront (CR=-0.125). Using the same rules as above, the voltage that propagates beyond the impedance discontinuity is 0.875 (CT = 1 + CR) times the impinging waveform. Therefore, a 4V wave (for instance) propagating along the main bus will cause -0.5V reflection. The voltage that propagates beyond the discontinuity along the bus will be 3.5V.

Determining the voltage that propagates up the stub is less trivial. Because of the negative reflection caused by the stub, only 87.5% of the impinging waveform is available to propagate beyond the junction. The isolation resistors additionally attenuate the transmitted voltage to 57% of its value at the stub connection. Additionally, this voltage is transformed by the turns ratio giving a net of 1.4V transmitted up the stub (0.875 x 4.0V x 0.57/ 1.41 =1.4V). The reflection off the end of the stub is dependent on the terminal input impedance and will be close to +1. So +1.4V is reflected causing the stub voltage to be 2.8V. The 1.4V reflected wave propagates down the stub toward the bus and gets stepped up through the transformer to 2V. This 2V gets attenuated to 0.5V as it crosses the isolation resistors and is added onto the bus voltage. Thus the voltage reflecting off the end of the stub adds to the bus voltage to produce the original 4V.

Because the terminal input impedance is typically close to the specification minimum, the CR at the end of the stub will be less than +1, so in the above analysis, less than 1.4V will be reflected off the end of the stub. Thus, less than +0.5V will return to the bus, not quite canceling out the -0.5V initial reflection. A net decrease in bus voltage will result. This demonstrates again that the transient loading is determined by the impedance of the stub cable characteristic impedance (as well as the transformer and isolation resistors) and the steady state loading is determined by the terminal input impedance.

It is important to note that the effect that a stub has on the bus waveform depends on the relative length of rise (fall) time versus the propagation time of a wave from the bus to the end of the stub and back to the bus. If the rise time of the waveform is longer than the time it takes for the reflection from the end of the stub to return to the bus, the reflection (off the end of the stub) will be adding back into the bus waveform before it has finished changing. When this occurs, the effect of the stub is reduced proportionally.

Comparison of direct- and transformer-coupled stubs. Direct-coupled stubs present to the bus an impedance equal to the fundamental impedance, thus giving rise to a discontinuity that is half the fundamental impedance. This yields a reflection of -33% for all impinging waveforms. The reflection from the end of the stub then propagates as a positive 44% edge back onto the bus (see figure 40-10).

Transformer-coupled stubs connect an impedance of 3.5 times Z_o to the bus. This results in an impedance of 0.78 x Z_o and a reflection of -12.5%. It also results in a reflection off the end of the stub that propagates as a positive edge of 12.5% onto the bus (see figure 40-11). Due to the smaller perturbations and relatively better isolation, transformer-coupled stubs are allowed to be up to 20 ft. long (4.5.1.5.1). Actually, the figure of 20 ft. is only a recommendation, but it is a strong one. Lack of isolation and larger perturbations limits direct-coupled stubs to a 1-ft. length.

The major difference in the level of isolation between transformer- and direct-coupled stubs is that transformer-coupled stubs have isolation resistors at the junction of the stub and bus and thus protect the bus from a short circuit should one happen anywhere on the stub or in the terminal. Direct-coupled stubs, however, have isolation resistors in the terminal, thus leaving the bus exposed to any short circuits that occur on the stub. They protect only against faults in the terminal.

There are, however, drawbacks to transformer-coupled stubs. The addition of the transformer to the circuit reduces the effective inductance of the stub because there are now two transformers in parallel: the coupling transformer and the terminal isolation transformer. This causes more droop on the bus. Droop is a form of waveform distortion so it reduces waveform quality. (See paragraph 40.6.4.2 for more on the effects of transformers).

Calculation of the amount of reflection returning from the end of a transformer-coupled stub to the bus showed that 35% of the voltage on a stub propagating toward the bus is seen on the main bus. This is because it is attenuated across the isolation resistors. Similarly, it can be said that, when transmitting, 35% of the output voltage of a transformer coupled terminal will get onto the bus. Also, if the terminal input impedance is assumed to be much higher than the cable impedance, 71% of the main bus voltage will be seen on a receiving (non-transmitting) transformer-coupled stub once reflections die out. The 71% is simply a result of the drop across the coupling transformer turns ratio. Thus, 25% (71% of 35%) of the voltage transmitted from a transformer-coupled stub (or reflected from a transformer coupled terminal) gets to any other transformer-coupled stub, neglecting any cable losses. For the same assumption (no cable losses), 100% of the transmitted voltage from a direct-coupled stub arrives at another (receiving) direct-coupled stub. Therefore transformer coupled stub voltages will be lower than direct coupled stub voltages.

Note that, in the analysis of the direct-coupled stub, there were re-reflections of the wave that had reflected off the end of the stub as it reached the junction of the stub and bus. These re-reflections are due to mismatch seen from the stub point of view. In the case of transformer-coupled stubs, however, the analysis ignored any re-reflection of the stub wave back onto the stub. This is because if the turns ratio is assumed to be exactly 1:1.41, the Z_0 of the stub is equal to Z_0 of the bus, and the isolation resistors have a value of exactly 0.75 x Z_0, there won't be any such re-reflection. From the point of view of a wave traveling down the stub toward the bus, a perfect impedance match is encountered at the junction. The isolation resistors (0.75xZ_o each) plus the bus cable in parallel with itself (Z_0/2) equal 2 x Z_0. This, seen through the turns ratio of the transformer, equals Z_o (see figure 40-8). Thus, the isolation transformer does several things for a network:

a. From the bus point of view it increases the impedance of the stub such that CR is smaller and thus there is less bus distortion.

b. From the terminal point of view it matches the transmission of signals from stub to bus.

c. It contributes to common-mode and fault isolation.

As a result of these factors, transformer-coupled stubs are the preferred connection and are numerically much more popular than direct-coupled stubs.

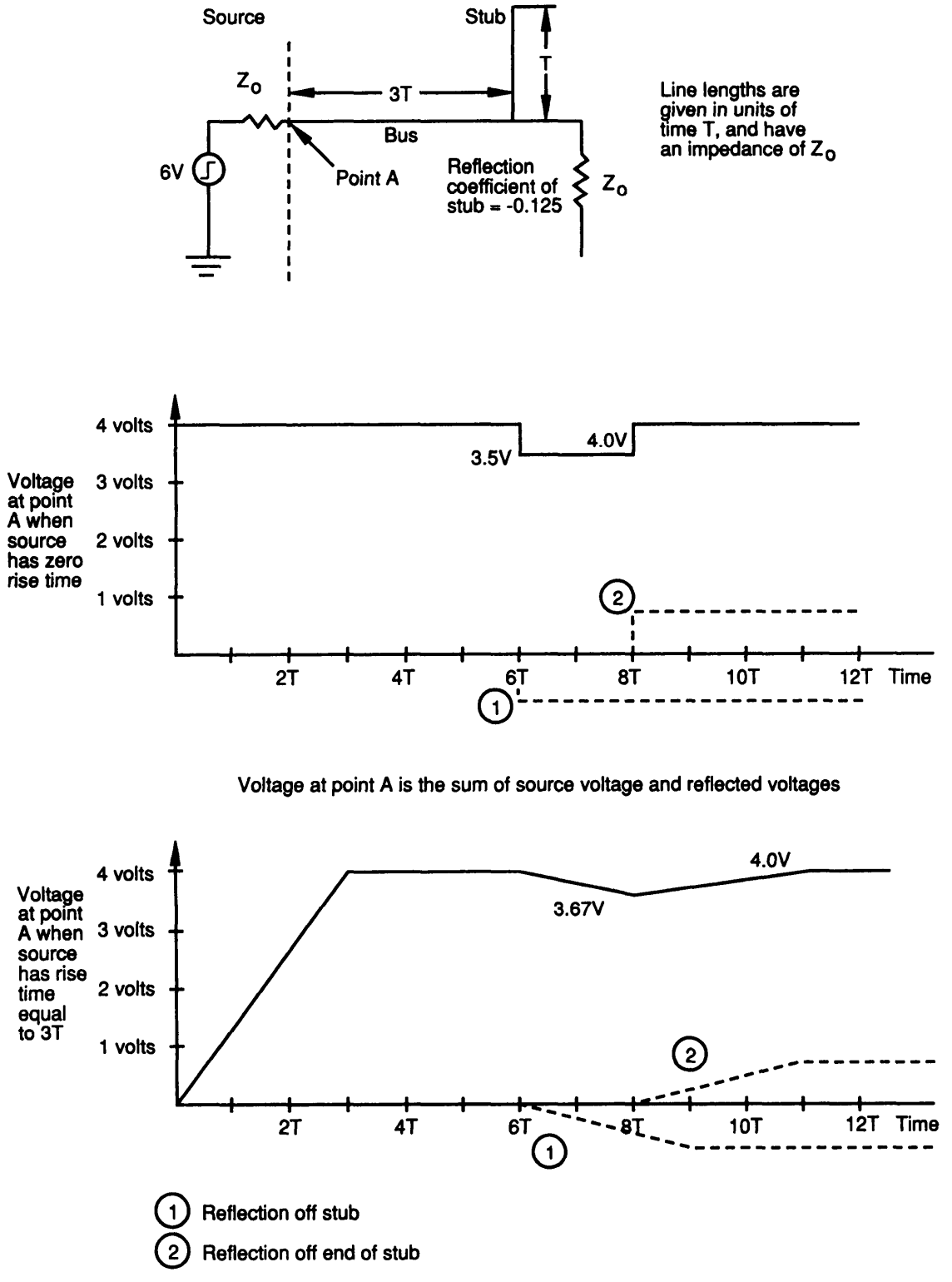


Figure 40-11. Reflective Distortion Caused by a Transformer-coupled Stub (lossless Case)

40.6.2.2 Frequency domain analysis of stubs. Another technique for looking at the effect of stubs on network waveforms is to recognize the fact that the input impedance of the stub can be calculated for a specific frequency. By knowing frequency, wave velocity, cable impedance, and the load connected to the stub, the relationship of the reflected wave to the transmitted wave is known. With this information, the current drawn at a specific voltage can be derived giving rise to an expression for impedance. This is called a frequency domain analysis. To simplify this analysis, only one frequency will be considered, not the continuum of frequencies contained in 1553B waveforms. Figure 40-12 shows the calculated worst case impedances in relationship to the stub length and stub type. The equations and theory used to generate the curves in figure 40-12 can be found in the book, "Applied Electromagnetism", by Liang Chi Shen and Jin Au Kong (Wadsworth Inc. 1983), pages 129-132.

Worst case stub impedance is defined as the lowest value because the lower the stub impedance, the more effect it has on the bus waveform because of a larger CR. Certain worst case assumptions can be made about components and conditions:

a. Excitation frequency is 1 MHz. As frequency goes up, the impedance of a stub decreases as long as the stub is shorter than a quarter wavelength. The quarter wavelength of a 1-MHz signal traveling with a velocity of 1.6 nanoseconds/ft. is 156 ft. Therefore, because there should not be any 156-ft. or longer stubs, the assumption is that stub impedance decreases as stub length increases. Because 1 MHz is the highest fundamental frequency that will be transmitted on the network, it is considered the worst case.

b. Terminal impedance is as low as allowed and completely reactive:-j1000 ohms for transformer-coupled terminals and -j2000 ohms for direct-coupled terminals.

c. Cable used to make the stub has Z_0= 70 ohms (the lowest cable impedance allowed by 1553B).

d. For transformer-coupled stubs, isolation resistors and turns ratio are assumed to be their minimum values. Because these parameters provide isolation from the effects of the stub, minimum values increase the effect of the stub.

Using the values in figure 40-12, the reflection coefficients (CR) for different stub lengths and types are shown in figure 40-13. These are also the worst case for two reasons: (1) the values of the stub impedances are worst case and (2) the bus cable is assumed to have a characteristic impedance of 85 ohms. This causes the greatest reflection (more than it would for 70-ohm bus cable) for a given stub impedance. Notice that the bus cable impedance and the stub cable impedance are assumed to be different, this is the worst case for stub reflection coefficient. Even though it is an extreme assumption (because a network should be made out of cable that is uniform in impedance), it is a necessary one because there is no prohibition in 1553B against using different cable for different portions of the network (as long as the cable used has a Z_0between 70 and 85 ohms).

If there is a fault on either type of stub, the impedance of the isolation resistors is connected to the bus. A short in a direct-coupled terminal will connect a minimum of 108 ohms to the bus; a short on a transformer-coupled stub will connect a minimum of 103 ohms to the bus. These shorts will yield maximum reflection coefficients of -0.28 for a direct-coupled stub and -0.29 for a transformer-coupled stub.

As a way of comparing the two methods for describing stubs, consider that the frequency domain method is a direct subset of the time domain method. The frequency domain method derives the impedance of a stub on the basis of the magnitude and time delay of reflections, but it limits the analysis to a specific frequency. Keeping track of reflections for the time domain method, however, is difficult unless a computer is used (see 40.8.2), so the frequency domain method of stub loading analysis is a good method for first approximations. It should also be noted that the method is a frequency domain representation for stubs, and it may be generalized to many frequencies (if one has a computer to keep track of them) in a frequency domain simulation (see 40.8.2). For a simpler analysis, a single frequency is chosen here.

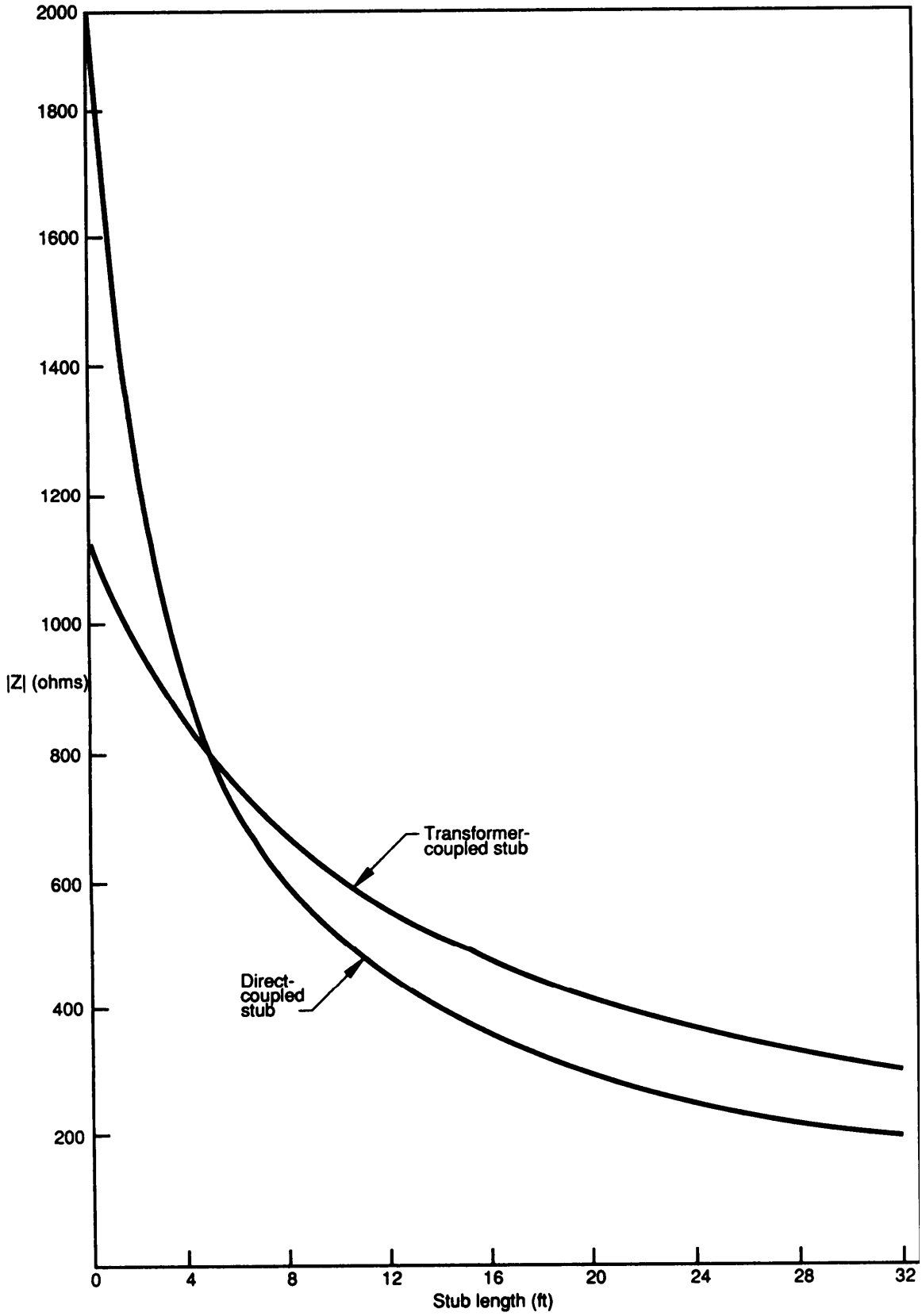


Figure 40-12. Impedance of Stub Versus Their Lengths

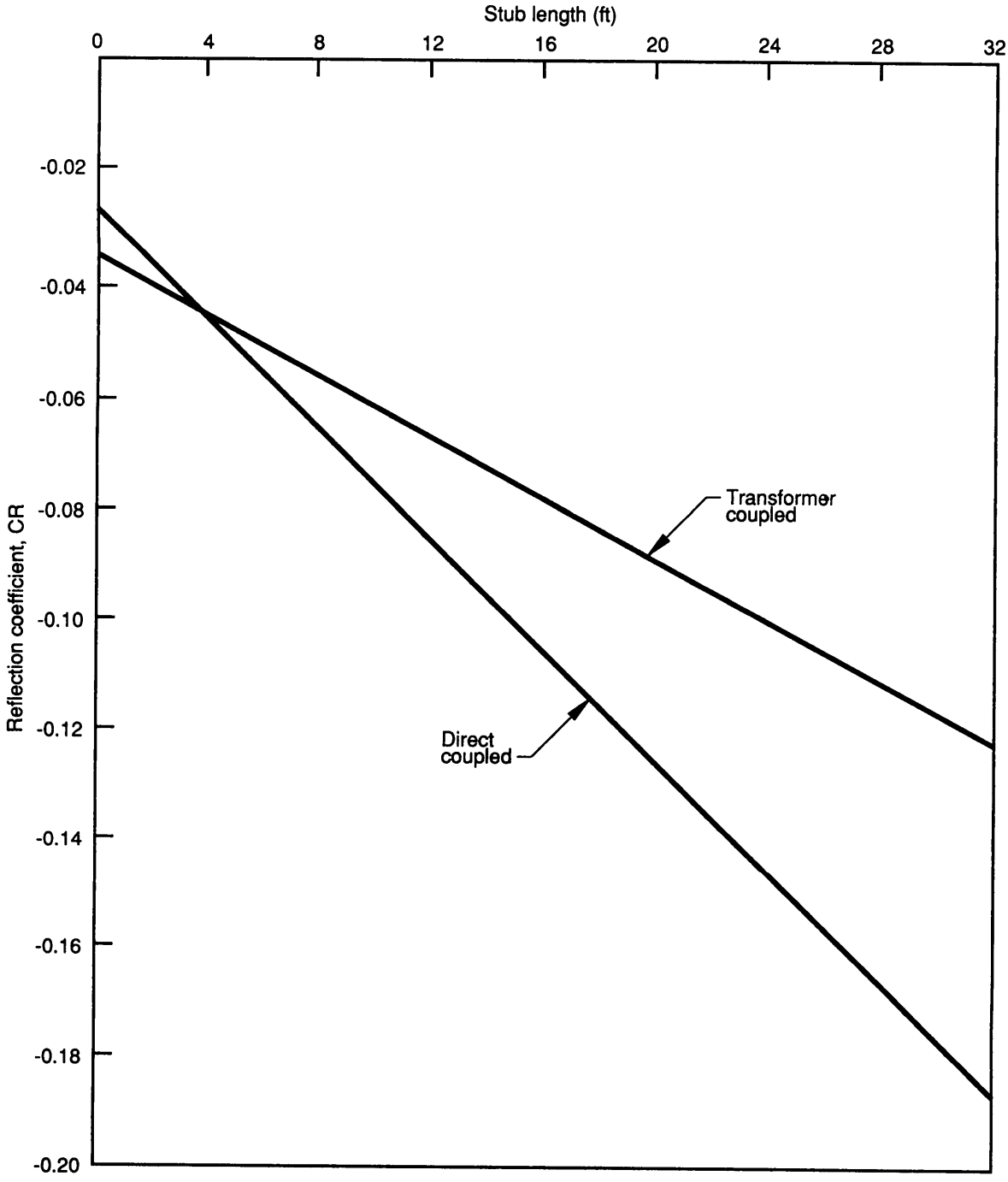


Figure 40-13. CR Versus Stub Length

The assumption that a stub has a single impedance is only an approximation. The stub impedance is a function of frequency, and there are different fundamental frequencies due to different data and synchronized waveforms. Also, because the waveform is not sinusoidal there are harmonics of the fundamental. Therefore, the effect of the stub on a waveform will not be uniform but will vary with the different frequency contents of different portions of the waveform.

Another way of describing the limitation of the simplified frequency domain stub analysis is to compare stub length and transition time. Any time the length of a stub, in units of time, approaches a quarter of the transition time of the bus waveform, reflections become significant (because the delay from the bus to the end of the stub and back will equal 50% of the transition time). When reflections become a factor, their effects must be accounted for with a more thorough analysis or simulation. The transition times of bus waveforms vary with transmitter type and network configuration, so stating an absolute maximum stub length for which the simplified frequency domain analysis is valid is not possible. As a rule of thumb, when there are stubs in a network that are 20 ft. long or longer, it is necessary to consider whether a more detailed analysis is needed. This is only a first order approximation, for a more accurate representation of the effects of a stub on a bus waveform, the time domain method or the generalized frequency domain method should be used.

40.6.3 Lossy cable. Cable used to build a 1553B network has associated losses, up to now in Section 40, these losses have been ignored. The wires of the twisted pair have resistance and series inductance, and there is shunt capacitance between them. The resistance affects cable impedance and wave velocity, making them both frequency dependent. There will also be frequency-dependent attenuation. The two primary results from these losses are a change in wave shape and an attenuation of the signal.

A lossy MIL-STD-1553B cable filters out the high-frequency components of propagating waveforms thus producing a low-pass effect. This is because the cable losses cause frequency-dependent attenuation and velocity. The dependence on frequency of the losses causes the different pulse widths of a 1553B waveform to be attenuated different amounts and therefore have different amplitudes. Frequency-dependent attenuation also decreases the higher frequency harmonics of the waveform. Attenuation of the harmonics serves to smooth out the propagating waveforms and tends to make an initially trapezoidal waveform look somewhat sinusoidal.

Because the velocity is a function of frequency, a lossy transmission line does not have flat group delay. This results in additional pulse distortion because the phase relationships of the different frequency components change as they propagate. Another intuitive way of viewing the effects of a twisted pair is that some frequency shaping results any time a capacitance is driven by a voltage source that has non-zero source impedance. In other words, the network acts as a low-pass filter to transmitted waveforms.

In addition to changing the wave shape, cable resistive losses uniformly attenuate the signal. The amount of this attenuation is determined by the value of the termination resistor and the resistance per foot of the conductors. Typical resistance for wire used in a 1553B network is 0.026 ohms/ft., so conductor resistance per foot is 0.052 ohms because the current must flow through both conductors in series in order for the voltage to propagate. For a 100-ft. piece of 78-ohm cable (properly terminated), the resistive attenuation is:

$$78/(100 \times 0.052 + 78) = 0.94 \text{ or } 0.6 \text{ dB}.$$

The total loss of the cable is the combination of the two loss components: the uniform attenuation caused by the resistive drop in the wire and the distortion of the waveform resulting from the frequency-dependent attenuation. In general, because the receiver input voltage resulting from typical transmitted voltages is so much higher than the minimum required, the uniform attenuation is not a problem, though it must be considered in network design. Of immediate interest, however, is the amount of frequency-dependent distortion because this changes the wave shape thus directly affecting waveform quality.

40.6.3.1 Frequency-shaping effects of dispersion. We will now look at what happens to a waveform propagating along a perfectly terminated lossy line. For a simple example, a propagating step function will

be examined. When a step voltage is applied to an uncharged piece of cable, a group of voltages at a continuum of frequencies (the amplitudes and phases at each frequency given by the Fourier transform of the step function) begin to propagate. From the information given earlier, it may be seen that the different components have different velocities and amounts of attenuation. Higher frequencies travel faster, but are attenuated more quickly. The result is a traveling wave with its relative amount of high-frequency content decreasing and low-frequency components lagging the higher frequency wavefront by an amount proportional to the distance traveled. This effect is called dispersion.

The waveform when viewed at points along the line begins to look like a step function that has gone through a low-pass filter. As the distance between the point viewed and the source increases, it appears that the rolloff of the apparent filter moves to a lower frequency. In other words, the rise time is increased as the wave propagates. This is a comfortable notion because the lumped-element equivalent model of this type of transmission line looks like a second order low-pass filter.

It will also be apparent that the amplitude decreases with the distance traveled even for the low-frequency components of the step. This decrease is because of cable resistance. The resistive losses of the cable in this case act like a voltage divider such that the voltage level at any point on the bus is dependent on the distance from the transmitter and the connected load.

The rise and fall times (transition time) of a 1553B waveform have both minimum and maximum values specified, so they will not be a step function but will be trapezoidal. Because it has less high-frequency content, the trapezoidal wave will experience less distortion. Over a short distance (10 or 20 ft.), the distortion will show up as the rounding off of the corners of the waveform because these contain the highest frequencies. After propagating a longer distance greater than 200 ft., the signal will be further rounded so that the amplitude of the higher frequency pulses of the waveform will start to be reduced by the shaping effect. Figure 40-14 shows the initially transmitted waveform, the waveform after a short distance, and the waveform after a longer distance. This example shows how dispersion changes the shape of a wave as it propagates along a cable.

40.6.3.2 Effect of dispersion on zero crossing. A typical 1553B waveform is made up of a mixture of four fundamental frequencies (1 MHz, 500 kHz, 333 kHz, and 250 kHz) plus harmonics. There will be uneven attenuation and nonlinear group delay in addition to the uniform attenuation caused by the resistance losses. These effects cause zero-crossing distortion in a propagating waveform. An understanding of how this attenuation occurs can be arrived at by considering that the rise time of a waveform will become longer as it propagates because the high-frequency energy is being attenuated.

When the rise/fall time becomes longer than the pulse width, the voltage begins to transition before full amplitude is reached. This reduces the amplitude of the signal. For a 1-MHz portion of the signal, when the rise time exceeds 500 nanoseconds it will begin to attenuate. Under these same conditions, a 500-kHz portion of the signal would not suffer any attenuation other than that caused by resistance losses; it would just have longer transition times. Thus, the 1-MHz portion the waveform will be attenuated more than any of the lower frequency portions.

Similarly, for a much longer bus, transition times will exceed 1 µs, and the 500-kHz portions of the waveform will begin to be attenuated with respect to the lower frequency portions. It can be seen that, as bus length increases, first the 1-MHz portions of the waveform begin to attenuate with all other components staying the same relative amplitude (though with longer transition times), then the lower frequency portions of the waveform begin to attenuate. All the while there is uniform attenuation caused by the resistive drop in the cable.

Typically, dispersion is not significant on 1-MHz portions of the waveform for bus lengths less than 200 ft. long. Dispersion is not significant for 500-kHz portions of the waveforms with bus lengths less than 400 ft. For the 1-MHz portion of a waveform, there is roughly 3% to 4% attenuation per 100 ft. traveled with respect to other non-frequency-attenuated portions of the waveform. The uniform attenuation of the resistive losses is typically 6% per 100 ft. for all frequencies.

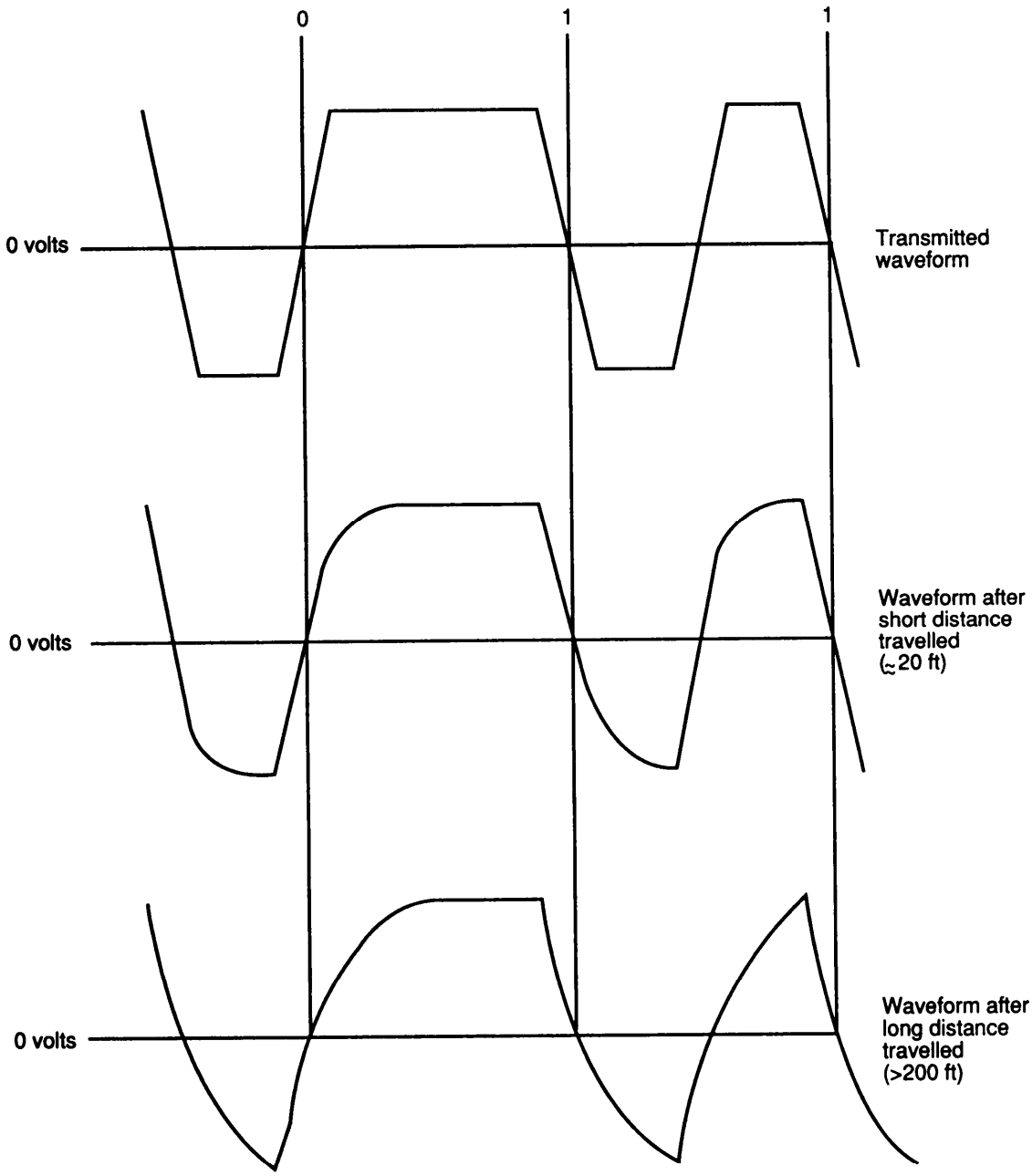
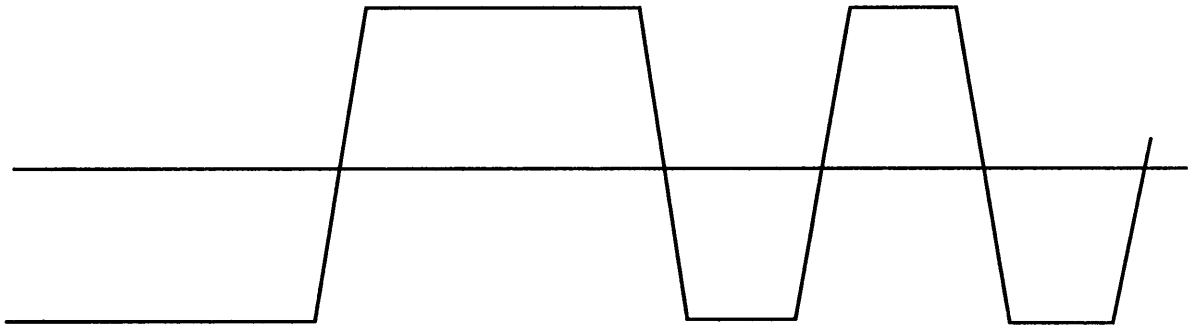


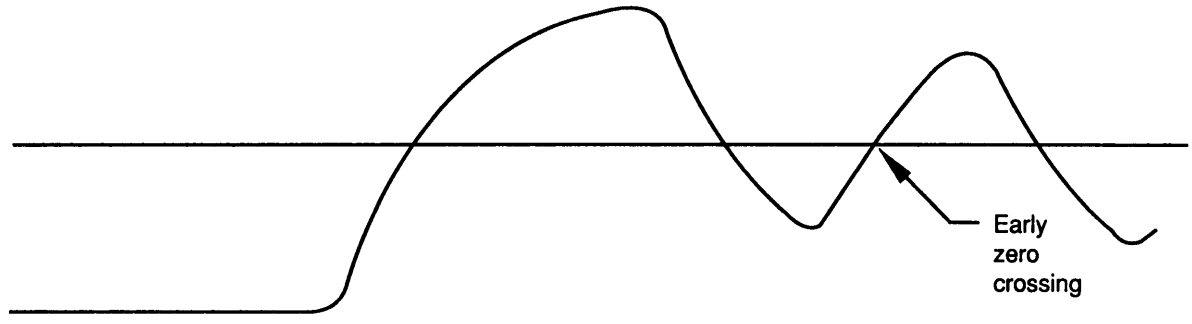
Figure 40-14. Waveform Distortion With Respect to Propagation Distance

Figure 40-14 shows the effect of dispersion on the shape of a propagating wave. Dispersion also causes zero-crossing distortion, figure 40-15 shows an example of this effect. Because dispersion increases the rise time of a waveform, pulses of different widths will end up having different amplitudes after traveling in a dispersive medium. Differences in amplitude of pulses with different fundamental frequency cause a transient voltage offset in the bus waveform. Because the rise (fall) time is greater than zero (it started out as greater than zero and has gotten longer due to dispersion), this voltage offset translates into a zero-crossing deviation.

40.6.4 Stub-coupling transformers. The transformer used to couple the stubs to the bus imposes some of its own personality on the bus waveform. Paragraph 4.5.1.5.1.1 in 1553B directly specifies the type of transformer and the allowable range of its divergence from the ideal. The turns ratio is specified to be 1:1.41 ±3% with the high-turns side connected to the resistors that connect to the bus (see figure 40-1). The input impedance of the transformer, at the high-turns winding, is specified to be greater than 3000 ohms for frequencies between 75 kHz and 1 MHz (4.1.5.1.1.1). The impedance is measured using a 1V RMS sine wave. Transformer waveform integrity is discussed in 4.5.1.5.1.1.2. There it is stated that the droop at the high turns side shall not exceed 20% when the low-turns side of the transformer is driven by a 250-kHz square wave (with a maximum rise time of 100ns) through a 360-ohm resistor. Additionally the amount of ringing and overshoot allowed on the output is to be less than ±1V. The output is defined to be the high-turns side of the transformer. Common-mode rejection (4.5.1.5.1.1.3) for coupling transformers must be greater than 45dB at 1 MHz. The suggested test method is to drive the high-turns side with a common-mode signal and measure the differential output at the low-turns side.



Undistorted waveform



Distorted waveform

Figure 40-15. Zero-Crossing Distortion Caused by Dispersion

Generally, commercially available 1553B transformers do not significantly change the shape of a waveform that goes through them. The primary effect is to change the amplitude. Thus, the waveform on a stub usually has the same shape as the waveform on the bus next to that stub and will only be different in amplitude.

40.6.4.1 Turns ratio. Turns ratio has the following effects:

a. It contributes significantly to the voltage amplitude of the signals transmitted across the network. The voltage passed through the transformer is proportional to the turns ratio. Thus, the transmitted voltage and the received voltage for a given terminal are proportional to the turns ratio of its coupling transformer. Therefore, the amplitude of the waveform transmitted from one stub to another is dependent on the turns ratios of the transmitting and the receiving stub coupling transformers.

b. It determines the impedance the stub presents to the main bus. Loading of the bus by a stub is approximately inversely proportional to the square of the turns ratio. Thus, the magnitude of distortion caused by a stub is dependent on it. Higher turns ratios cause less distortion, but provide lower signal amplitude to a receiving terminal. Therefore, a compromise value must be used; 1.41 to 1 was chosen.

c. It determines how well matched stub-to-bus transmission is, from the stub point of view. The impedance seen through the transformer is dependent on the square of the turns ratio and the actual impedance connected to the secondary. For the selected turns ratio, the isolation resistor values have been chosen such that there is perfect matching when looking from the stub toward the bus.

40.6.4.2 Transformer input impedance. The input impedance of the coupling transformer is specified to beat least 3000 ohms over a specified range of frequencies (4.1.5.1.1.1) when looking into the high-turns side (the side that is connected to the bus through the isolation resistors). This specification then directly controls parameters of the transformer that affect its input impedance.

For simplicity of analysis it will be assumed that, a transformer looks like a shunt capacitor in parallel with a shunt inductor. The value of the capacitance determines the high-frequency input impedance, and the value of the inductor determines the low-frequency input impedance. Using this two-component model, the minimum allowed inductance (on the high-turn side) is approximately 6.4 mH, and the approximate maximum allowed shunt capacitance is 53 pF (when looking into the high-turns side). These are worst case values for inductance and shunt capacitance. Since the transformer characteristics are strongly temperature dependent the designer must take care to select a transformer that meets these requirements over the military temperature range, typically -55 degrees to 125 degrees Celsius. Doing so will ensure that the transformer meets the 1553 impedance requirement under even the most stringent conditions. The magnitude of the input impedance contributes to the loading (in addition to the stub load) placed on the bus. As the approximation shows, the input impedance is frequency dependent, which contributes to frequency dependent wave shaping.

At low frequencies, this shaping shows up as droop in the waveform that contributes to zero-crossing distortion due to nonzero rise time and also contributes to amplitude degradation. Droop in a transformer output is a result of the current increasing in the primary with time. The result of this increased current is to reduce the output amplitude because the increased current will accentuate the losses in the source driving the transformer and the losses in the transformer. Because there can be many transformers on a single network, the effective droop on the signal is greater because there are many inductors in parallel. More inductors in parallel cause less effective inductance and less effective inductance causes more droop. The effect of droop tends to work against the effects of the lossy cable, because cable is low pass and transformer droop creates a high-pass situation.

At high frequencies, the capacitive portion of the input impedance of the coupling transformer starts to dominate. This limits rise times of the waveform and contributes to amplitude and zero-crossing degradation. The shaping effect of the transformer at high frequencies serves to reinforce the effects of lossy cable.

In an effort to minimize the shaping and loading effects, 1553B has specified the minimum input impedance. To achieve this, the transformer designer must develop a device that has both high inductance and low capacitance. Because the inductance is proportional to the square of the number of turns and shunt capacitance is proportional to the number of turns, increasing one properties will usually increase the other. Hence, the designer must compromise to reach an optimum design and still meet the specification.

MIL-STD-1553B (4.5.1.5.1.1.2) requires that the droop of the output waveform at the high-turns side be less than 20% when driving the low-turns side of the transformer through a 360-ohm resistor with a 27V peak-to-peak square wave. This test constrains the low-turns side primary inductance to be greater than 3.2 mH, which in turn constrains the high-turns side to have a primary inductance of at least 6.4 mH (due to the fact that inductance is proportional to the square of the number of turns). Note that these limits already include any adjustments for worst case temperature variations. This result is consistent with the high-turns input impedance requirement. The output waveform is monitored for overshoot and ringing while doing this droop test. A maximum of ±1V peak is allowed on the approximately 38V output waveform, this is a±2.6% limitation. Overshoot and ringing are related to the values of the leakage inductance, shunt capacitance, and interwinding capacitance. The relationship is complex, but minimizing them will minimize the output distortion.

40.6.4.3 Common-mode rejection. Common-mode rejection for the coupling transformer is required to be greater than 45 dB at 1 MHz (4.5.1.5.1.1.3). The method for testing it is not specified, although it is suggested that the high-turns side be driven with a 1-MHz source while measuring the differential voltage across the low-turns side (with one end of the low-turns winding grounded). Lack of common-mode rejection capability is a result of parasitic capacitances between core and coils or interwinding capacitance that cause differential voltages on the secondary. Reducing the magnitude of these parasitic will reduce the magnitude of the imbalances and thus limit the amount of passed common mode.

When testing the common-mode rejection of a transformer, it is necessary to have a balanced load connected to the secondary for the test to be accurate. If the transformer being tested has one side of the secondary grounded, a decidedly unbalanced condition exists. This test method has two disadvantages:

a. It is unfair to the transformer, because it unbalances the internal parasitic. There are always parasitic in a transformer, and achieving a good design is not only a matter of minimizing them but balancing those that cannot be eliminated. Unbalancing the transformer makes the test more stringent than it needs to be.

b. The imbalance mentioned in item a can cause another effect, it can make the test inaccurate. If the parasitic capacitances are not balanced to begin with, then the transformer probably will not have very good common-mode rejection. If, in the testing process, the transformer is imbalance by the test setup, a false balance may occur between parasitic capacitances, and an incorrect passing grade maybe given to the transformer.

Therefore, it is recommended that a balanced circuit be used in detecting the passed common-mode voltage when testing transformers for common-mode rejection. Additionally, during common mode rejection testing, the transformer essentially forms a voltage divider between its interwinding capacitance and the input impedance of the detecting voltmeter. Thus, the results are determined as much by the voltmeter as the transformer. Care should be taken to use a meter which has as low an input capacitance as possible. It would be good to attach a load to the output winding as well, to reduce the sensitivity of the measurement to the impedance of the instrument used as a detector.

40.6.4.4 Summary of transformers. Coupling transformers are an important component of the bus network and may have a marked effect on the transmitted waveform. Using transformers that meet or exceed the requirements will help to ensure a network that has waveforms with minimum distortion and of high quality. There are several manufacturers that produce transformers that meet all 1553B requirements. Couplers that contain resistors connected per 1553B also are readily available on the commercial market.

40.7 ZERO-CROSSING EVALUATION. When designing a network, it is prudent to ascertain by some form of analysis whether or not the network will function. There are three primary classes of analysis that maybe undertaken: simplified hand analysis, computer simulation, and hardware simulation. Hardware simulation, the most reliable, is discussed in paragraph 40.8 along with software simulation. Here, analysis techniques are discussed using methods meant to provide a conservative estimate of performance of a proposed network. While not as accurate as hardware or software simulation, hand analysis is a quick way of determining the viability of a network.

40.7.1 First-approximation bus analysis. For any network, the most important feature of its waveforms is the zero-crossing distortion. Because this is a first-approximation method, only primary reflections will be considered, more complicated effects such as dispersion, transient stub reflections, and transformer losses will be ignored.

40.7.2 Zero-crossing eveluation. An important aspect of bus performance is the amount of zero-crossing distortion that the waveform can be expected to have. As mentioned earlier, dispersion causes zero-crossing distortion, but for a first approximation, this is too complicated an issue. Reflections from stubs add to the bus waveform producing zero-crossing distortion, and this effect is appropriate for a first approximation.

The amount of distortion caused by reflection is dependent on the reflection amplitude which, in turn, is dependent on the length of the stub. Also, whether this reflection distortion causes zero-crossing distortion is dependent on the timing of the reflection with respect to the bus waveform, so it is dependent on the bus length. All reflections on a 1553B network will be negative if the simple stub model is used.

Negative reflections occur when the bus waveform encounters an impedance smaller than Z_o, the parallel combination of the stub and the continuing bus. The direction that the reflection propagates is back toward the source. Beyond the stub, only a decrease in amplitude of the waveform is observed. Therefore, when deciding which stubs contribute reflective distortion to a specific receiving stub, ignore stubs that are between it and the transmitter. All other stubs contribute to reflective distortion.

Additionally, only primary reflections need be considered. Primary reflections are caused by the fundamental bus wave encountering a stub. A secondary reflection is caused by a primary reflection encountering a stub. Because primary reflections are on the order of 10%, secondary reflections will be on the order of 1% and can be considered insignificant for a first approximation.

40.7.3 Quantifying zero-crossing distortion. Reflections add to the fundamental bus waveform and change its shape. This, in turn, changes when the zero crossings occur. If all of the zero crossings are changed in the same manner, the result does not amount to zero-crossing distortion because the zero crossings have not moved in relation to each other. Therefore, reflections that are delayed by less than a pulse width add back onto the waveform before the subsequent transition occurs. For 1553B waveforms, the minimum pulse width is 500 nanoseconds. This “short” return reflection changes all zero crossings in the same manner, so it does not introduce zero-crossing distortion. Short return reflections may also affect the wave tops, but because these are supposed to be significantly above the zero crossing, wave-top distortion will not usually affect the zero-crossing distortion.

Figure 40-16 shows the effect of a short return reflection on the zero crossing of a received waveform. Note that the zero crossing of the received waveform is earlier than it would have been without the reflection. Because the reflection arrives at the receiver before any subsequent transition can take place, all zero crossings are shifted forward in time and no net zero-crossing distortion occurs. The amount that the zero crossing is shifted is equal to the transition time multiplied by the ratio of the reflection amplitude divided by the waveform amplitude (the reflection coefficient).

If the receiver is between the transmitter and the stub causing the reflection, reflections that return to the receiver delayed by less than 500 ns have to be the result of a stub that is less than 250 ns from the receiver. This is because the total reflection delay is the propagation time from the receiver, to the stub causing the

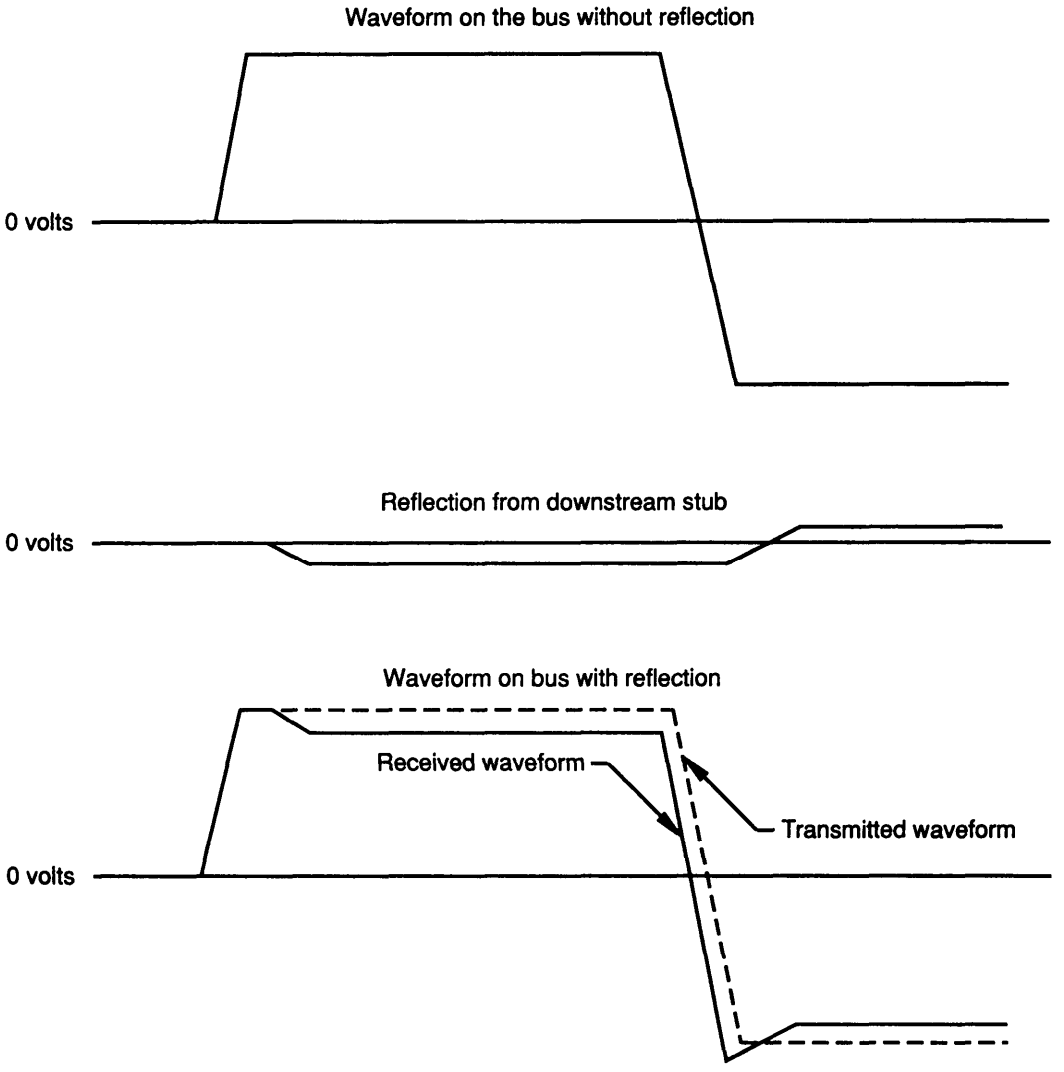


Figure 40-16. Effect of a Short Return Reflection on a Zero-Crossing Distortion

reflection, and back. Therefore, in this case, stubs less than 156 ft. from the receiver do not cause zero-crossing distortion. If the transmitter is between the receiver and the stub causing the reflection, reflections off the stub will arrive at the receiver delayed (with respect to the fundamental waveform) by twice the propagation delay from the transmitter to the stub. Thus, in the case where the transmitter is between the receiver and the stub causing a reflection, if the stub is less than 156 ft. from the transmitter, reflections from that stub will not contribute to the zero-crossing distortion at the receiver. Note also that all reflections change the shape of the wave tops.

Reflections delayed by more than one pulse width contribute to zero-crossing distortion. This is because the reflection of one transition affects the shape of the subsequent transition. If all pulse widths were equal, there would be no net zero-crossing distortion because all zero crossings would be changed the same amount. However, 1533B waveforms have varying pulse widths due to phase changes and sync pulses. Thus, zero crossings will be affected by different amounts of reflection and cause net zero-crossing distortion.

The delayed reflections are approximately 180 degrees out of phase with the 1-MHz portions of the waveform. As the reflections are negative in sign and completely out of phase, they add to the other 1-MHz portions of the waveform constructively. For longer pulses, they will still add destructively. This transient change in

amplitude causes the zero crossings of the 1-MHz pulses to be late relative to where they would have been without the reflection. The amount that the zero crossings are late is equal to the reflection coefficient multiplied by the rise time. The zero crossings for longer pulse widths will still be shifted early by the reflection coefficient multiplied by the transition time (because the reflections still add destructively). The net zero-crossing distortion is the difference between the zero crossings of the various portions of the waveform and will be equal to twice the reflection coefficient times the transition time.

For a signal whose rise time is 200 nanoseconds and has a 10% reflection (which is delayed by more than one pulse width, that is to say the result of a stub that is more than 156 ft. away), the zero-crossing distortion will be 40 ns. Figure 40-17 shows the relationship between the zero crossings of a 1-MHZ portion and a 500-kHz waveform portion (500-ns pulses and 1000-ns pulses) in the presence of a 10% reflection coefficient.

40.7.4 Assumptions for zero-crossing distortion calculation. For this analysis, the following assumptions are made to simplify calculations:

a. Turning the transmitter on does not affect the behavior of the reflections.

b. Waveform transitions are linear.

c. Stubs that cause reflections are resistive.

d. Dispersion does not affect the shape of the fundamental waveform or the shape of the reflections.

e. Transition time maybe ignored when determining how faraway a stub must be for its reflection to cause zero-crossing distortion.

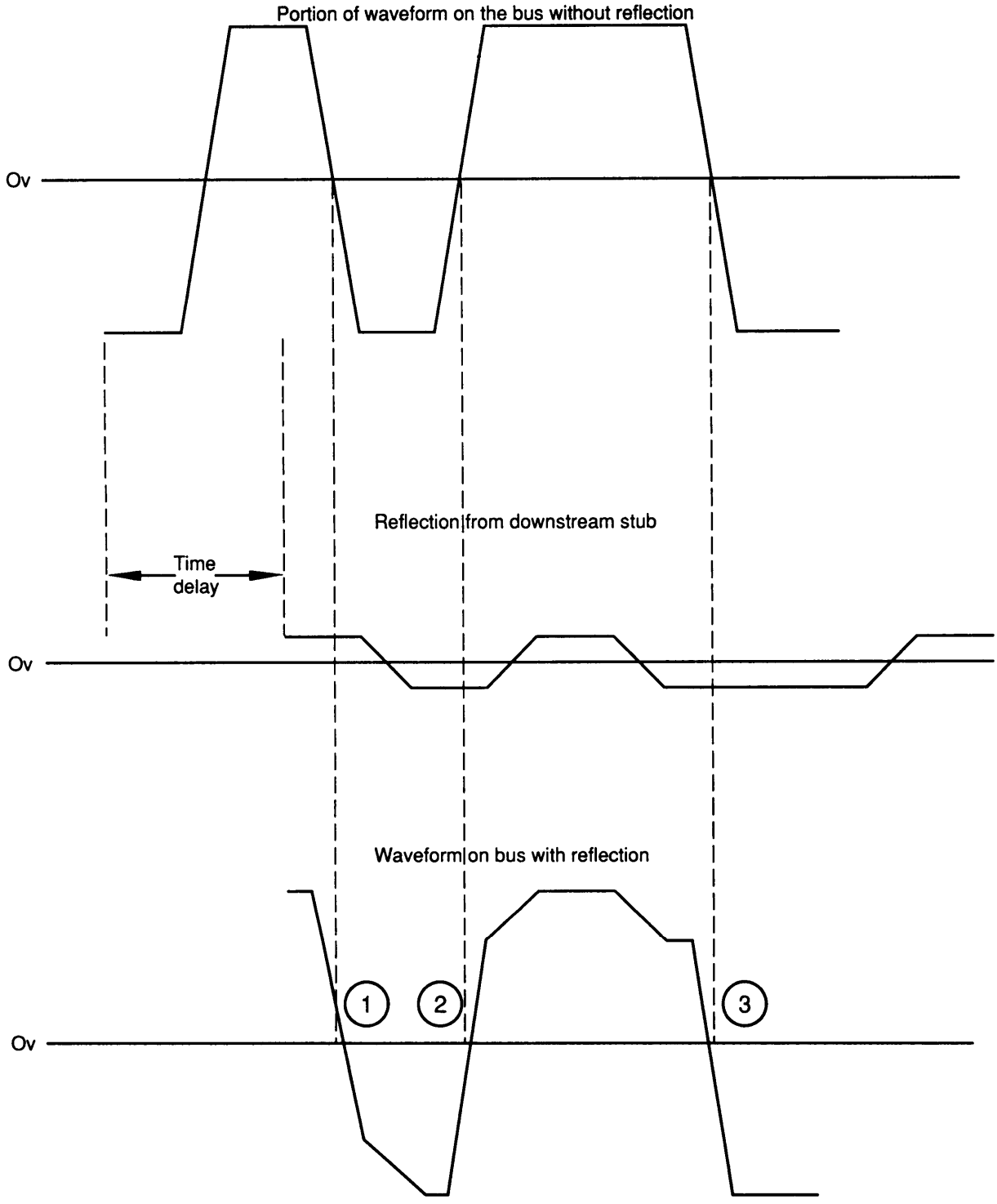
Assumption a ignores the fact that when the transmitter is on, the amplitude of reflections will be decreased. The transmitter may have a low output impedance when on. Thus, when it is on, it presents approximately a 110-ohm impedance to the bus because of the isolation resistors. This will decrease the amplitude of reflections by a factor of 0.75 because the CT of a 110-ohm load connected to it is approximately 0.75. Assuming that the amplitude of thereflections is not attenuated is a conservative assumption and therefore acceptable.

Assumption b ignores the dispersiveness of the cable, which was a stated assumption at the beginning. The effect can be ignored for buses up to 200 ft. long.

Assumption c was justified in paragraph 40.6.2.5. It is an assumption that is necessary for this type of analysis. Because long stubs are less than 20 ft. long, this is a relatively good assumption. It must be noted though that, because stubs appear to be a larger impedance to lower frequency pulses, this assumption is also a conservative assumption.

Assumption d is also a conservative assumption because it presumes that the amplitudes of reflections will be maximum. In reality, they will be attenuated and therefore have less effect than this analysis assumes.

Assumption e concerns itself with the selection criteria for when stub reflections contribute to zero-crossing distortion. The analysis assumes that zero-crossing distortion begins immediately when a reflection gets delayed by 500 nanoseconds. In fact, zero-crossing distortion begins when the reflection is delayed by 500 nanoseconds minus the transition time of the signal. This is sooner than the analysis assumes. However, the amount of zero-crossing distortion at this point is zero. The amount of zero-crossing distortion increases as the delay increases until the distortion reaches its maximum. The maximum distortion occurs when the reflection delay is equal to 500 ns plus the transition time. Therefore, the analysis assumes for the sake of simplicity that maximum distortion begins at the median reflection delay time. This assumption mayor may not be conservative depending on the length of the bus. For buses that are under 156 ft. long, there maybe some reflective zero-crossing distortion that this analysis does not take into account.



Note: Crossings 1 and 2 are offset in the same direction so there is no relative zero crossing distortion between them. Crossing 3 is offset in the opposite direction from 1 and 2, causing zero crossing distortion.

Figure 40-17. Effect of a Long Return Reflection on Zero-Crossing Distortion

40.7.5 Calculating Zero-crossing distortion. Zero-crossing distortion worsens with reflection delay. Therefore, it is bound to be worst at the ends of the bus. A good way to determine whether a bus has the potential for zero-crossing distortion problems is to perform the following steps:

a. Convert stub lengths to reflection coefficients using figure 40-13. Convert bus lengths to nanoseconds by multiplying by 1.6. Figure 40-18 shows the network converted to reflection coefficients and nanoseconds.

b. Select, as the worst case receiver stub, the stub that is second from the end of the most lightly loaded half of the bus. The worst case transmitter stub is assumed to be the end most stub on the same end as the worst case receiver stub. For the network in figure 40-18, the receiver stub is stub2 and the transmitter stub is stub1.

c. For every stub located more than 250 nanoseconds from the receiver stub, add the reflection coefficients to forma total. Only stub 6 in figure 40-18 qualifies, and its total reflection coefficient is -0.088.

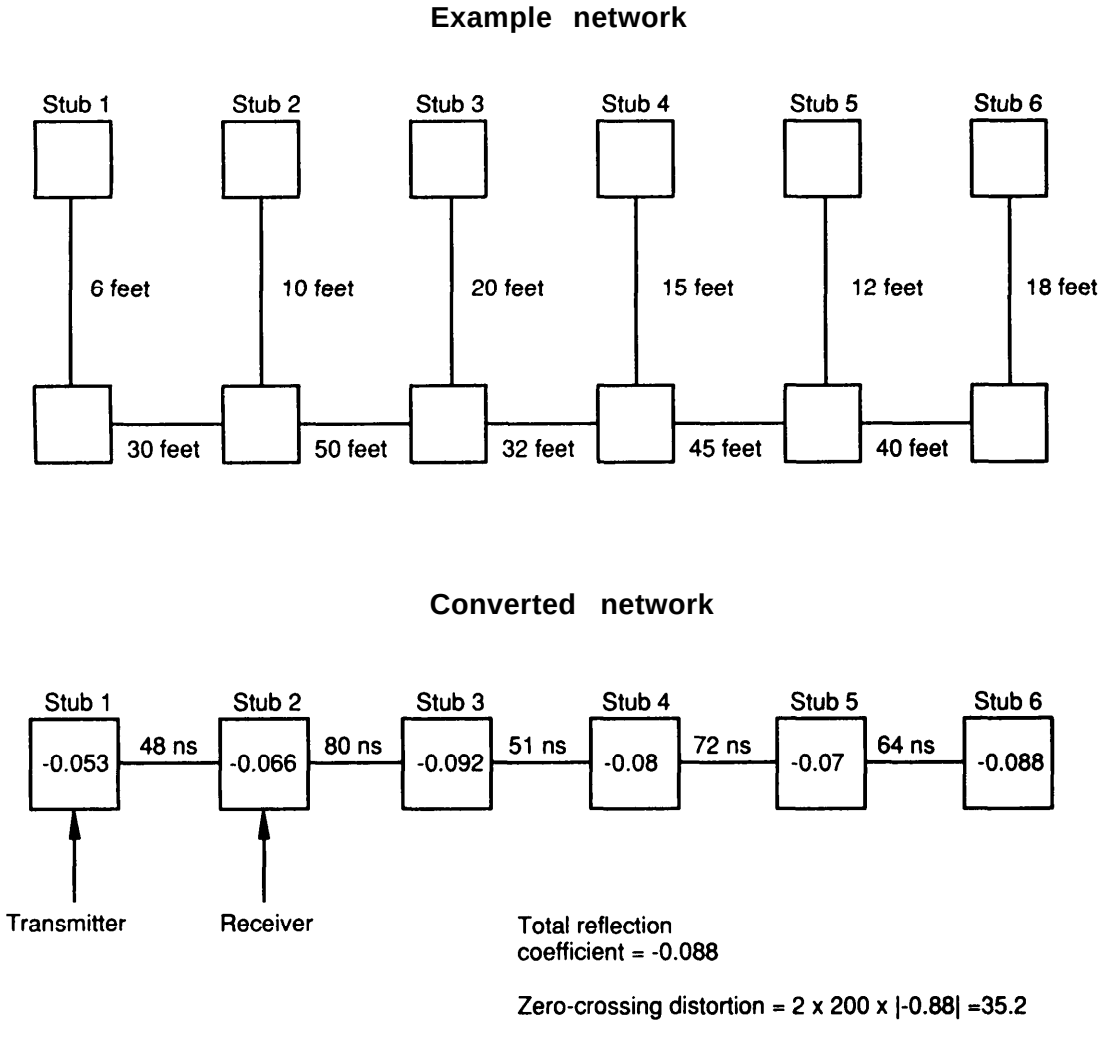


Figure 40-18. Example Network

d. Multiply the sum of the reflection coefficients by the signal transition time. Because the receiver and transmitter stubs are at the same end of the bus, the transition time at the receiver will be nearly identical to the transition time at the transmitter. On the average, this will be 200 nanoseconds. Multiply the total reflection coefficient times the transition time for the reflective zero-crossing distortion. In this case,

(2 x 200 x 0.088)=35 nanoseconds.

This number is substantially below the 125-ns limit suggested in paragraph 40.9.1. For buses with more or longer stubs, the zero-crossing distortion will increase. If the number grows beyond 125 nanoseconds, caution should be exercised in implementing the design, and further analysis and simulation should be carried out.

A maximum value for total reflection coefficient maybe derived if a transition time is assumed. For a 200-ns transition time, this maximum allowed total reflection coefficient is -0.31. The worst case reflection coefficient for a shorted stub is -0.29. This is so closet ot the -0.31 maximum allowed value that the conservative approach of this simplified analysis will almost always cause a network design to be declared inadequate. Therefore, to assess the effect of a shorted stub on the bus waveform, a more detailed analysis and simulation must be done.

40.7.6 Assessing results. The bottom line recommendation resulting from this first approximation bus analysis discussion is that a warning flag be raised if either the amplitude or zero-crossing test fails. Failure of one of these tests does not mean that the network will not work, the conditions assumed are absolutely worst case and may not apply. If either test fails, more analysis and simulation is needed before committing to a design. Remember that the best and most certain way to determine whether a network will work is to build and test it in the laboratory. There is no substitute for laboratory results.

40.8 NETWORK SIMULATION. It is essential that a proposed network be simulated before the design is finalized. There is enough latitude in 1553B that a network fully in compliance with the standard might still not work. Therefore, as part of the design process, time and assets must be allocated for evaluating the proposed network.

There are two ways to simulate a bus: with a computer or with a hardware mockup. The most accurate and most certain method is with the hardware mockup. Because the accuracy of a computer simulation is only as good as the assumptions it makes, it is limited.

40.8.1 Hardware mockup. Ideally, the network designer will have access to a fully equipped laboratory for designing and verifying a data bus network. This maybe an in-house laboratory or facilities of the component suppliers. The facilities should have the capability of modeling any configuration of production components and the equipment necessary to exercise the bus.

The first step in the simulation process is to identify stub types, lengths between stub connections, and stub lengths necessary to interconnect system terminals. Note, at this point, future expansion should be considered. This will yield a “stick” diagram of the bus to act as the baseline. With this information, a hardware mockup is constructed in the laboratory. A test regimen is applied to determine the waveform quality at each of the stubs for a transmission from each of the other stubs under nominal conditions. For a network having N stubs, this will result in (N - 1)N waveform evaluations.

This may result in a lot of tests (992 for a 32-terminal network), so stubs that are within 1 ft. of each other may be assumed to have the same received waveform. This is best done with realistic terminal loads connected to the unused stubs. If the network does not produce waveforms within limits stated in 1553B at all of the stub ports, the interconnect layout must be modified. The sources of the distortion must be identified and corrected. Refer to paragraphs 40.6 and 40.10 for additional information. If the network does not meet the recommendations in paragraph 40.9, modifying the layout should be considered.

Modification of the network maybe as simple as trading bus length for stub length (i.e., routing the bus closer to the terminals and shortening the stub lengths). It maybe as complicated as totally reorganizing the layout.

After the network has been verified as producing acceptable signals for all potential paths, it should be tested under a variety of fault conditions to maximize its robustness. The most important of these tests is the shorted stub. The network is required to produce acceptable waveforms with one shorted stub. To test this exhaustively would require an unreasonable amount of additional testing, so placement of the short and selecting the transmitter and receiver location prudently can save on test length. Emphasize the shorted stub testing for stubs that had the worst nominal characteristics. For stubs with poor amplitude characteristics, placing the short near the receiver (with the transmitter far away) will be the worst case. Stubs that had poor nominal zero-crossing characteristics should be tested with the shorted stub 156 ft. away and further (or as far as bus length permits) and the transmitter as near as possible to the receiver. The effect of having all stubs open circuited except the receiver and transmitter should also be investigated, but this will usually have little effect if stub lengths are short.

40.8.2 Computer simulation. While there is no substitute for a hardware mockup of a network, considerable time can be saved through use of a computer simulation. Computer speed allows evaluation of baseline bus design variations in a fraction of the time it would take using hardware. There are two types of computer simulations: time domain and frequency domain.

Time domain simulation is the most conceptually easy to understand. A transmission line maybe modeled with a delay (proportional to length) and a shaping response. Sections of these transmissions maybe linked to forma network. At stubs, the reflection coefficients are determined by the stub length and stub coupler characteristics. A time representation of a transmitted waveform can be input at a stub and the other stubs monitored for their output waveforms. The program automatically keeps track of the reflections at stubs and their delays. The output waveform at any stub can then be evaluated directly. The major drawback of this method is that it is difficult to model the lossy effect of transmission lines in the time domain.

A more accurate way of simulating a network on a computer is to handle the network response in the frequency domain. To do this, a frequency domain model of the network is constructed. At a transmitting stub of interest, the frequency spectrum of the transmitted wave is input; at the receiving stubs, the frequency domain representation of the received waveform is acquired. The received frequency spectrum is then converted back to the time domain for analysis. The most obvious drawback of frequency domain simulation is the complexity and amount of calculation. It has the main advantage, though, that transmission lines can be more accurately modeled in the frequency domain. Additionally, components such as transformers and receiver input filters convert readily to frequency domain analysis.

As with most modeled systems, assumptions must be made. Computer simulation can be accurate and detailed only to the point that the models used are accurate and detailed. Therefore, belief in the results of a computer simulation should be tempered with the knowledge that they are approximations. They are useful in determining the general behavior of a particular network layout, but they are no substitute for a hardware mockup in evaluating network performance accurately. An example of a network simulation program is presented in the next paragraph.

40.8.3 Bus network simulation example. A 1553 bus network simulation program was written to assist in determining bus network design guidelines (Reference, ‘Bus Length and Loading Limits of MIL-STD-1553 Buses, ”SAE Aerospace Avionics Equipment and Integration Conference; Dallas, Texas, November 1987 by: W.G. Briscoe, M. Davila and B. Skinner). Application of transmission line theory to signal propagation on the main bus cable of a 1553 bus network shows that the original transmitted waveform becomes distorted as reflected waves are generated at bus couplers along the bus cable. Although the reflected voltage amplitude at one single-port coupler with a 20-ft. long stub cable is only 5% (nominally) of the incident voltage, the reflections from several couplers can add to produce significant waveform distortion. A simulation based on a time domain analysis was developed because a frequency domain analysis would require considerably

longer computation times, and the time domain analysis produced sufficiently accurate results. Transformations between the time domain and frequency domain are not required when a time domain analysis is used because both the input waveform and the desired output waveform are time functions.

A signal on a bus transmission line is a traveling wave that propagates along the line at a constant velocity. Part of the wave is reflected at bus couplers, and the remainder of the wave continues to propagate down the line. A primary reflected wave is generated when the transmitted wave arrives at each coupler. These waves propagate back toward the transmitting terminal. Also, each primary reflected wave generates secondary reflected waves when the primary reflected wave arrives at each coupler. Additional reflections will occur, but a reflection will become insignificantly small after more than two reflections. For example, if a wave is reflected by a reflection coefficient of 0.1 and reflected again by a second 0.1 reflection coefficient, the amplitude of the secondary reflected wave is 1.0% of the original wave amplitude. The amplitude of a third reflection would be only 0.1% of the original wave amplitude. Therefore, the bus simulation program calculates the effect of only the primary and secondary reflected waves.

The Manchester-coded waveform is simulated by linear superposition of step functions with an exponential multiplier to give the proper rise and fall times. The program used up to eight step functions to simulate three of four bit periods at the end of a 1553 message. A complete waveform was simulated by computing the waveform at a point on the bus due to each step function, and then adding all of them. Step function waveforms were computed by calculating the amplitude of each primary and secondary reflected wave and then calculating the time of arrival of each wave at the selected point on the bus. Voltage waveform was computed as a function of time by incrementing time and adding waves that have arrived at the selected point on the bus at each time. If a step function has not arrived at the time for the calculation, its value is zero. At anytime after the step function has arrived, the voltage value for the wave is added. The time of arrival of a wave is the total distance traveled by the wave times the propagation delay factor of the cable (typically 1.5 to 1.6 nanoseconds/ft).

The voltage reflection coefficient (CR) at each coupler was computed using the equation:

$$CR = \frac{Z_L - Z_0}{Z_L + Z_0}.$$

Load impedance Z_L is given by:

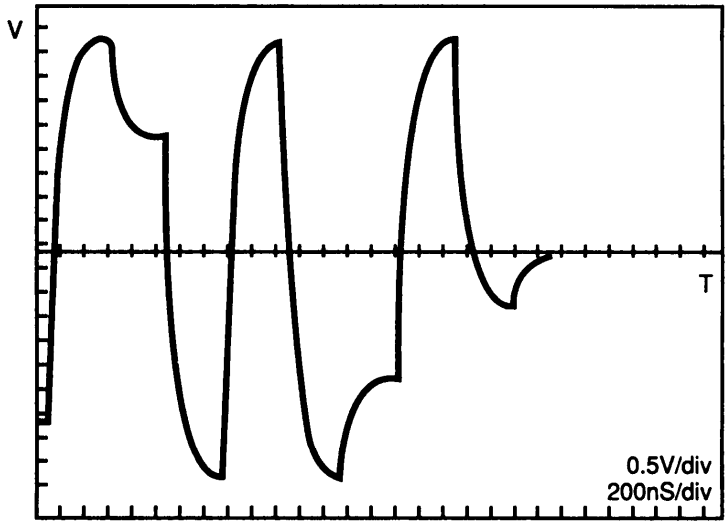
$$ZL = \frac{Z_C \times Z_O}{Z_C + Z_O}.$$

Where Z_0 is the coupler impedance and Z_0 is the characteristics impedance of the bus cable.

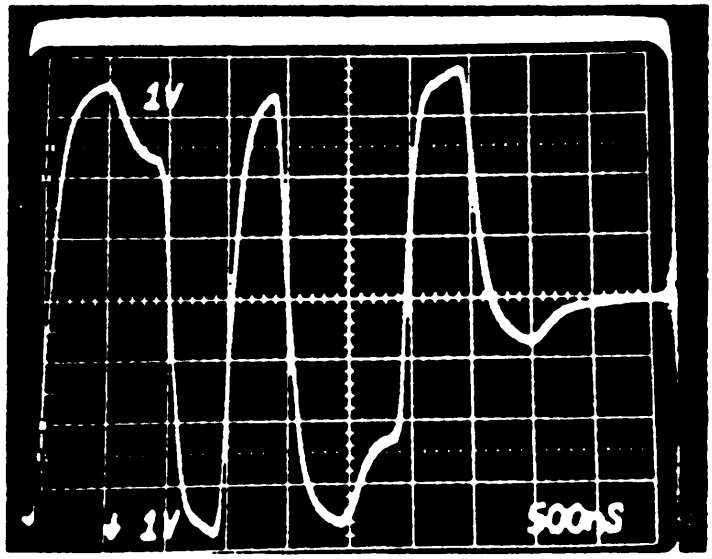
The reflection coefficients at the couplers were determined in the same manner as in paragraph 40.6.2.5, but nominal (instead of worst case) values were assumed for the bus components.

The bus simulation program computes the waveform at any coupler on the bus. It is assumed that the waveform received at a terminal (the end of the stub) is essentially the same as the waveform at the coupler connection to the main bus cable.

The computer simulation program was written for execution on an IBM PC or compatible computer. The bus waveform plot from the simulation and an oscilloscope photo of the bus waveform on the actual bus are given in figure 40-19. This was a 177 ft. long bus with nineteen bus couplers. Couplers 1 to 7 are grouped within six feet of one end of the bus, couplers 8 to 11 are grouped within three feet of each other and are 160 feet from the first group. Couplers 12 to 19 area multi port and are therefore only inches apart, they are five feet beyond couplers 8 to 11. The load resistance at coupler 11 was zero to simulate a short circuit fault condition.



a. Simulated Results



b. Lab Results

Figure 40-19. Simulation Output

The source was at coupler 1 and the output was at coupler 4. The plot and photo show the typical wave top distortion and extra pulse at the end of a transmission that are caused by bus reflections. Computer computation time for this simulation was about six minutes.

40.9 WAVEFORM QUALITY. As stated in the introduction, the most important aspect of a network is its ability to transfer voltage waveforms with minimum distortion. The ultimate test of the viability of a network is whether the received voltage waveform quality at all terminals meets the input requirements when receiving a transmission from any other terminal. To design and build a 1553B bus network that will work or analyze one that already exists, the received voltage waveform quality must be evaluated. Three indicators of received waveform quality are:

a. Received waveform amplitude.

b. Received waveform zero-crossing distortion.

c. Received waveform tailoff.

In 40.9.1, the waveform quality requirements of 1553B are discussed as an introduction to discussions of the three indicators of received waveform quality.

40.9.1 Waveform quality requirements. There are only two places in 1553B that explicitly state network performance requirements: paragraphs 4.5.1.5.1.4 and 4.5.1.5.2.3, which specify the minimum and maximum output voltages for direct- and transformer-coupled stubs. The voltage of any transformer-coupled stub must be between 1.0V and 14.0V peak-to-peak for any stub receiving a transmission from any other stub. The transmission may be between worst case specified voltages (at the transmitter), and there can be one shorted stub. The voltage of any direct-coupled stub must be between 1.4V and 20.0V peak-to-peak, with the same set of conditions. The required output levels for a terminal are 18V to 27V peak-to-peak for a transformer-coupled type and 6V to 9V peak-to-peak for a direct-coupled type. Either type of terminal may be connected to the same bus such that combinations of any types of transmitter and receiver pairs is allowed (i.e. transformer coupled with transformer coupled, transformer coupled with direct coupled, or direct coupled with direct coupled).

There is an implicit constraint that a network may add only 125 nanoseconds zero-crossing distortion to a signal. This comes from the fact that a terminal must correctly decode bus traffic with up to 150 nanoseconds zero-crossing distortion (4.5.2.2.2.1) and that a transmitting terminal may have up to 25 nanoseconds zero-crossing distortion in its output signal (4.5.2.1.1.2 and 4.5.2.2.1.2). Thus, for a signal to arrive at a terminal with less than 150 nanoseconds distortion, if it had 25 nanoseconds of distortion to begin with, the network had to have added less than 125 nanoseconds of distortion.

Consider as well that the network must work with a single shorted stub (4.5.1.5.1.4 and 4.5.1.5.2.3). It is also wise to design so there is margin for noise (and for good measure) as well as for future growth. These practices are not always possible, although attempting them will tend to make a design better.

40.9.2 Received waveform amplitude. The amplitude at any receiver is determined by the transmitted waveform amplitude, the total network loading, and the position of the receiver relative to the transmitter. The effect of the waveform amplitude on terminal ability to decode depends on the manner in which the receiver interprets the waveform at its input. (Transmitted waveform is discussed in section 50.)

As shown in 40.7.1.1, the amount of voltage from the transmitting stub to the main bus depends on total network loading. Total network loading is the impedance connected to the main bus. Because the terminating resistors are fixed, total network loading is a function of the number of stubs and their lengths.

The effect of receiver placement relative to the transmitter is shown in 40.7.1.1. Long distances between receiver and transmitter cause lower received voltages.

One advantage of higher amplitude is more noise margin. Because receivers typically have positive and negative thresholds (see section 50), the amount of margin is the peak waveform amplitude minus the threshold voltage. Therefore, it is not the amplitude above (or below) zero that is important, it is the difference between peak voltages and thresholds. The waveform amplitudes at which terminals are required to reject Gaussian noise at an acceptable rate are specified in 1553B as 2.1V peak-to-peak for transformer-coupled terminals and 3.0V peak-to-peak for direct-coupled terminals (4.5.2.1.2.4 and 4.5.2.2.2.4). It is strongly recommended that a network be designed that will meet these amplitudes. If, in an extreme case, lower amplitudes will occur, the designer must closely assess the noise environment in which the network operates.

Higher amplitude also provides greater immunity to distortion caused by reflections. As mentioned in 40.7.1.4, all reflections will affect the shape of the wavetops. Therefore, if waveform amplitude is near the threshold voltage of the receiver, the receiver will in essence be using wavetops to decode the signal. In such a case, the reflections ignored initially (because they were not delayed enough to affect zero-crossing accuracy) start to factor into the decoding of the waveform. Thus, overall, decoding integrity is more sensitive to reflections when the received amplitude is low.

40.9.3 Received waveform zero crossing. The zero-crossing distortion at the receiver input is a function of bus length, the number of stubs, and stub lengths. Reflections off stubs are typically the largest source of zero-crossing distortion. The effect of dispersion on zero crossing does not become a significant factor until bus length gets long.

Paragraph 40.7.1.4 discusses the effects of stubs on zero-crossing distortion. Paragraph 40.6.3.2 discusses the effects of dispersion on zero crossing. It is necessary that the zero-crossing distortion of the waveform reconsidered when designing a network. A system will not work if it does not meet the requirements in 1553B for zero-crossing distortion.

A network should always be designed such that it contributes no more than 125 nanoseconds to the waveform zero-crossing distortion. This applies to the case in which there is a shorted stub. It is recommended, however, that a network be designed with at least 25 ns of margin (including a shorted stub) to allow for future growth. Paragraphs 40.7.1.3 through 40.7.1.6 show a first approximation method for determining zero-crossing distortion. For a more accurate picture of network performance, it must be simulated (see 40.8).

40.9.4 Received waveform tailoff. At the end of a transmission, there are still reflections on the bus that are basically of the same frequency content as the bus waveform. Additionally, there will typically be a low-frequency exponentially decaying voltage (time constant approximately 25 us) that is the result of waveform imbalance (see 40.4.3). These two voltages add up to form the tailoff.

Tailoff is a conservative indicator of bus performance. The absence of any fundamental waveforms allows for close inspection of the reflections. If the reflections themselves (minus the low-frequency component) exceed 30% of the peak waveform amplitude and are delayed by 500 nanoseconds or greater, it means that the waveform is near the zero-crossing distortion limit. If the low-frequency component is very large (greater than 200mV), it is possible that the transmitting terminal has a waveform balance problem. This could cause problems with meeting the intermessage gap requirement (see section 50).

In either case, investigation of the tailoff waveform is a good measure of bus (and terminal) performance. When analyzing an existing system, the tailoff is an important piece of information.

40.9.5 Summary of waveform quality. Ultimately, waveform quality is the measure of network performance. Voltage waveforms at all stubs must meet requirements for minimum amplitude and maximum zero-crossing distortion. They should meet limits recommended in this document.

40.10 DESIGN GUIDELINE. The following guidelines are derived from section 40 as well as from experimental data. It is essential that the network designer consider them at the beginning of the design process. Beginning with a prudent design is an expedient way of drastically reducing the probability of future system problems.

40.10.1 Bus length. Keep bus length as short as possible. In other words, connect the bus to each terminal by the most direct path possible. Because reflections caused by transmission line effects are more dominant for longer transmission distances, keeping lengths short will minimize reflection. In addition, lossy effects of practical cable cause distortion that worsens proportionally with length. Although 1553B does not specify a maximum allowable bus length directly, there is an implicit constraint in the terminal response times. Because there is a difference of 2 us between maximum remote terminal (RT) response time and bus controller (BC) error declaration, the bus must be less than 1 us long. This limit is to allow for the propagation time from the BC to the RT and from the RT to the BC. Using 1.6 nanoseconds/ft., maximum bus length would be 625 ft. If a longer bus length is to be used, the RT response time and BC response timer interals will require careful attention to preclude spurious "no response" declarations. See section 50 for details of terminal design.

40.10.2 Stub distribution. Spacing of stub connections on the bus should be as uniform as possible. Collocating stubs causes an effectively larger mismatch at that point on the bus. It is twice the mismatch as for two closely located stubs, and three times the mismatch as for three, etc. It is best to locate stubs such that the bus distance between adjacent stubs is at least as long as twice the length of the longest of the two stubs. This will minimize the overlap of the transient portion of the distortive effects caused by the different stubs (see 40.6.2. 1). it should be noted that multistub couplers are becoming more popular. This is not a recommendation against using them. When making use of multistubcouplers, exercise caution to ensure that the distortion limits are not exceeded.

40.10.3 Cable routing. Route the main bus cable so stubs areas short as possible. Because the main bus is primarily a properly terminated transmission line and the addition of stubs causes distortion (worse with longer stubs), it can be reasoned that, in most cases, the best solution is to add length to the main part of the bus to lessen the length of the stubs. Following this suggestion will force the network toward the configuration suggested in guideline 40.10.2. It should be noted that the advantages of doing this must be weighed against the advantages of keeping the bus length as short as possible. The cable used throughout the bus and stubs should have the same part number to ensure uniform cable impedance. Also, where there is redundancy (two or more buses), route the data buses so a single event failure does not cause the loss of more than one bus (4.6.2).

40.10.4 Bus simulation. Perform simulations to determine waveform quality at each terminal connected to the network. From previous descriptions it can be seen that the effect of one stub on bus waveform quality may be readily understood when certain assumptions are made. Predicting the outcome when several (or many) stubs are connected to a substantially long bus becomes a much more complex and difficult task. Add to this task the variable of non-ideal considerations, and a complex situation arises. Therefore, simulations of any proposed network must be performed before a permanent design is committed. The final simulation should bean actual hardware mockup. Computer simulations are helpful in the early stages of design. It is important to remember that, despite some general rules, each network configuration is unique and must be validated individually. Although 1553B are a standard and fairly well thought out, there are enough allowable variances to warrant investigation of individual networks. Criteria for judging bus waveform quality are in 40.9 through 40.9.5; simulation is in 40.8.

40.10.5 Selecting resistors. Select isolation and termination resistors with proper values, tolerances, and power ratings.

MIL-STD-1553B specifies resistors to be used in three places:

a. In direct-coupled terminals for isolation between terminal and stub.

b. In couplers used for transformer-coupled stubs to isolate stub and coupler from the bus.

c. For terminating the ends of the bus.

Resistors used indirect-coupled terminals will not be discussed here because they are covered in section 50.

Isolation resistors specified for transformer-coupled stubs (4.5.1 .5.1.2) are 0.75 x Z0 ± 2% ohms. The only problem is to accurately know the nominal Z_0 of the cable, this value is specified by the manufacturer at a certain frequency (usually 1 MHz for cable that is designed for 1553B). Additionally, the power dissipation capability must be sufficient to handle worst case transmission duty cycle and amplitude.

The worst cast for isolation resistors exists when the terminal connected to the same stub as the isolation resistors is the transmitter. Making all worst case assumptions (small rise time, 100% duty cycle, maximum transmitter amplitude, and minimum bus impedance), the most power that these resistors will have to dissipate is 1W each.

The bus-terminating resistors are required to be Z_0±2% (4.5.1.4). Again, as in the case of the isolation resistors, their value depends on the nominal cable impedance, so cable manufacturer specifications must be consulted before selecting these resistors. The maximum power dissipated in these resistors, using the same worst case assumptions as for the isolation resistors, is 0.35W.

For both types of resistors, be certain that their resistance is constant from direct current up to frequencies of at least 6 MHz. Most of the energy of a 1553B waveform is within this frequency band.

40.10.6 Shielding. Properly shield the network. The requirements for the bus cable in 1553B paragraph 4.5.1.1, as redefined by 30.10.1 of Notice 2, state that there must be four twists of the two conductors per foot of wire length and that there must be at least 90°4 shielding coverage. Additionally, 1553B paragraphs 4.5.1.5.1.3 and 4.5.1.5.2.2, as well as 30.10.2 of Notice 2, state that the junctions between bus and stub must have 75% shielding coverage.

The percentage of cable shielding coverage is a measure of the density of the metal braiding commonly used for shielding. The denser the braid, the higher the percentage of coverage. Typically, manufacturers can furnish the level of shielding for the cables they produce.

Shielding is a measure taken to reduce the energy coupled to the bus. Shields usually are grounded at each coupler. Care must be taken that the shields of the various pieces of cable that makeup a network are held at the same potential by connecting them through the cable junction.

Twisting the two wires that make up the cable ensures that most of the energy that gets past the shielding is coupled as common mode. MIL-STD-1553B is, by specification, resistant to common-mode voltages and making sure that most of the coupled noise is common mode enhances network performance.

40.10.7 Experimentally based guidelines. The following subset of guidelines is based on experimental results and practical experience, they include the effects of a single shorted stub. They are put here to give the reader an idea of practical limits of bus loading. Despite numerical guidelines such as this, it is still necessary to simulate a bus design.

a. If total bus length is less than 100 ft., 32 terminals with stubs up to 10 ft. long can be connected in almost any desired distribution along the bus cable. This is true because waveform distortion due to reflections on transmission lines only becomes significant when reflected waves are delayed by at least 100 nanoseconds (for a 100-ns rise time) relative to the transmitted wave. The reflection point must be located about 33 ft. from the receiving terminal to produce this amount of delay. Because the reflection from a single coupler with a 10-ft. long stub under nominal conditions is only about 3.0% of the incident voltage wave, a closely spaced group of 12 couplers is required to cause transmission errors. A safe design rule would be to position no more than 12 terminals on any 33-ft. section of the bus.

b. Total bus length can be 200 ft. if the 32 terminals are distributed so that no more than eight terminals are positioned on any 50-ft. section of the bus. It maybe necessary to keep stub cable lengths less than 10 ft. long. Simulation should be used to ensure that waveform distortion is not excessive.

c. If all stubs are transformer coupled and less than 1 ft. long, 300- to 400-ft. long buses are possible. Because the reflection from a single coupler with a 1-ft. long stub under nominal conditions is only about 1.0% of the incident voltage wave, a closely spaced group of 30 couplers would be required to produce transmission errors.

d. In general, stub length should be short to minimize waveform distortion. One coupler with a 15 ft. stub causes about the same amount of waveform distortion as two couplers with one foot stub lengths. A 25 ft. long stub can cause as much waveform distortion as three couplers with one foot stub lengths. In special cases, where the main bus is short (less than 50 ft.) and only a few terminals are required, it may be possible to use one or two stubs that are 25 to 50 feet long.

SECTION 40 INDEX

SECTION 50

TERMINAL DESIGN

CONTENTS

FIGURES

TABLES

50.1 INTRODUCTION.

50.1.1 Scope. This section discusses hardware design of MIL-STD-1553B terminals. A basic understanding of MIL-STD-1553B is assumed. Section 20 of this handbook should be read and its commentary understood before reading this section. Explanations of the rationale behind sections of the standard will sometimes be repeated or expanded where necessary.

This section was written for the engineer who is just starting to design a MIL-STD-1553 terminal. There are many integrated circuit or hybrid microcircuit parts available from many vendors with which to build the terminal. The designer should probably have a collection of data sheets for candidate parts in hand while reading this section. This section contains guidance to the designer on choosing the proper parts for his application, although no vendor names are mentioned. System requirements will determine the need for some of the optional features, so the terminal design should not be attempted until system requirements have been defined.

This section discusses many factors that must be considered when designing MIL-STD-1553B terminals. Very few hard-and-fast rules are given or can be given. The system considerations that play a big role in the design decisions that have to be made are discussed further in section 60 of this handbook.

It is hoped that the discussions in this section alert the reader to requirements in MI L-STD-1553B that are not obvious or are often overlooked and that it suggests design solutions for them.

The analog front end of a terminal is one of the most critical elements of the overall design. The fact that most terminals being designed today use off-the-shelf hybrid or VLSI IC parts has gone far toward simplifying terminal design.

Hints for designing the rest of the terminal are also given, along with generic design examples of a remote terminal (RT) and a bus controller (BC). These examples, along with the specific system design examples in section 70, should enable the designer to design terminals in a much more intelligent and efficient manner.

This terminal design section is organized as follows:

a. Paragraph 50.2 explains terminal types and discusses issues that are common to all terminals.

b. Paragraph 50.3 discusses the analog front end or that portion of the terminal that deals with the terminal characteristics discussed in 4.5.2 of MIL-STD-1553B. Two design examples are included.

c. Paragraph 50.4, the digital section, deals with bits, words, and messages. This section is applicable to all types of terminals.

d. Paragraph 50.5 discusses remote terminal (RT) requirements. A general design example is included.

e. Paragraph 50.6 discusses bus controller (BC) requirements. A general design example is included.

f. Paragraph 50.7 discusses bus monitor requirements.

g. Paragraph 50.8 is a short discussion of design issues related to compatibility of terminals with older systems.

1553, 1553A, and 1553B- These terms will be used to mean MIL-STD-1553 (any version), MIL-STD-1553A, and MIL-STD-1553B, respectively.

Terminal- A terminal is defined in 1553B (3.10) as “The electronic module necessary to interface the data bus with the subsystem and the subsystem with the data bus. Terminals may exist as separate line

replaceable units (LRUs) or be contained within the elements of the subsystem." This definition allows a terminal to be a totally separate LRU, a circuit card, or a small portion of a circuit card; there is no restriction on the physical partitioning of the system. However, the current trend in technology is for smaller size and fewer parts.

A terminal is either a bus controller (BC), a remote terminal (RT), or a bus monitor. Nothing in 1553B precludes a terminal from including the capability of performing the functions of more than one of these three types of terminals, but a terminal may perform only one function at any onetime.

Bus controller (BC)- A BC is defined in 3.11 of 1553B as "The terminal assigned the task of initiating information transfers on the data bus." There is one (and only one) BC on a 1553B bus at any given time, and this terminal totally controls the flow of information on the bus. No other terminal may transmit anything on the bus except as instructed by the BC.

Bus monitor— A bus monitor is defined in 3.12 of 1553B as "The terminal assigned the task of receiving bus traffic and extracting selected information to be used at a later time." A bus monitor does not transmit status words or anything else on the bus. It may have no terminal address and, in fact, can receive information addressed to any (or all) terminals on the bus. As defined in section 4.4.4 of 1553B, a bus monitor may have an assigned terminal address, in which case it acts just like an RT for commands to that address. The two most common applications of bus monitors are:

a. Instrumentation, for recording bus traffic from many or all terminals for off-line analysis.

b. Backup BC, to provide a terminal with enough information to become the BC on the bus if commanded to do so, either with a dynamic bus control mode command or by some other method.

Remote terminal (RT)- RTs are defined in 3.13 of 1553B as "All terminals not operating as the bus controller or as a bus monitor." An RT cannot initiate any data transfer on the bus (like a BC can) and must respond to commands issued by the BC (unlike a bus monitor). It is important to note that an RT cannot initiate information transfers on the bus; only the BC may do this. Each RT has a unique terminal address assigned to it; information may thus be directed to each specific RT.

Subsystem- The subsystem is defined in 3.8 of 1553B as "The device or functional unit receiving data transfer service from the data bus." The subsystem is considered to be the portion of the LRU (line replaceable unit—the entire item of electronics) other than the terminal. In other words, it is the hardware interfacing with the nonbus side of the terminal.

System configuration- A 1553 bus system includes a BC (and possibly one or more backup BCs), one or more RTs (up to a maximum of 31), and zero or more bus monitors (typically not more than one, but could be any number). The BC has control of the system. It initiates messages that transfer data to or from an RT or control the operation of an RT. Each RT receives data sent to it by the BC, transmits to the BC or to another RT the data requested by the BC, or performs the commanded control function. A bus monitor listens to the traffic on the bus and extracts whatever information it has been programmed to extract.

50.1.2 Terminal block diagram. A general diagram of a 1553B terminal is shown in figure 50-1. This figure applies to all types of terminals (RT, BC, and bus monitor). The partitions between functions shown do not necessarily represent actual physical partitions. That is, the blocks shown might or might not represent actual parts. In a real system, functions might be partitioned differently among the parts used to implement the design.

It infrequently difficult to define the dividing point between the terminal and the subsystem. In many systems, this dividing point would logically be drawn through the middle of a physical component. That is, there is a component that performs some of the functions described here and some of the functions assigned to the

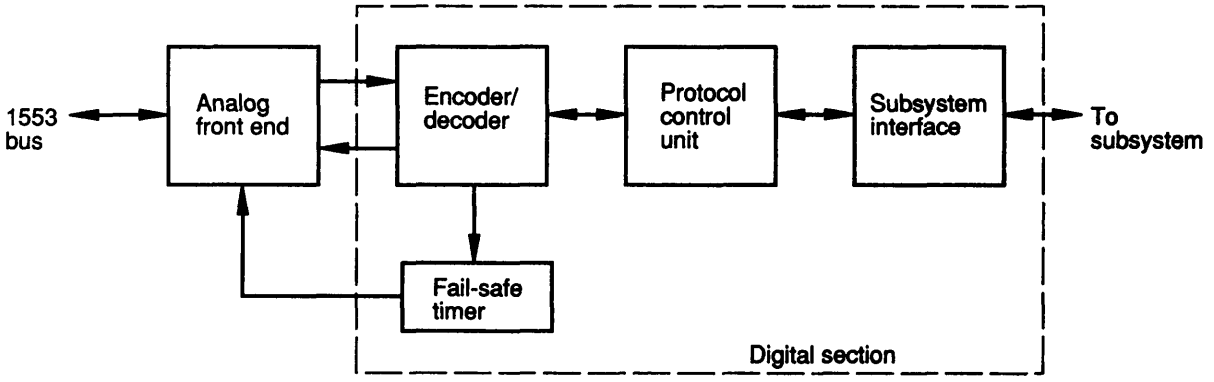


Figure 50-1. Terminal Block Diagram

subsystem. However, all the functions discussed need to be performed, and the arrangement shown is a common way of actual physical partitioning.

The analog front end of a 1553B terminal (see 50.3) consists of one or more channels (multiple channels are used for redundancy-see 50.4.3). Each channel contains an interface to translate the 1553B bus signal (whose signal characteristics are as defined in 1553B) into a digital signal with voltage levels appropriate for the remainder of the terminal (typically TTL-transistor-transist or logic-voltage levels). Conversely, the digital levels must be translated into the 1553B signal levels for transmission.

The remainder of the terminal is termed the digital section (see 50.4). The digital section contains a fail-safe timer to prevent transmissions longer than 800 µs, as required by 4.4.1.3 of 1553B (see 50.4.2 for more discussion of the fail-safe timer).

Each channel of the digital section also contains an encoder/decoder that deals with the data on a bit and single-word level. Its purpose is to change the data from its Manchester-coded format into the proper digital data format (typically 16-bit parallel) needed by the rest of the terminal (and vice-versa), and to perform error detection for word-level 1553B errors (e.g., bit count errors, Manchester coding errors, etc.). There must be a separate decoder for each channel, but there might be only one encoder.

The protocol control unit in the digital section deals with the message as a whole. There maybe one of these per channel, or there maybe only one for the whole terminal. Its purpose is to form messages from words (and vice-versa), to know the type of message and perform the proper actions depending on this, and to perform error detection for message-level 1553B errors (e.g., word count errors). This section is different in each of the three types of terminals.

The final element of the digital section is the subsystem interface. Its design varies greatly depending on the type of interface required between the terminal and the subsystem.

Those portions of the terminal design that are common among all three types of terminals are discussed first (50.3 and 50.4). Portions unique to each type of terminal (i.e., the protocol control unit and the subsystem interface) are discussed later in individual sections for RTs (50.5), BCs (50.6), and bus monitors (50.7).

50.2 GENERAL DESIGN CONSIDERATIONS. The design of a 1553B terminal depends on many different factors. First, of course, is the choice of BC, RT, or bus monitor. This choice is usually obvious. In most 1553B systems, the BC is part of a computer that processes information transferred on the bus. Each source of information (e.g., a switch panel or an inertial navigation unit) and each sink for information (e.g., a display panel or a store, which is a device carried by an aircraft and normally used up during a mission, like a bomb

or a missile) includes or interfaces with an RT. Note that nothing precludes a particular LRU from being both a data source and a data sink. There mayor may not be a bus monitor connected to the bus for instrumentation purposes (e.g., for gathering data for flight test or mission analysis) or as part of a backup BC. In each case, the required function (BC, RT, or bus monitor) is usually clear.

In some cases, a terminal must perform the functions of more than one of the three types. Some RTs must also have the capability to be BCs. If the (current) BC issued a dynamic bus control mode command to an RT with the capability to accept it, the RT would become the BC, and the (former) BC would become an RT. Note that Notice 1 and Notice 2 prohibit the use of this function for Air Force avionics applications, although neither BCs nor RTs are prohibited from implementing the capability. Some bus monitors may also act as RTs with a defined terminal address. This capability is often used to check the status of the bus monitor, particularly in systems in which a bus monitor is permanently installed.

50.2.1 Types of terminals. Terminals can be designed with different degrees of intelligence and autonomy. They can be divided into three categories by the type of control or protocol logic used in their implementation. From the simplest to the most complex, these are single-word, single-message, and multiple-message terminals. BCs can be designed to fit any of these categories, but normally RTs or bus monitors would be designed only as single-word or single-message terminals.

50.2.1.1 Single-word terminals. In a system with a single-word terminal, the subsystem must process each word in each message individually. That is, a single-word terminal requires subsystem intervention or action for every word. After all the words have been received, the subsystem processor must determine the validity of the message and construct the proper response. The response must then be transferred to the terminal one word at a time and transmitted.

A single-word RT would send all received data words to the subsystem, one at a time. The subsystem would have to validate the message, construct and send the status word on the 1553 bus, and then send any data words required. For a single-word BC, the subsystem would have to construct the desired command, instruct the BC to send it, define which of the 1553 buses to send it on (in a redundant bus system), provide any data words required, read the response from the BC, evaluate the response, and initiate any further action.

In a microprocessor-based subsystem, this type of terminal would probably be an I/O channel to the processor. Depending on the level of bus traffic, the subsystem processor could experience a reduction of 20% or more in throughput due to the processing demands of the 1553 I/O channel. Terminals of this sort were common in the early days of 1553 but are seldom seen today. The amount of support that they demand from the subsystem is usually unacceptable, and parts are available to implement terminals that are more intelligent with little difficulty.

50.2.1.2 Single-message terminals. A single-message terminal has enough capability to construct or process a complete message without any action by the subsystem. Subsystem action is required only at the beginning (for a BC) or end (for an RT) of the message or in the event of an error.

A single-message RT is always ready to respond autonomously to a valid command on the 1553 bus. It decodes the command to determine the proper data and then transfers it to or from the subsystem. The subsystem may need to be informed that a message has been received so that the data may be used or updated, but commonly, the subsystem does not require such notification. Since the RT is controlled by the commands received on the bus, there is no need for any control by the subsystem.

A single-message BC transmits the required command and data words on the 1553 bus. The status word received in response is then provided to the subsystem, along with any error indication. The subsystem is responsible for processing any errors and interpreting the status word contents, deciding what the next message should be, and then issuing it. This type of terminal is typically used with a microprocessor-based subsystem; the messages to be sent are all constructed by the subsystem processor and placed in defined

memory locations (to be read by the terminal via direct memory access (DMA)) or written to registers in the terminal.

In either case (RT or BC), the terminal provides the data to the subsystem or gets the necessary data from the subsystem autonomously, usually via DMA into subsystem memory. The terminal informs the subsystem, probably with a discrete interrupt, when the message is complete and if there were any errors.

50.2.1.3 Multiple-message terminals. A multiple-message terminal has even more intelligence. It is a processor or sequencer in its own right. This type of terminal only makes sense as a BC, although some multiple-message BCs are capable of being configured to act as RTs upon command from the subsystem or with a discrete interrupt. It is capable of chaining several messages together, maintaining a schedule of messages required on the bus, and initiating all transfers at the required times and in the required sequence. In system terms, the multiple-message BC would be programmed with a whole minor frame or even major frame at a time.

Some multiple-message BCs are intelligent enough to interpret the responses (e.g., status word bits), automatically retry failed messages, and perform exception chaining (i.e., modification of the message list in the event that a message fails). The subsystem would normally be interrupted only when the message list is complete or if there is an error. In some systems, there might need to be notification of each message or selected messages. This would need to be defined in the system's specification.

50.2.2 Terminal partitioning . Terminals may have various proportions of their design in hardware, firmware, and software. Typically, an older design, simple terminal would be almost all hardware, while a newer design, complex terminal would consist largely of software or firmware. Most of the design tradeoffs are similar in the case of 1553B terminals to those for most other systems, so they will not be repeated here. The availability of integrated circuit and hybrid microcircuit parts that implement large portions of the terminal design, and which are considered hardware, simplify the partitioning. This point is discussed further in the design examples later in this section (see 50.5.8 and 50.6.6).

50.3 ANALOG FRONT END. The analog front end of a 1553B terminal is a very important portion of its design. An inadequate analog design can cause an otherwise well-designed terminal to be marginal and a marginal terminal to be inoperative. This section discusses the devices that are available for terminal front end design and some design considerations for meeting the specifications in 1553B. It also includes two design examples.

There are two major elements in the analog front end of a terminal (see figure 50-2). The receiver translates bus signals into a digital form suitable for the rest of the terminal. The transmitter, or driver, translates signals from the remainder of the terminal into the proper waveforms to be transmitted on the bus. Almost all practical terminals also contain an input transformer, and a terminal designed for a direct-coupled stub input contains two fault-isolation resistors.

Transmitters and receivers are usually implemented in current designs as hybrid microcircuits. Most terminals that are designed today use a transceiver, which consists of a transmitter and a receiver mounted together in one package. Transceivers are available with either one or two complete units mounted in a single package. Newer parts commonly have greater portions of their design in monolithic integrated circuits (ICs). That is, they are built with fewer parts. There will soon be available a true monolithic transceiver, or an entire transceiver built on one piece of silicon.

Receivers and transmitters are treated separately in the following discussion (50.3.1 and 50.3.2). Even when packaged as a transceiver, the receiver and transmitter portions are generally electrically and functionally independent. Considerations that apply to the whole transceiver are also discussed (50.3.3).

50.3.1 Receivers. The receiver is the terminal element that translates the analog waveform received from the 1553 bus into a digital signal of appropriate characteristics (typically differential TTL) for the rest of the

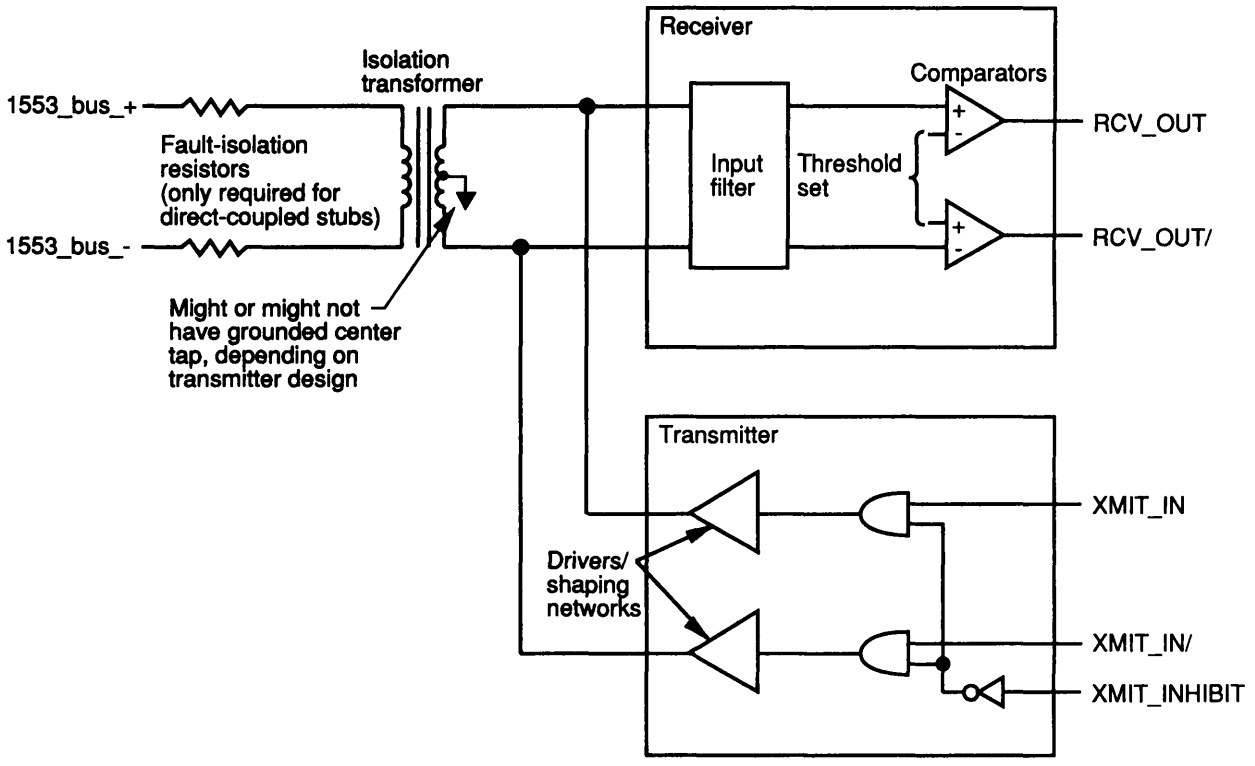


Figure 50-2. Analog Front End

terminal. It does no decoding or checking of the signal. A receiver contains an input filter to remove noise and a threshold comparator. It produces an output of 1 (i.e., RCV_OUT high) when 1553_BUS_+ is sufficiently greater than 1553_BUS_—, an output of 0 (i.e., RCV_OUT/ high) when 1553_BUS_— is sufficiently greater than 1553_BUS_+, and both differential outputs high (or low, see 50.3.1.2) when there is no sufficiently large signal on the 1553 bus.

50.3.1.1 Receiver input filtering. The input filter is a key element in determining receiver performance. The bus signal is corrupted by the addition of noise, often to the point that it is difficult to decode. This noise is mainly due to reflections from impedance discontinuities (e.g., stubs, in-line connectors, and terminators) in the bus network. Another source of noise is electromagnetic interference (EMI) or coupling of signals into the cable from other parts of the system. Both of these types of noise are mostly higher in frequency than the 1553B fundamental frequency of 1 MHz. The purpose of the receiver input filter is to eliminate as much of this noise as possible while minimizing signal attenuation.

This noise and signal distortion can cause multiple zero-crossings to occur in a bit time (1 µs) and can also cause a large error in the time of a zero-crossing (a zero-crossing shift error). This could cause the word to be misinterpreted by the decoder. The decoder would detect this as a Manchester error, which is a bit that does not have opposite values in the two halves of the bit time. One bit could also be distorted sufficiently that it is decoded as valid but of the wrong value. The decoder would detect this error with the parity bit. In both of these cases, the decoder knows the word is invalid, and the message transfer fails. It is also possible that the signal could be distorted to such an extent that the decoder thinks it is valid, but decodes the wrong value. The purpose of the receiver input filter is to reduce the word error rate by reducing the noise or distortion of the signal. Design experience has shown that the specified word error rate cannot be met without filtering on the input of the receiver.

A 1553B bus operates at a bit rate of 1 MHz. Due to the Manchester encoding of the data, there are frequency components at 250 kHz, 333 kHz, and 500 kHz as well as 1 MHz. This follows from the possible zero-crossing

time intervals of 0.5, 1.0, 1.5, and 2.0 µs in a 1553B signal. At first glance, therefore, it would appear that a filter that passed the band of 250 kHz to 1 MHz and rejected everything else would pass the entire signal but reject much of the noise. However, the trapezoidal waveshape of the input (as opposed to a sinusoidal waveshape) adds high-frequency components. Actually, even if the signal were sinusoidal in shape, the fact that it is time limited (i.e., a message has a finite length) introduces higher frequency components.

As mentioned above, the noise present on the bus signal is mostly higher in frequency than the signal. Low-frequency distortion is also possible; typically, it is a result of droop in the coupling and isolation transformers. There could also be some low-frequency noise coupled onto the bus. The amount should be low, however, since low-frequency noise couples onto a line much less easily than high-frequency noise. Experience has shown that there is little need for filtering of low-frequency noise.

There is no requirement in 1553B that covers the nature of the input filter. In fact, there is no requirement for one at all. There is only the need to meet the other 1553B requirements, most importantly the noise test (see 4.5.2.1.2.4 0f 1553B). Typically, receiver input filters are multipole low-pass designs; they start to roll off between 1 and 2 MHz. No low-frequency rejection filtering (high pass) is done directly. However, the isolation transformer (see 50.3.4) does reject low frequencies to some extent. The shunt capacitance of the isolation transformer contributes more rolloff at the higher end of the frequency response. The desired response of the input filter is one that band limits the received pulses as much as possible without adding significant distortion.

50.3.1.2 Current-and voltage-mode transmitters. Receivers differ in the states of their differential outputs while there is no voltage on the bus. Also, decoders differ in the states they require on their inputs when there is no voltage on the bus. Therefore, the proper type of receiver must be selected to match the decoder being used (or vice versa).

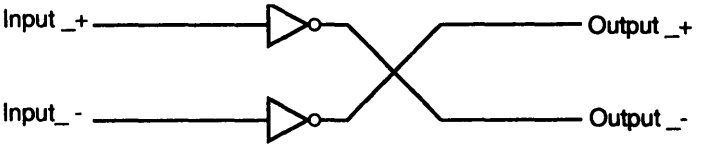
All receivers are required to provide a 1 on the OUTPUT_+ line and a 0 on the OUTPUT_— line when the INPUT_+ line is positive with respect to the INPUT_—line, and vice versa. Some receivers, however, set both OUTPUT_+ and OUTPUT_—to 0 with no signal on the bus, and some set them both to 1. A similar situation exists with decoders; some decoders require both differential inputs to be 0 when there is no signal on the bus, and some require both inputs to be 1.

If it is desired to connect a receiver and a decoder of the incorrect type, the receiver outputs may be inverted and swapped as shown in figure 50-3. This reverses the quiescent values of the outputs without changing the active states. Reference the truth table included in figure 50-3. This circuit changes an input with both lines at 1 to an output with both lines at 0 and changes an input with both lines at 0 to an output with both lines at 1, but leaves unchanged an input with one line 1 and the other 0.

50.3.2 Transmitters. The transmitter is the element in the terminal that drives the bus. It accepts as its input the digital signal from the encoder (typically differential TTL) and produces a signal on the 1553 bus that meets the requirements of 1553. It typically contains two drivers, one for each side of the differential 1553 bus. Each is designed to control the rise and fall times and the waveshape of the outputs. A transmitter also typically contains an inhibit input (XMIT_INHIBIT) by which it may be disabled. This input is used by the fail-safe timer (see 50.4.2) to turnoff the transmitter if, due to a failure condition, a transmission would last longer than 800 µs.

50.3.2.1 Current- and voltage-mode transmitters. There are two types of transmitters available today. These are the current-mode transmitter (figure 50-4) and the voltage-mode transmitter (figure 50-5).

A current-mode transmitter is one that produces a consistent output current. When loaded with a 70-ohm (or 35-ohm) resistor, as specified in 4.5.2.1.1. or 4.5.2.2.1 of 1553B, this consistent current produces a consistent voltage, but if the load varies from 70 (or 35) ohms, the output voltage will also vary. A voltage-mode transmitter is one that produces a consistent peak output voltage that does not depend greatly on load impedance. Another way of stating this is that the output impedance is fairly low (typically about 4 ohms). As



Input _+	Input_ -	Output _+	Output _-
0	0	1	1
1	1	0	0
1	0	1	0
0	1	0	1

Figure 50-3. Circuit to Change Quiescent States of Receiver Outputs

was discussed in section 40, the impedance that a terminal actually sees can vary quite a bit from the nominal value.

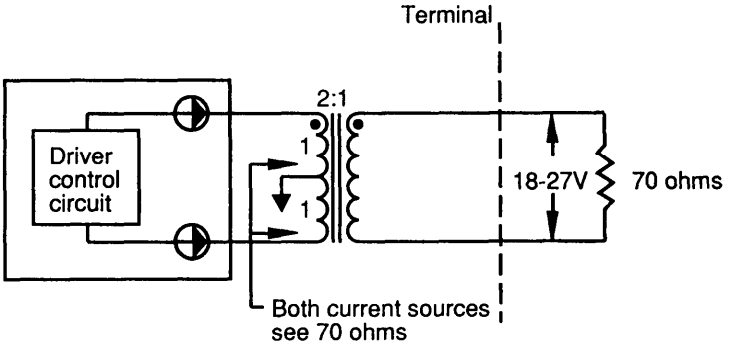
The isolation transformer turns ratios shown in figures 50-4 and 50-5 are for ransmitters that use a 15V power supply. A transmitter designed for a different supply voltage (e.g., 12V or 5V) requires an isolation transformer with a different turns ratio. However, the relative values of the turns ratios between different types of terminals will be consistent. For example, in Figure 50-4, the transformer used with a direct-coupled stub will have a turns ratio that is a factor of 1.4 (equals 2:1/1.4:1) less than the transformer used with a transformer-coupled stub.

Figure 50-4a shows a current-mode transmitter for connection to a transformer-coupled stub. Note that the transformer has a grounded center tap. There are two drivers in the transmitter, one connected to each half of the transformer winding. The winding direction of the transformer is such that the top driver drives the output positive. The bottom driver drives current in the transformer in the opposite direction to the top driver, thus producing a negative output. During a transmission, the top driver drives the positive half of the output pulse and the bottom driver drives the negative half.

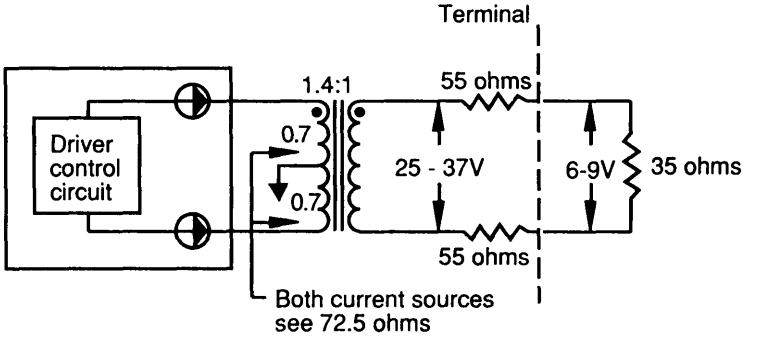
As required by 1553B, the transmitter produces an output amplitude of 18 to 27 V_{p-p} (Volts peak-to-peak), line to line, when connected to a 70-ohm resistive load. Typically, the output voltage is about 20 to 21 V_{p-p}. Since the network presents approximately this impedance to the terminal, this is approximately the output voltage of the terminal in a network. Each driver operates into a load of 70 ohms.

Figure 50-4b shows a current-mode transmitter for connection to a direct-coupled stub. The current drivers drive the transformer in the same fashion as discussed in the previous paragraph. The turns ratio of the transformer is different, though, to provide the correct terminal output voltage. The output voltage required by 1553B is 6 to 9 V_{p-p} when the terminal is connected to a 35-ohm resistive load. Because of the voltage-dividing effect of the two 55-ohm fault-isolation resistors, the voltage at the bus side of the transformer is 25 to 37 V_{p-p}. The driver operates into a load of 72.5 ohms, which is approximately equal to the 70 ohms for the previous (transformer-coupled) case.

Figure 500-5a shows a voltage-mode transmitter for connection to a transformer-coupled stub. The transformer does not have a center tap. The voltage-mode transmitter drives the complete winding of the



a. Transformer-coupled stub



b. Direct-coupled stub

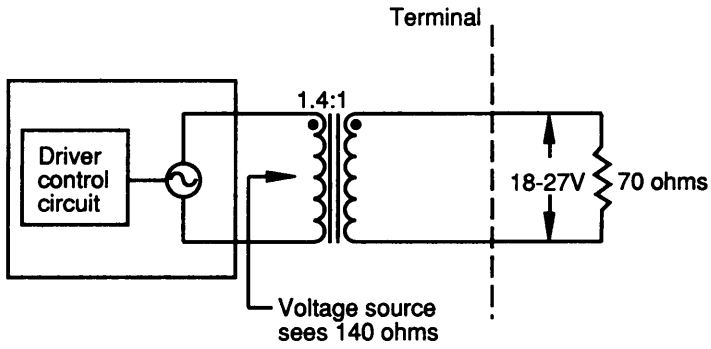
Figure 50-4. Current-mode Transmitters

transformer. The driver drives the transformer positive to produce a positive output and negative to produce a negative output. The terminal output voltage is still 18 to 27 V_{p-p} as required by 1553B. The-70-ohm resistive load through the 1.4:1 transformer presents a load of 140 ohms to the driver.

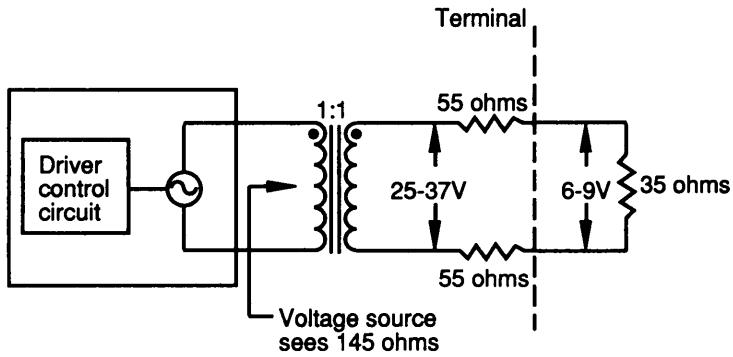
Figure 50-5b shows a voltage-mode transmitter for connection to a direct-coupled stub. It is similar to the transformer-coupled case; the difference again is the output voltage. The voltage at the bus side of the transformer is again 25 to 37 V_{p-p} to produce the terminal output voltage of 6 to 9 V_{p-p} required by 1553B. The driver sees a load of 145 ohms, again just about the same as the 140 ohms for the transformer-coupled case.

It is sometimes difficult to determine if a given part has a voltage-mode or a current-mode transmitter because these terms are not typically used on data sheets. One indication is the typical application circuit shown. If the isolation transformer has a grounded center tap (on the transmitter side), the transmitter is current mode. Voltage-mode transmitters use a transformer without a grounded center tap. The output impedance of a current-mode transmitter is usually not specified, since the output impedance of a current source is difficult to define. Voltage-mode transmitters usually do specify an output impedance. Finally, voltage-mode parts are larger and draw more power.

In summary, the advantages of these transmitters areas follows:



a. Transformer-coupled stub



b. Direct-coupled stub

Figure 50-5. Voltage-Mode Transmitters

a. **Voltage-mode transmitters-** Voltage-mode transmitters have lower output impedance. When driving a network with a highly reactive impedance, a lower driver impedance results in less distortion and less amplitude inconsistency in the output signal. Since a voltage-mode transmitter uses an input transformer with a different turns ratio, a terminal using it also has a higher input impedance (see 50.3.7.2). This tends to improve the network waveform integrity. They could also function better in a system in which the 1553 bus impedance changes dynamically (e.g., a system in which stores [devices carried by an aircraft and normally used up during a mission, like bombs or missiles] are disconnected from the bus as they are used), since their output doesn't change as much with a varying load impedance.

b. **Current-mode transmitters-** Current-mode transmitters tend to have lower power consumption, smaller packages, and lower cost.

50.3.2.2 Transmitter output loading. MIL-STD-1553A specifies the output characteristics of the terminal with the terminal connected to a bus system. On the other hand, 1553B specifies the output characteristics with a 70-ohm (±2%) resistive load (35 ohms for a direct-coupled stub). With the load specified in this fashion, there is no longer any benefit (from the standpoint of meeting the requirements of the standard) in the use of a voltage-mode transmitter. Note, however, that in a real system the impedance seen by the terminal does vary. See section 40 for this discussion.

50.3.2.3 Transmitter input requirements. A transmitter is generally driven from the encoder with two differential inputs. There is no problem of incompatibility with the transmitter inputs like the receiver output problem presented in 50.3.1.2. However, the inputs must be very closely balanced (with very little time skew between them). Standard encoders are designed to provide this. Otherwise, the Q and QN outputs of a flip-flop, or a similar circuit, is the recommended circuit to provide this, as opposed to use of an inverter to generate the negative input. If this guideline is not followed, there could be residual transformer currents at the end of transmissions or transformer saturation during transmission that cause tailoff in excess of the specified values (see 50.3.7.1).

50.3.3 Transceivers. Receivers and transmitters are generally packaged together as transceivers. Issues that really apply to the transceiver as a whole rather than to either part are discussed in this section.

50.3.3.1 Transceiver power consumption. Hybrid transceivers (or transmitters and receivers) consume a fair amount of power (seethe examples in 50.3.9 and 50.3.10 for typical values). This power consumption is of concern for two reasons. The first is the loading on the power supply and the second is that much of this power must be removed from the transceiver as heat.

Power supply loading calculations are no different than for any other circuit design task. It is necessary to provide a power supply for the system with sufficient capacity. Different transceiver designs consume different amounts of power. If low power is a design goal for a system, a transceiver with lower power consumption should be selected. Of course, the transceiver design must also be evaluated against other requirements.

The power dissipated by a transceiver causes its temperature to rise. Careful consideration must be given to this power in order to limit the temperature of the device to an acceptable value. There is typically one or several devices in a hybrid part that rise to a higher temperature than the rest of the hybrid. It is the temperature of these devices that is the limiting factor in the thermal calculation.

The transmitter dissipates more power when it is transmitting. There is some quiescent value, which is the amount of power dissipated when not transmitting. The extra power while transmitting is a linear function of the percent of the time the transmitter is transmitting (the duty cycle). Care must be taken when evaluating the data sheet of a transceiver because power dissipation is sometimes specified at duty cycles other than 100%. Thus, for a given physical environment (mounting method, ambient temperature, allowable part temperature, etc.), it is usually necessary to limit the duty cycle of the transmitter to prevent it from overheating. Sections 50.3.9 and 50.3.10 present two typical thermal calculations.

Current-mode transmitters generally dissipate less power than voltage-mode transmitters, and thus are desirable when high transmit duty cycles are necessary or in high ambient temperatures. It is also possible to lower the temperature of the device by reducing the thermal impedance from case to ambient by mounting the device on a heat sink.

50.3.3.2 Transceiver size. A transceiver is typically smaller than a combination of a transmitter and a receiver. A current-mode transceiver is typically smaller than a voltage-mode transceiver. If the size of the terminal is the overriding concern, a current-mode transceiver is the proper choice. Voltage-mode transceivers typically occupy an area of 1.6 in^2, or 3.2 in^2 for the two transceivers necessary in a dual redundant terminal. Current-mode transceivers are typically 1.1 in^2 per channel or 2.2 in^2 for a dual-channel system. Current-mode transceivers (but not voltage-mode) are available in a package that contains two independent transceivers with an area of about 1.5 in^2.

50.3.3.3 Other transceiver considerations. Other features that are sometimes included in transceivers are:

a. **Fail-safe timer-** Some transceivers include the fail-safe timer (see 50.4.2) internally. This may lower the parts count for the terminal. However, most of the available transceivers with this feature use an analog timer, which may not be desirable.

b. **Over-temperature shutdown-** Some devices include a temperature sensor that shuts down the transmitter if it gets too hot. This protects the part from damage, so it is desirable. However, this feature increases the cost and may slightly decrease the device reliability. The impact of a device with this feature on system performance should be considered and evaluated.

c. **Output short circuit protection-** Some devices are protected against short circuits applied to their outputs. This could be used to protect parts in debugging or breadboarding activities. Note that this is somewhat inherent in the design of a current-mode transmitter.

d. **Input threshold adjustment-** some receivers allow the input voltage thresholds to be adjusted. It may be desirable to adjust the voltage thresholds to alter the noise performance for some special applications. Receivers are generally supplied with the input voltage threshold adjusted for optimum performance, and the range of acceptable threshold values is not wide. Input voltage thresholds are discussed in 50.3.7.2.

e. **Output voltage adjustment-** Some transmitters offer adjustable output voltage. This feature could be very useful in the design of test equipment but is of limited usefulness otherwise.

There are several vendors producing transceivers that are nominally pin-compatible with one another. The single-channel model is available in a 24-pin by 600-mil-wide package and the dual-channel model is available in a 36-pin by 600-mil-wide package. These parts are only functionally similar, though; they are not identical. That is, they are not interchangeable in all designs, although they are interchangeable in some designs. These parts differ in several possible ways. For example:

a. **Power supply voltages-** There are parts that use the following combinations of supply voltages.

- o +5, +15, —15
- o +5, +15
- o +5, —15
- o +5, +12, —12
- o +5, +12
- o +5, —12
- o +5 only

The three-supply parts vary in the amount of current drawn from the +15V and—15V (±12V) supplies; some parts draw most of their current from the +15V (+12V) supply, and some draw most of their current from the—15V (—12V) supply. In substituting parts from different vendors, the designer must ensure that his power supplies are capable of providing the required currents and voltages.

In general, the older parts require three supplies, and the newer ones use one or two supplies. The older parts dissipate more power for the same output and are therefore less efficient. The 12V versions are somewhat more efficient than the 15V designs. 15V supplies are more commonly available in existing systems and power supplies, though, and are thus probably cheaper and easier to provide. The choice of which transceiver version to use depends on the power that is available. Higher efficiency units are generally preferred since they allow cooler operation or require less cooling for operation at required transmit duty cycles.

b. **Extra features-** The inclusion or exclusion of some of the extra features discussed previously also affects interchangeability. If interchangeability of parts from different vendors is a high priority, then it is advisable not to select parts which incorporate extra features. The inclusion or exclusion of a feature should be considered and evaluated for its effect on system performance.

c. **Receiver output state-** Another major difference between transceivers is the state of the receiver outputs with no voltage on the bus, as discussed in 50.3.1.2 above.

50.3.4 Transformers. The other major analog component is the isolation transformer. There is no specific requirement in 1553B for an isolation transformer. It is interesting, however, that 1553B figures 9 and 10 do show an "isolation transformer" on the input of the terminal. It turns out that an isolation transformer is the most appropriate design choice to meet the terminal characteristics specified in 1553B, especially the common-mode rejection ratio (CMRR) requirement.

As in the case of the transceiver, transformers are usually not custom designed. There are many available off-the-shelf that are specifically designed to work with available transceivers to meet the requirements of 1553B. MIL-T-21038/27 is a military specification sheet for appropriate transformers. Care is necessary with this selection, however, as not all transceivers work properly with all transformers. This section concentrates on specifications of purchased transformers and their effects on terminal performance.

50.3.4.1 Transformer turns ratio. The most important criterion for selection of an isolation transformer is its turns ratio. Transformer-coupled and direct-coupled transmitters are designed to drive different loads and thus have different output characteristics. A transmitter for a direct-coupled stub must drive a load of about 145 ohms with an output voltage of 25 to 37 V_{p-p}. (this is the load and the voltage into the fault-isolation resistors that are actually part of the terminal). In comparison, a transmitter for a transformer-coupled stub must drive a load of about 70 ohms with an output voltage of 18 to 27 V_{p-p} By changing the turns ratio of the transformer, the load impedance can be transformed so that the transmitter sees the same load for both cases. Thus, the same transmitter design is able to meet both these requirements. This solution is easier than designing a transmitter to drive loads of different impedance.

Proper selection of the isolation transformer turns ratio also enables transmitters with different power supply voltages to output correct voltage levels. For example, transmitters that require only a +5V supply require a transformer with a significant step up to achieve the appropriate output voltage levels.

50.3.4.2 Transformer input impedance. The isolation transformer affects the input impedance of the terminal. The requirement in 1553B (4.5.2.1.2.3 and 4.5.2.2.2.3) is that the input impedance must be greater than 1000 ohms (2000 ohms for terminals for direct-coupled stubs) for frequencies between 75 kHz and 1.0 MHz. This imposes an absolute minimum primary (i.e., bus side) inductance of approximately 2.1 mH and an absolute maximum shunt capacitance of approximately 159 pF (4.2 mH and 80 pF, respectively, for terminals for direct-coupled stubs). It should be noted that transformer inductance varies substantially with temperature. The minimum values stated above apply over the full operating temperature range. In practice, the transmitter and receiver are connected to the secondary (i.e., terminal side) of the transformer, so their impedances appear in parallel with the transformer, thereby reducing the input impedance of the terminal. As a result, transformer inductance and shunt capacitance must fall substantially within the absolute limits stated above.

Isolation transformer inductance may be increased by adding more turns, but this also increases shunt capacitance, so a tradeoff is necessary. A higher core permeability also increases inductance with the same number of turns. These design considerations have been taken into account by vendors of 1553B transformers, and there are many compliant transformers available.

50.3.4.3 Transformer common-mode rejection. Another 1553B requirement (specified in 4.5.2.1.2.2 and 4.5.2.2.2.2) is common-mode rejection. The standard states that a terminal must be able to operate without error in an environment with up to ±10 V_p common-mode input at frequencies from DC to 2 MHz. To meet this requirement, the CMRR of the isolation transformer should be above 27 dB (see 50.3.7.2). The common-mode requirement is the major reason that the terminal includes an input transformer. A transformer designer attains good common-mode rejection by paying proper attention to shunt capacitance and core-to-winding capacitance during the design phase. As with the input impedance requirements discussed above, these design considerations have been taken into account by vendors of 1553B transformers, and there are many compliant transformers available.

50.3.5 Fault-isolation resistors. Terminals for direct-coupled stubs require two fault-isolation resistors between the terminal output and the bus connection (Figures 50-4b and 50-5b). The value of these resistors is required to be 55 ohms ±2% (4.5.1.5.2.1 of 1553B). Their function is to isolate the bus from a terminal that has shorted (i.e., a terminal that, due to some failure, is presenting an abnormally low impedance to the bus). The fault-isolation resistors keep the load that the terminal puts on the bus greater than 110 ohms. Paragraph 4.5.1.5.2.3 of 1553B requires that a transmitter output its specified voltage when one terminal on the bus is presenting its fault impedance of 110 ohms. In effect, this requires that the bus system continue to operate properly (for the other terminals on the bus) when one terminal has failed in a shorted mode.

Since these fault-isolation resistors are located in the terminal, they cannot have any effect on shorts that occur in the stub wiring to the terminal. They will protect the bus only from shorts that occur downstream of the resistors. Because a short is more likely to happen in the wiring external to a terminal than inside the terminal, the value of the fault-isolation resistors in a direct-coupled stub terminal is marginal. Nonetheless, 1553B requires that they be used.

Terminals for transformer-coupled stubs do not include fault-isolation resistors. For these terminals, the fault-isoiation resistors are included in the stub coupler, but except for their physical location, they provide exactly the same function. See section 40 for a discussion of stub couplers and the fault-isolation resistors that they may include.

Fault-isolation resistors should be selected for minimum series inductance and parallel capacitance. They must also be selected for sufficient power-handling capability. It is recommended that fault-isolation resistors be capable of dissipating the maximum power that the terminal can produce (i.e., transmitting 100% of the time). Other than these considerations, any resistor that meets the resistance and tolerance requirements is satisfactory.

50.3.6 Fail-safe timer. The fail-safe timer may be implemented as an analog timer or as a digital timer. It is discussed with the digital section of the terminal (see 50.4.2).

50.3.7 Meeting 1553B analog requirements. This section discusses in more detail the sections of 1553B that directly affect the analog (or front end) portion of the terminal. They are found in paragraphs 4.5.2.1, 4.5.2.2, and 4.6.1 of 1553B. The pertinent paragraphs are listed at the end of the title of each subsection. When two paragraphs are listed, the first applies to terminals for transformer-coupled stubs and the second applies to terminals for direct-coupled stubs. Also note that some of these requirements are met (at least partially) by the digital portion of the terminal (see 50.4).

50.3.7.1 Terminal output characteristics (4.5.2.2.1) The output characteristics of terminals for direct-coupled stubs are measured with the terminal driving a resistive load of 35 ohms ±2%. Terminals for transformer-coupled stubs are tested with a 70-ohm ±2% resistive load. Note that this resistive load does not necessarily match the load that the terminal sees in actual operation. See section 40 for more discussion about the load a terminal sees in actual system operation. These values were chosen for test convenience and consistency.

Output levels (4.5.2.1.1.1 and 4.5.2.2.1.1). The standard specifies that terminal output signals shall have an amplitude of 18 to 27 V_{p-p} (6 to 9 V_{p-p} for direct-coupled stubs). This can be achieved by selecting a transmitter of adequate power to drive a transformer with the proper turns ratio for the power supply used by the transmitter.

Output waveform (4.5.2.1.1.2 and 4.5.2.2.1.2). This paragraph specifies several requirements on the waveform output by a transmitter. Figure 50-6 shows these requirements graphically.

a. The output zero-crossing error shall be less than ±25 ns from ideal. That is, the Manchester encoded waveform shall have zero-crossing intervals of 500, 1000, 1500, or 2000 ns, all ±25 ns, as appropriate.

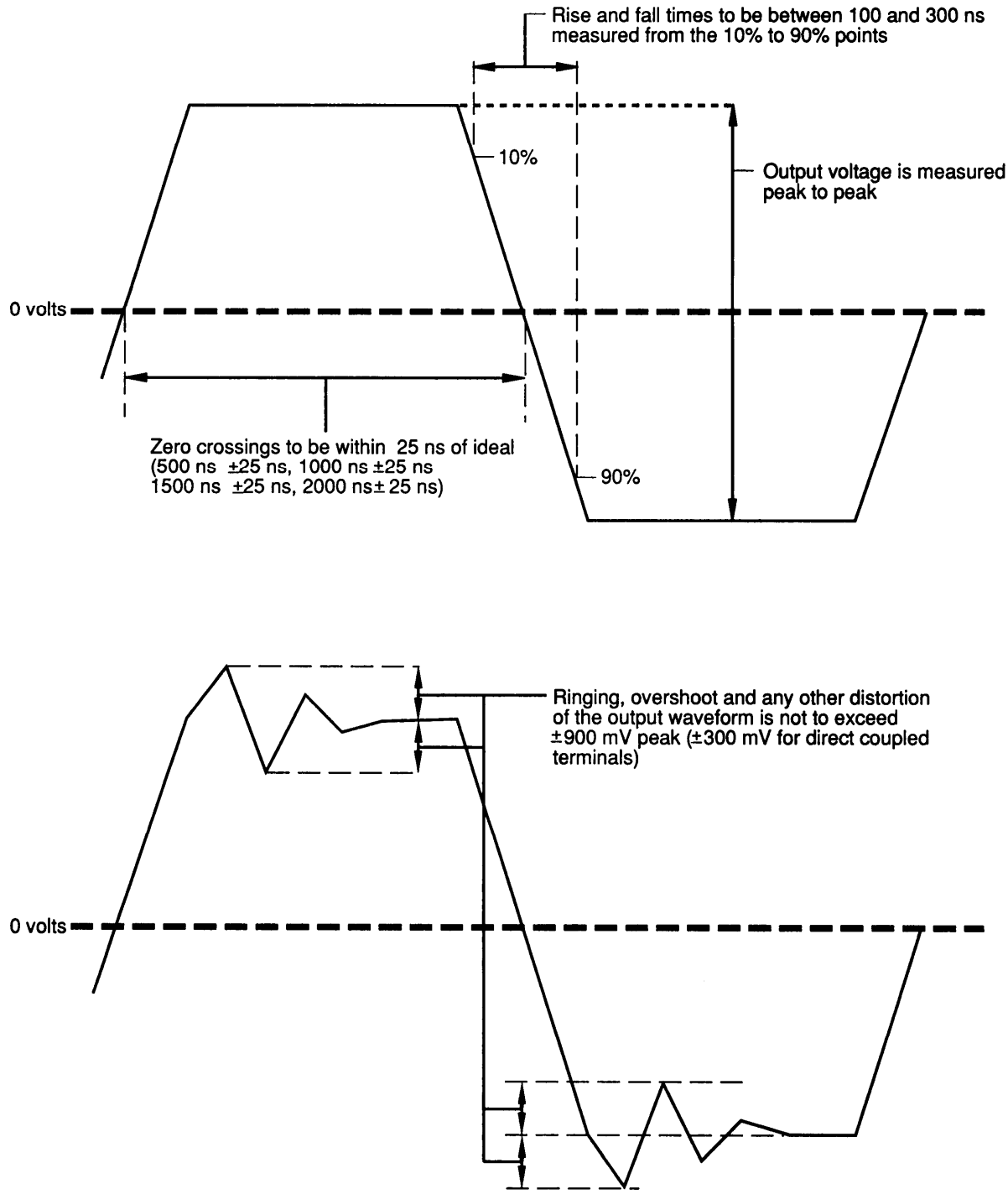


Figure 50.6 Terminal Output Waveform Parameter Definitions

b. The rise and fall times of the waveform measured from the 10% to 90% points shall be between 100 and 300 ns.

c. Any distortion in the waveform including overshoot and ringing shall be less than ±900 mV_p(±300 mV_p for direct-coupled stubs).

To meet the first condition, an accurate clock must first be supplied to the terminal. A terminal that meets the requirements of 4.3.3.3 of 1553B (which states that the transmission rate must be 1.0 MHz ±0.1%) should have no trouble with this. Transmitter positive and negative drivers must have exactly equal delays. Also, the encoder's outputs to the transmitter must both switch at exactly the same time. The combined error of these last two effects must not exceed 25 ns to meet this requirement.

The rise and fall times are preset internally in a transmitter and typically range between 150 and 250 ns. In present transmitters, the output is usually shaped simply by limiting the rate of change of the output. This produces a trapezoidal waveform. To reduce power dissipation, the rise and fall times of most transmitters are closer to 100 than 300 ns. This follows from the fact that, when the voltage is between its maximum and minimum values (in the rising or falling portion of the output signal), the output transistors are not saturated and, hence, are dissipating more power.

The distortion limitation of ±900 mV (±300 mV for direct-coupled stubs) limits the amount of ringing or overshoot that can appear on a transmitted signal. Meeting the distortion, overshoot, and tinging requirements is ensured by proper transmitter design as well as proper selection of transformer characteristics(in particular, leakage inductance).

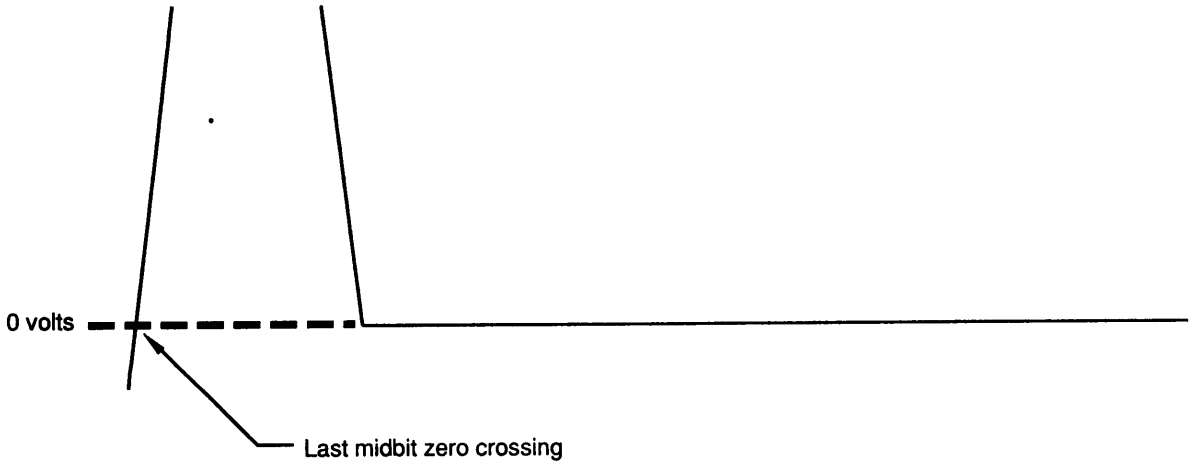
Output noise (4.5.2.1.1.3 and 4.5.2.2.1.3). When in a receiving mode (i.e., the transmitter is off and nottransmitting) or with power off, a terminal may not output more than 14 mV_{rms} (line to line) of noise (5 mV_{rms} for direct-coupled stubs). To meet this requirement, a transmitter design that is tolerant of power supply and logic noise must be used. Proper power supply bypassing will reduce the noise. Routing of input and output wiring away from sources of noise is generally necessary. A transformer that has a high CMRR (from input to output) also cuts down on the amount of quiescent noise because much of the power supply (and other) noise coupled into the terminal appears as common-mode noise.

Output symmetry (4.5.2.1.1.4 and 4.5.2.2.1.4). The 1553B paragraph on output symmetry states that the voltage on the bus shall be less than ±250 mV for the period beginning 2.5 µs after the last midbit zero-crossing of the last bit of a message (less than ±90 mV for direct-coupled stubs). The voltage present on the stub at the end of a message shall be called "tailoff".

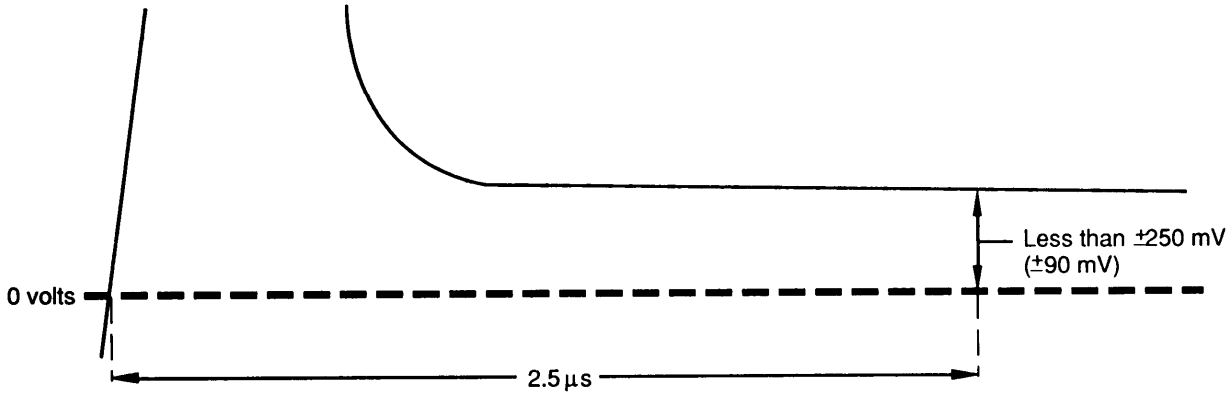
Figure 50-7 shows the last half-bit of three transmissions. Figure 50-7a shows the ideal case. Figure 50-7b shows a case with no ringing that slowly decays toward zero from the positive direction. Figure 50-7c shows a case with quite a bit of ringing that eventually settles down toward zero from the negative direction. All three cases are satisfactory. The requirement is only that the voltage be below the limit at 2.5 µs and all times thereafter.

The distortion (overshoot and ringing) specification (in 4.5.2.1.1.2 and 4.5.2.2.1.2 of 1553B) also applies to the last transition of the transmission, limiting any ringing to 900 mV_p (300 mV_p for direct-coupled stubs). Thus, the signal would be limited to 900 mV_p during the time between the end of the transmission and 2.5 µs.

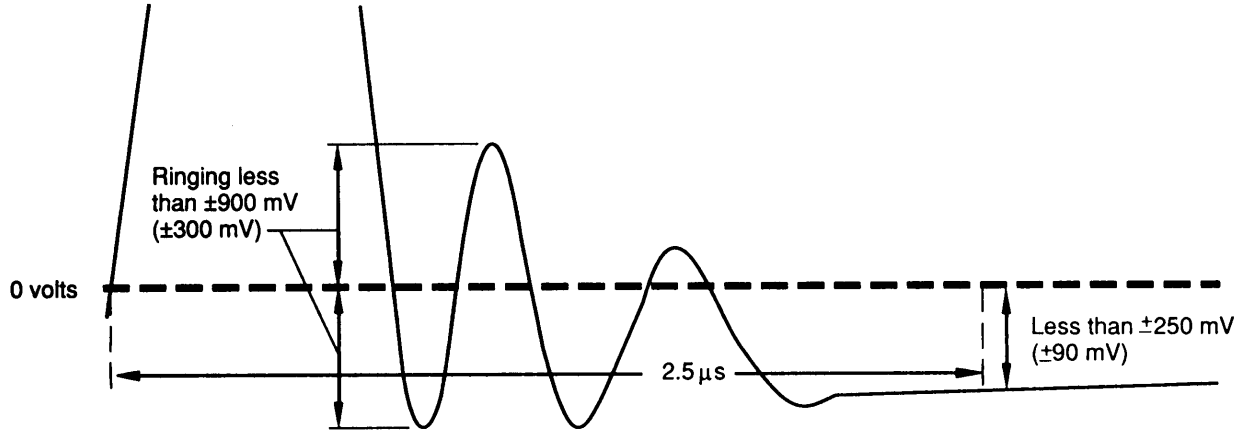
The value allowed for tailoff (250 mV) was originally chosen to "protect" a terminal's input from transmissions of all the other terminals on the bus, but not from transmissions of the terminal itself. In the case of a transformer-coupled stubs, only 1/4 of the voltage on the output of a terminal appears on the input stub of another terminal (due to the coupling transformer turns ratios and the voltage-dividing effect of the fault-isolation and bus-terminating resistors). In order to achieve the same level of protection from its own transmissions, a terminal's tailoff should be less than 250/4 or 62 mV. This would only be of concern in a system if back-to-back transmissions to the same terminal (i.e., transmissions only 4 µs apart) were envisioned.



a. Ideal case with no tailoff or ringing



b. With positive decaying tailoff



c. With ringing and negative decaying tailoff

Figure 50-7. End of Transmission

The title (output symmetry) results from the fact that this tailoff is primarily caused by lack of symmetry in the transmitter. If the positive area of the transmitter output voltage waveform does not equal the negative area of the waveform, a residual current will exist in the isolation transformer at the end of a transmission. This current driving into the load impedance will cause a tailoff voltage, which decays exponentially depending on the value of the load resistance and inductance. A primary (i.e., bus side) inductance on the isolation transformer (or stub coupling transformer) that is too low will cause the tailoff voltage to be higher but to decay faster.

If the transformer primary inductance is near the minimum value of 2.1 mH (4.2 mH for direct-coupled stubs) calculated earlier to meet the input impedance requirement (see 50.3.4.2), tailoff voltages will be higher than may be desirable. To keep the tailoff voltages to reasonable values (i.e., so that the terminal meets the output symmetry requirement), the primary inductance should be higher, typically 7 or 8 mH. Also, note that transformer inductances are much lower at Iow temperatures; transformers must be designed for the minimum value of inductance at the lowest temperature they will ever see, typically, for military applications, –55°C. See also the discussion in section 40 about the effect on the bus network of low transformer primary inductance.

The transformer is the major contributor to tailoff, but the transmitter and the layout of the circuit certainly contribute also. Some transceiver designs are less sensitive to transformer properties (with respect to tailoff) than others. With off-the-shelf transmitters, the only real way to know how a given transmitter will perform is to test it. Also, locating the transformer on the circuit board farther from the connector increases the tailoff distortion. Therefore, it is recommended that the transformer be kept as close to the edge of the card as is practical.

Different transmitted data words produce different tailoff voltages. For example, a transmitted data word of all zeros, in the absence of any imbalance of any sort, produces a negative tailoff. This “default tailoff is caused by the noninfinite load inductance and transmitter output impedance.

Circuit imbalances add to this default tailoff to produce the actual tailoff voltage. 1553B specifies that the maximum number of words allowable (usually 32) be transmitted. Sending the maximum number of words is assumed to be the worst case, although, due to the exponentially decaying nature of tailoff voltage, only the 10 to 12 most recently transmitted words make significant contributions to the tailoff. The standard also specifies that the test be done six times, with all the data words in each transmission set to 8000, 7FFF, 0000, FFFF, 5555, and AAAA (hexadecimal). One or the other of these data word patterns should be the worst case, as determined by the experience of transmitter users. Note that different transmitter designs display their worst tailoff with different data word patterns.

Output symmetry should be tested over the temperature range at which the terminal is required to operate. Imbalances often result from mismatch in the driver transistors, and these properties are often temperature dependent. Another relevant property that varies with temperature is transformer inductance.

Current-mode transmitters use the two halves of the secondary of the isolation transformer (i.e., with a grounded center tap) as part of the circuit. It is therefore important that these two halves of the secondary winding be balanced as closely as possible. The two halves should be balanced not only for number of turns, but also should have balanced leakage inductances (as small as possible) and parasitic capacitances.

50.3.7.2 Terminal input characteristics (4.5.2.1.2and 4.5.2.2.2). 1553B states that the input characteristics specifications must be measured (met) independently. Hence, it is reasonable to assume that the terminal need only be tested for (and function properly for) one worst case condition at a time.

Input waveform compatibility (4.5.2.1.2.1 and 4.5.2.2.2.1). 1553B also states that a terminal must be able to correctly decode incoming signals that have up to ±150 ns of error in any time interval between zero-crossings. Dealing with received waveform timing errors is primarily a function of the decoder (see 50.4.1). The role of the analog front end is to remove high-frequency distortion and to add as little error as possible to the input waveform.

Receivers typically contain two comparators and two outputs to the decoder. One has a negative threshold and thus detects negative excursions of the input (bus) signal and the other has a positive threshold and detects positive excursions. Since the transition time of the bus waveform is required to be at least 100 ns, the transitions in the two receiver outputs take place at different times than the actual zero-crossing. One changes a little earlier and the other changes a little later. The time of the actual zero-crossing will be between these two times. Ideally the zero-crossing will have happened halfway between the transitions of the two outputs, but unbalanced comparator thresholds modify this. Because the decoder typically assumes that the comparator thresholds are balanced, this could introduce additional zero-crossing errors into the signal seen by the decoder.

Figure 50-8 shows this graphically. The output of the positive comparator is RCV_OUT. RCV_OUT/ is the output of the negative comparator. $v_{threhold+}$ is the threshold of the positive comparator, and $V_{treshold}$ is the threshold of the negative comparator. As the Figure shows, the pulse on RCV_OUT is narrower than a positive pulse in the 1553 bus signal and the pulse on RCV_OUT/ is wider. Correspondingly, the pulse on RCV_OUT is wider (and on RCV_OUT/ is narrower) than a negative pulse in the 1553 bus signal.

Another potential contributor to receive zero-crossing error is unequal propagation delay through the receiver for negative versus positive going signals. The net effect at the output would be the same as comparator threshold imbalance. In both cases, balance between the two halves of the receiver is necessary for best operation.

MlL-STD-l553B states that terminals for transformer-coupled stubs shall respond to input signals of 0.86 to 14 V_{P-P} and shall not respond to signals less than 0.20 V_{P-P} (1.2 to 20 V_{P-P} and less than 0.28 V_{P-P} for direct-coupled stubs). To state this another way, the input threshold of the terminal, which is the voltage at which it detects an input signal, must be less than 0.86 V_{P-P} and greater than 0.20 V_{P-P} (1.2 V_{P-P} and 0.28 V_{P-P}). To state it still another way, the positive and negative input thresholds must each be less than 0.43 VP and greater than 0.10 V_P (0.60 V_P and 0.14 V_P) if the positive and negative thresholds are balanced. The analog front end design has a large effect on whether the terminal meets these requirements.

To meet these requirements, the terminal designer must first choose an isolation transformer with the correct turns ratio. Thus, the receiver input sees the voltage for which it was designed. The input voltage threshold of the receiver is normally fixed by the receiver manufacturer. Receiver thresholds are usually close to the maximum allowed value of 0.86 V_{P-P} (1.2 V_{P-P}) to enhance the noise-rejection characteristics. (See 50.4.1.3 for further discussion of noise rejection.)

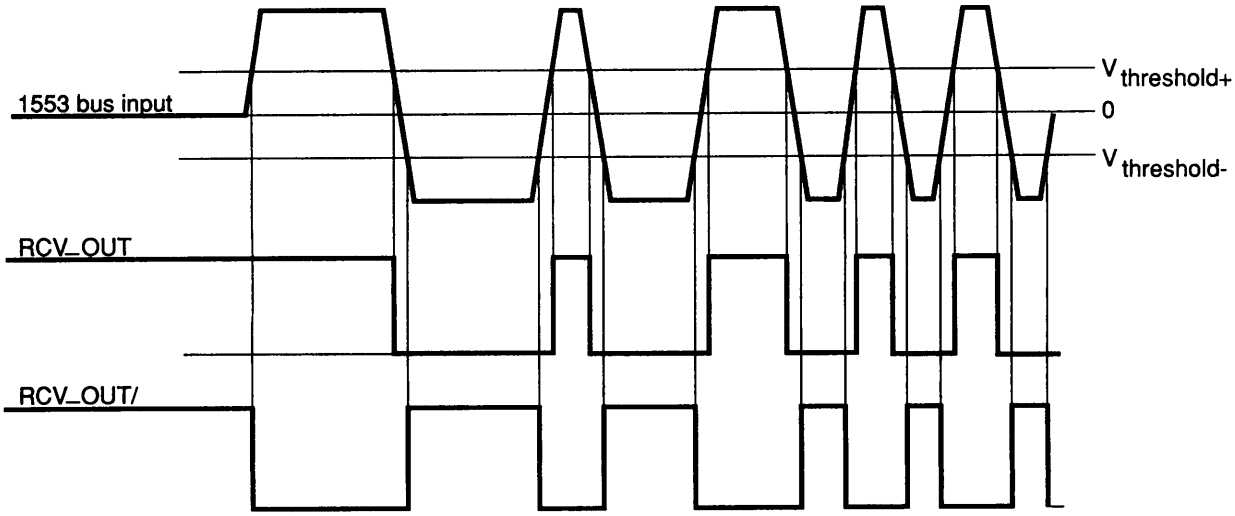


Figure 50-8. Receiver Waveform Decoding *Process*

The decoder also plays a role in determining the effective threshold of the terminal. As input amplitude is lowered, zero-crossing error could be introduced into the signal due to the nonzero rise and fall times of the input signal as discussed above. As the voltage of the input signal falls toward the threshold value, the signal is below the threshold for a greater part of each bit time. There will thus be a greater difference in the transition times of the receiver outputs from the actual zero-crossings. The decoder's method of measuring its two inputs to determine the actual times of zero-crossings determines its sensitivity to this kind of error. A decoder that didn't handle this well could reject a word because of zero-crossing errors even though the receiver detected it properly (i.e., it was above threshold). It is therefore necessary to evaluate the receiver and decoder together for proper operation. Paragraph 50.4.1.2 discusses this point further.

Common-mode rejection (4.5.2.1 .2.2 and 4.5.2.2.2.2). This requirement in 1553B is fairly vague. On one hand, it is stated in 4.5.2.1.1 or 4.5.2.1.2 that the input conditions are to be imposed separately. At the same time, this paragraph states that acommon-mode signal shall not degrade terminal performance, which implies that there is a set of conditions under which the degradation is measured. Most simply, to not degrade the performance of the terminal the common-mode rejection would have to be infinite.

The ratio of the minimum input voltage to which the terminal may respond (interminals for transformer-coupled stubs) of 200 mVpp to the common-mode voltage requirement of ±10VP (or 20 V_{p-p}) is 100:1 or 40 dB. If the terminal threshold was just above the minimum allowed, a common-mode rejection of less than 40 dB could allow the terminal to see a common-mode signal as a real signal, which would presumably degrade the terminal performance. To define a measurable requirement, some assumptions must be made. The RT validation test plan (5.1 .2.2 of section 100 of this handbook) performs this test (for terminals with transformer-coupled stubs) using an input signal of 0.86 V_{p-p} (which is the minimum input voltage at which a response is required) and a common-mode signal of ±10V, thus verifying that the terminal will correctly reject common-mode signals that are 27 dB above the desired signal.

An ideal transformer, of course, has infinite common-mode rejection. Most of the terminal's common-mode rejection is a result of its isolation transformer. To meet this requirement, a proper transformer must be selected or designed. Any impedance in the input wiring of the terminal will cause a voltage drop. Any imbalance in impedance between the two differential lines of the input will generate a differential voltage from a common-mode voltage. It is therefore important to keep any stray impedances in the input wiring as small as possible and, more importantly, matched for the two halves of the differential signal.

Input impedance (4.5.2.1 .2.3 and 4.5.2.2.2.3). Terminal input impedance is a function of the isolation transformer, the parallel combination of the transmitter and receiver, and the interconnect wiring.

As discussed in 50.3.2.1, a voltage-mode transmitter uses an isolation transformer with a smaller turns ratio than a current-mode transmitter (see figures 50-4 and 50-5). A current-mode transmitter will use a transformer with a turns ratio that is a factor of 1.4 greater. Typically, current- and voltage-mode transmitters do not differ in input impedance. The input impedances of the transmitter and receiver are transformed by the square of the turns ratio of the isolation transformer. Therefore, the input impedance of the transmitter and receiver will have twice as great an effect (i.e., half the value in parallel with the other components) on terminal input impedance for a terminal with a current-mode transmitter. Thus, input impedance is somewhat higher for a terminal with a voltage-mode driver than for one with a current-mode driver.

The shunt capacitance of the interconnect wiring degrades terminal input impedance. This wiring should be kept as short and direct as possible to minimize this. The isolation transformer and transceiver (or transmitter and receiver) should be located on the terminal card as close to the connector as practical. The effects of running the bus connections through a printed circuit motherboard should be evaluated. These traces must be designed for proper characteristic impedance and low capacitance. The bus connecting wires may also be run separately (i.e., not through the motherboard).

In measuring the input impedance, it is very important either to eliminate or to account for stray impedances in the test setup, particularly shunt capacitance. Note that stray impedances in the terminal forma legitimate

part of the input impedance and hence cannot be ignored. Input impedance will also vary significantly with temperature, so it should be measured over the range of temperatures at which the terminal is required to function.

Terminal input impedance is important for proper system operation. For example, if the input impedance of a transformer-coupled terminal is 500 ohms (rather than the 1000 ohms required), the bus voltage could drop by as much as 30 %. Also, input impedances are typically complex. Thus, their magnitudes vary with frequency and hence cause distortion of the bus waveform which leads to zero-crossing errors and amplitude degradation. It is desirable to keep terminal input impedance as high as possible to minimize these effects.

Noise rejection (4.5.2.1 .2.4 and 4.5.2.2.2.4). Terminal noise rejection is tested with a stub signal input voltage of 2.1 VP-P (3.0 VP-P for direct-coupled stubs) with added white Gaussian noise of 140 mVrms (200 mVRms. The noise is to be distributed over a bandwidth of 1 kHz to 4 MHz. Under these conditions, the word error rate must be less than 1 in 10,000,000. That is, the terminal may incorrectly decode no more than 1 word in 10,000,000 words sent to it. An incorrectly decoded word is indicated by a no-response of the RT or a status word in which the message error bit is set.

Table II in 1553B states how many words must be sent to the terminal without error, or with a stated number of errors, to have a high confidence level (statistically) that the word error rate is less than 1 in 10,000,000. The test can still pass even though there are a few word errors (up to 40). The test passes if, for the number of errors that have occurred, the total number of words sent to the terminal is greater than stated in the “Accept” column of table Il. The test fails if, for the number of errors that have occurred, the total number of words sent to the terminal is less than stated in the "Reject” column of table Il. The test takes a fair amount of time to run because a minimum of 44,000,000 words (and possibly up to 330,000,000) must be sent to the terminal. For 44,000,000 words, it takes an absolute minimum of 15 minutes and 12 seconds to send (32-word messages; minimum intermessage gap and response times of 4 us).

The spectrum of the noise source used is very important. The spectrum should be as flat as possible. That is, there should be the same power level at all frequencies of interest. Though this isn’t stated specifically in 1553B, the statement “white Gaussian noise distributed over a bandwidth of 1.0 kHz to 4.0 MHz” does imply this because, by definition, Gaussian noise has a constant noise power per unit bandwidth. Due to the filtering at the front of the terminal, the very low and very high frequencies are rejected. The frequencies between about 75 kHz and 1 MHz are passed very well. The RMS voltage measurement effectively averages the voltages at all frequencies. If there is relatively more noise power in the middle of the range (i.e., 75 kHz to 1 MHz), the terminal is being subjected to a more stringent test than planned. Likewise, if the power concentration in the noise spectrum is not in the middle region, the testis too easy. The noise spectrum given was chosen after analysis of typical systems and the types of coupled interference that were actually encountered (the most common being random and periodic impulsive type noise).

There are several noise testers available today to perform this test. Some are complete, requiring only that the terminal under test be plugged into the tester. Some are only noise sources that depend on another unit to send messages, count errors, and calculate the results based on Table II of 1553B.

50.3.7.3 power on/off noise (MIL-STD-1553B Notice 2 paragraph 30.10.6). A terminal may not emit more than ±250 mV_p (90 mV_p for direct-coupled stubs) of spurious output while power is being applied to or removed from the terminal. Transmitters should be designed not to emit spurious noise, although the specification sheets for most of them do not address this issue. Transmitters should be evaluated for spurious noise emission as part of the design process. In any case, if a transmitter emits noise during power-up or power-down, and Notice 2 is a requirement on the terminal design, a different transmitter must be selected.

The designer must also ensure that the encoder remains quiescent (i.e., doesn’t output anything to be transmitted) on power-up and power-down. This can be accomplished by holding the encoder reset until power supply voltages are stable (on power-up) and reapplying the reset before power supply voltages reach a point where logic could be corrupted (on power-down or during a power glitch). No matter how good the

The designer must also ensure that the encoder remains quiescent (i.e., doesn't output anything to be transmitted) on power-up and power-down. This can be accomplished by holding the encoder reset until power supply voltages are stable (on power-up) and reapplying the reset before power supply voltages reach a point where logic could be corrupted (on power-down or during a power glitch). No matter how good the transmitter design is, if the encoder output (which is the transmitter input) is noisy during power-up and power-down, the transmitter could well transmit this noise. A soft-starting controlled-rise-time power supply may also help ensure that no spurious noise occurs when the power is turned on.

50.3.7.4 **Isolation between buses (4.6.1.)** the active and quiet buses for a redundant terminal is specified to be 45 dB. That is, the output on the channels not being driven must be at least 45 dB less than on the desired channel. There are several design properties that affect this. Transmitters should have good power supply rejection ratios. Because transmitters are devices with fairly high currents, some of the signal is bound to appear on the power leads during the transmission due to variations in supply currents, though the addition of proper local bypass capacitors to the supplies minimizes this. This signal could then couple into the transmitter on the other channels on its power supply pins and may cause it to output a signal. Transceiver manufacturers generally specify a method of power supply bypassing for their part. In many cases, the part will not even function if not bypassed correctly due to the amount of current needed to drive the bus.

Signals can also couple to the other channels through ground current return paths. Inadvertent signals can couple not only into the transmitter itself, but also, for current-mode transmitters, into the grounded center tap of the isolation transformer. Good grounding practices should be followed. Avoid ground loops and make all ground connections short and of low impedance. Separate the analog and digital grounds. These should be tied together only at the power supply. This also Iessens the coupling of digital noise into the transmitted signal or having digital noise corrupt a received signal. Keep each power supply line close to its return and as short as practical. Note that transmitters (and transceivers) usually have more than one analog ground per channel. These must be individually connected to the analog ground of the LRU.

The physical layout of the printed wiring assembly deserves some attention. It is desirable that trace lengths to both received data inputs and transmitted data outputs of the transceiver be of similar length and as short as possible. This tends to eliminate any skew being introduced to the data by uneven loading. It is usually desirable that transceivers be located near the edge of the board to provide a lower thermal resistance from the part to the cooling source. This also helps to keep the power and ground lines as short as possible.

50.3.8 **Analog specification conflicts.** 1553B specifies certain worst case conditions for which a terminal must function properly. A question that may arise is how many of these worst case conditions must be met at the same time? In 1553B it is clear (4.5.2.1.2 and 4.5.2.2.2) that each input requirement need only be met by itself. That is, when testing a terminal for zero-crossing errors on its input, for example, the signal voltage should not be set to its minimum value of 0.86Vp-p.

Validation test plans for RTs and BCS (see sections 100 and 110) have been written. The writers of these plans have resolved these conflicts and have chosen particular methods of testing each requirement. Although no test can test everything in 1553B, these plans are quite complete. If the appropriate validation test plan is called out as a requirement for a given terminal design, it is generally accepted that a terminal meets the requirements of 1553B if it passes the validation test.

50.3.8.1 **Input zero-crossing test.** An example of the nonapplicability of two worst case conditions at once is the low-amplitude and input zero-crossing error tests. When the input signal amplitude is just above threshold, it follows that the signal is below threshold during the rise and fall time intervals. The signal, remember, is changing from just above the positive threshold to just below the negative threshold. The signal is in the region below threshold for almost the entire 100-to 300-ns rise and fall time. Stated another way, the signal zero-crossing is uncertain during this 100-to 300-ns interval when both receiver outputs are off. A good decoder design should compensate for this to some extent (see 50.4.1.3), but the inevitable difference between the positive and negative thresholds definitely adds skew or zero-crossing error to the signal. It can

thus be seen that low amplitude in itself adds zero-crossing distortion to the signal and, therefore, that adding 150 ns more results in an overly rigorous test.

50.3.8.2 Gap test. 1553B is much less clear when input and output characteristics get mixed into the same requirement. An example of this are the gap and tailoff tests. Intermessage gap (4.3.3.7) is an input requirement. The standard requires that a terminal must be able to respond to a message that is sent 4 us after the previous message. Tailoff (4.5.2.1 .1.4 or4.5.2.2.l.4) is an output characteristic. 1553B requires that, at the end of a transmission, the voltage on the bus be less than ±250 mV (±90 mV for direct-coupled stubs) during the period beginning 2.5 us after the transmission. The tailoff requirement was designed to prevent the end of a transmission from interfering with the reception of the next message sent with the minimum intermessage gap. With signals just above threshold and to the same terminal, this goal is not met.

The gap test is typically done by sending two messages in close succession with a 4-µs gap time. Figure 50-9 shows an example of a gap between two words on the input/output of a terminal for a transformer-coupled stub. The last half-bit of a transmission by the terminal is shown followed in 4 µs by the start of a command word from another terminal. The terminal transmission has a tailoff voltage of 0.25V, the maximum allowed by 1553B. The second message has an amplitude of 0.86 V_{p-p} the minimum allowed by 1553B. The receiver sees the first half-bit of the command word as a voltage level of 0.18V (0.86/2 – 0.25). The receiver would have to have a threshold voltage of 0.36 V_{p-p} to detect this half-bit properly. 1553B certainly does not require this; the requirement is 0.86 V_{pp} Typical receiver thresholds are about 0.7Vp-p Also, 1553B requires rejection of all signals less than 0.2 V_{p-p} If the receiver were to accept 0.36 V_{p-p} signals, the actual threshold would have to fall within a range of 0.16 V_{p-p} or 0.08V of tolerance for the positive and negative comparators. This would make manufacturing a definite challenge.

To determine the amplitude of the second message so the gap test can pass, assume 0.86 V_{p-p} (0.43V both positive and negative) for the receiver threshold. Add to these thresholds 0.25 V_p of offset (tailoff). This gives a minimum required voltage of 1.36 V_{p-p} for the second message.

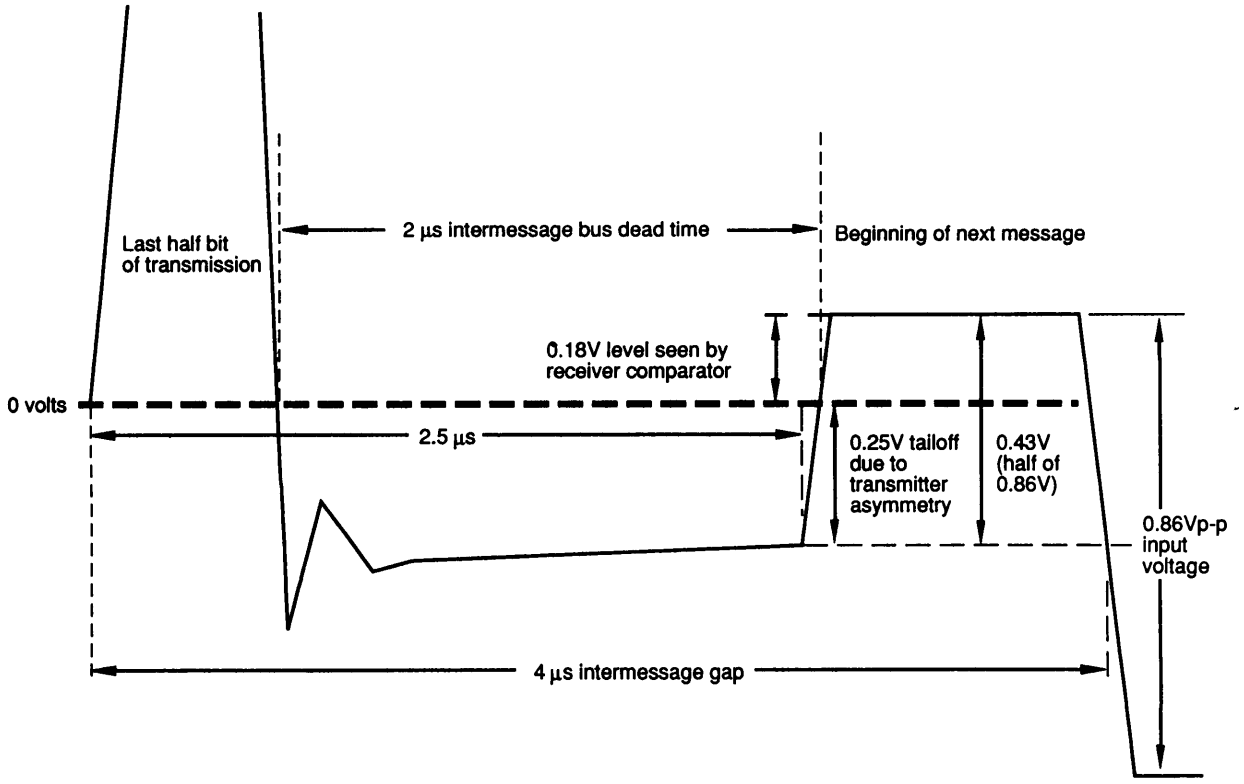


Figure 50-9. Minimum Intermessage Gap

Note that this problem arises because the first message of the pair was assumed to retransmitted by the same terminal as the input being looked at. Tailoff voltages from outputs of other transformer-coupled terminals are attenuated to 1/4 of their value by the bus network (see 50.3.7.1). If 62 mV were used instead of 250 mV in the above calculation, there would be no problem.

50.3.9 Analog example 1. Figure 50-10 shows an example terminal analog front end. For this example, a current-mode transceiver has been chosen. It has been designed to interface with a transformer-coupled stub. Please note that this is only an example; there is no reason that this terminal could not have been designed to interface with a direct-coupled stub. The only difference would have been the inclusion of the fault-isolation resistors and a different turns ratio in the isolation transformer. Note also that examples of complete terminals are presented later (see 50.5.8 and 50.8.6).

The transceiver has a current-mode transmitter and a receiver with a preset threshold. It includes none of the extra functions mentioned in 50.3.3.3 (e.g., over-temperature protection or an internal watchdog timer). Its interfaces with the rest of the terminal are TTL voltage levels. This type of transceiver is an industry standard; several vendors provide pin-compatible transceivers that could be used in this circuit.

While all of these transceivers are designed to meet 1553B, they are not identical. They have different thermal characteristics, encoder/decoder compatibility, and power supply requirements. (See 50.3.3 for a more complete discussion of these differences.) With respect to power supply voltages, note that transceivers with different power supply requirements might still be pin compatible. An example of this is that a transceiver that requires only +5V functions properly in a board designed for a transceiver that requires two or three power supplies. The pins on the board that are connected to + 15V or –15V are not connected internally in the single-supply transceiver. The designer would have to allow for the added +5V power supply loading, though. The

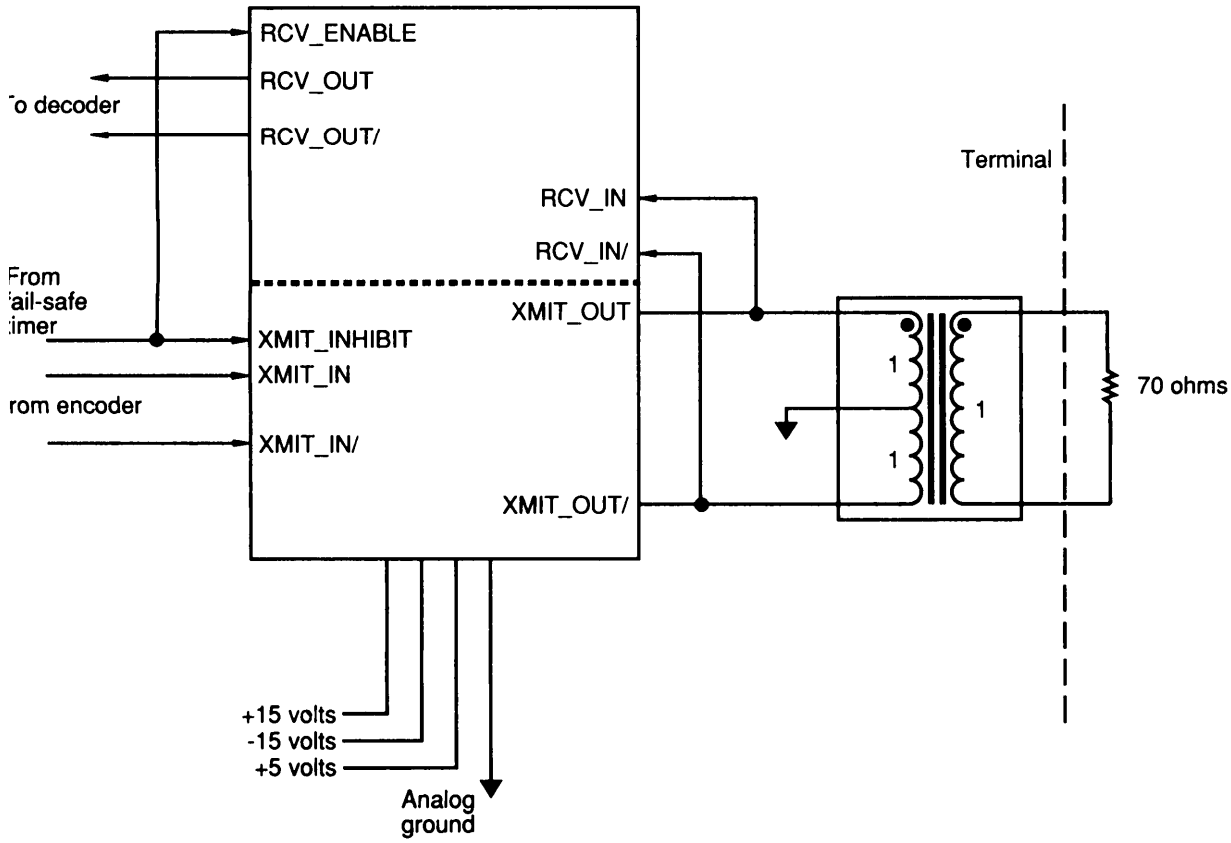


Figure 50-10. Example Terminal Front End Design Using a Current-Mode Transceiver

isolation transformer would also have to be changed, because a transceiver that requires only +5V typically requires an isolation transformer with a different turns ratio.

The transformer is also available commercially. Like the transceiver, it is an industry standard part. Transformers differ in turns ratio (for different transceivers) and can also differ in electrical performance. (See 50.3.4 for a more complete discussion.) Since this is a terminal for transformer-coupled stubs, there are no fault-isolation resistors. Remember that these are included with the stub coupler to the 1553 bus in this case.

The parameter values, signal names, and operational descriptions used in this discussion represent a typical design and therefore do not necessarily match any particular combination of parts. The designer should remember that the values for the parts he is using are likely to differ.

The following two sections discuss transmitter and receiver operation. When the transmitter is operating, the receiver is assumed to be quiescent and vice versa, which is typically (but not necessarily) true.

50.3.9.1 Transmitting. To initiate a transmission, the encoder first removes XMIT_lNHIBIT. This input allows the fail-safe timer to turn the transmitter off and thus limit the length of the transmission. The encoder then sends the data to be transmitted on XMIT_IN and XMIT_IN/. To output a positive pulse, the encoder sets XMIT_IN high and XMIT_IN/ low and vice versa for a negative pulse. The transmitter output is inhibited (i.e., OV) when these two inputs are in the same state. Either both inputs high or both low shutoff the transmission, but both high is recommended since TTL signals have more noise margin when high.

The output voltage of the transmitter is about 20 VP-Pinto a 70-ohm load. The rise and fall times, measured from 10% to 90% of the full-scale waveform, are about 150 ns. The transformer, designed for 1553B, has a primary (i.e., bus side) inductance of 5 mH and a shunt capacitance of 49 pF.

It is important that the transmitter drive the output high exactly the same amount of time and to the same amplitude as it drives it low. The terminal designer using this standard transceiver can do little about the asymmetry introduced by the transmitter itself, but the inputs (from the encoder) should be as symmetrical as possible. Tailoff results from energy remaining in the isolation transformer's core (inductance) at the end of a transmission. Remember that every bit (data or sync) in Manchester format is high for half the bit time and low for the other half. Each half-bit that is high stores energy in the core in one direction (of magnetic flux), and each half-bit that is low stores energy in the core the opposite direction. Therefore, if the high and low times are not symmetrical, or if the amplitudes are different, there will be some nonzero energy left at the end of the transmission, and tailoff will result.

50.3.9.2 Receiving. When RCV_ENABLE is true, the receiver looks at the stub voltages. All waveforms on the stub with high enough voltage and proper frequency (so they are not rejected by the receiver's threshold logic and input filter) are converted into TL level signals on RCV_OUT and RCV_OUT/. Note that RCV_ENABLE is connected in the example circuit to XMIT_INHIBIT. This connection always disables the receiver when the transmitter is enabled to transmit and vice versa.

When the receiver detects no signal on its input, it sets both RCV_OUT and RCV_OUT/ high. Note that some pin-compatible parts set both of those signals low in the absence of an input signal. It is important to choose a receiver with receive data outputs that have a quiescent state that matches the requirements of the decoder used.

The input voltage threshold of the receiver is about 0.7 V_{p-p} The receiver contains two comparators, one with its threshold set to +0.35V and the other to 4.35V. Input signals are first filtered, cutting out frequency components above about 1.5 MHz. The value 1.5 MHz was chosen because the frequency spectrum of an ensemble of 1553B messages is primarily concentrated at 1.5 MHz and below. if the cutoff were any lower, substantial signal energy would be removed. Thus, any signal whose frequency is 1 MHz or below and whose positive and negative amplitudes are greater than 0.35V will be detected. Note that, due to zero-crossing errors introduced by the rise and fall times of the input signal, the decoder will not necessarily decode a signal

correctly even though the receiver detects it. See 50.3.7.2 for more discussion. An example of a waveform decoding process is shown in figure 50-8.

The input impedance of the terminal is calculated as follows (all calculations are based on line-to-line measurements):

a. The output impedance of the transmitter in the inhibited state is 16K ohms capacitive or about 10 pF (assuming 1 MHz). The input impedance of the receiver is 16K ohms and is mainly resistive. The transceiver impedance is the parallel combination of these.

   At 75 kHz, the transceiver impedance is 16000 – jl200 ohms, where j indicates the reactive part (+j is inductive; –j is capacitive).

   At 1 MHz, the transceiver impedance is 7900 – j8000 ohms.

b. The turns ratio of the isolation transformer is 2:1, so the transceiver impedance appears at the terminal input reduced by a factor of 4 (impedance transforms as the square of the turns ratio).

c. The transformer impedance can be calculated from the primary (i.e., bus side) inductance of 5 mH and the shunt capacitance of 49pF.

   At 75 kHz, the transformer impedance is j2500 ohms.

   At 1 MHz, the transformer impedance is –j3600 ohms.

d. The wiring between the transformer and the terminal output and between the transceiver and the transformer will add some capacitance (the second of these is effectively multiplied by 4 by the isolation transformer). This value can vary greatly. Using a PC card typical value of 0.5 to 1.0 pF/in, a value of 10 pF is assumed. This gives an impedance of –jl 6000 ohms at 1 MHz and –j21 0000 ohms at 75 kHz.

e. Taken in parallel, these impedances yield a net input impedance as follows:

   At 75 kHz, the input impedance is 1100 +jl800 ohms, or a magnitude of 2200 ohms.

   At 1 MHz, the input impedance is 600 – jl400 ohms, or a magnitude of 1500 ohms.

This meets the input impedance requirement (4.5.2.1.2.3 of 15536) of 1000 ohms minimum (for a terminal with transformer-coupled stub).

50.3.9.3 Power and thermal consideration. The current-mode transmitter in this example uses only +15V as the source for the output driver. In other words, as transmit duty cycle changes, only the +15V supply current changes. The transmit duty cycle is defined as the percent of total time that the transmitter is transmitting.

As discussed in 50.3.3.1, there are two important issues relating to power consumption: power supply loading and maximum allowable transmit duty cycle for the given thermal conditions. To calculate either quantity, consult vendor specifications.

The power and thermal specifications for the transceiver in this example are shown in table 504.

The power consumption can be calculated at different transmit duty cycles by multiplying the supply voltages and their respective currents. The total power consumptions are given in table 50-11. Some of this power (most of it, actually) is dissipated internally, and some of it is dissipated by the load. Assuming an output voltage

Table 50-1. Transceiver Power and Thermal Specifications, Analog Example 1.

	+5V		+15V		-15V	
	Typ	Max	Typ	Max	Typ	Max
0% duty cycle (mA)	25	40	25	30	25	30
25% duty cycle (mA)	25	40	65	75	25	30
100% duty cycle (mA)	25	40	185	210	25	30

Thermal impedance, hottest device to case: 65°C/W
Thermal impedance, case to air: 30°C/W
Power dissipated by hottest device at 100% duty cycle (decreases linearly to 0 mW at 0% duty cycle): 400 mW (typ) 550 mW (max)

Table 50-11. Total Power and Consumption, Analog Example 1.

	Total power	Dissipated By load	Dissipated Internally
0% duty cycle (mW)	875	0	875
25% duty cycle (mW	1475	250	1225
100% duty cycle (mW)	3275	1000	2275

Note: Values in this table are rounded to 25 mW,

of 20 V_{P-P}, a load impedance of 78 ohms resistive (typical for the 1553B bus – the reactive part of the load impedance varies from one bus to another and is very difficult to calculate; for simply in this example, a resistive load is assumed), and arise and fall time of 150 ns (and thus an RMS voltage of 0.85 times the peak voltage), the power dissipated in the load is as given in table 5041. The power dissipated internally to the transceiver is thus the difference between the power drawn from the power supplies and the power output into the load (see table 5041).

To determine the maximum allowable transmit duty cycle, the designer must know the maximum allowable junction temperature and the maximum ambient temperature under which the unit is expected to operate. These are given by the system specification. For this example, we assume a maximum operating temperature of 45°C and a maximum allowable junction temperature of 105°C. The calculation looks like this:

$$T_j = P_{max}\theta_{jc}DC + T_c \quad (1)$$

where:

T_j = Junction temperature
P_{max} = Power in hottest device at 100% duty cycle
e_{jc} = Thermal impedance-hottest device to case
DC = Transmit duty cycle
T_c = Case temperature

$$T_c = (P_q + P_{xmit}DC - P_{load}DC)\theta_{ca} + T_a \quad (2)$$

where:

T_c = Case temperature
P_q = Quiescent (0% duty cycle) total power
P_{xmit} = Extra power drawn when transmitting at 100% duty cycle
DC = Transmit duty cycle
P_{load} = Power dissipated in load at 100% duty cycle
θ_{CA} = Thermal impedance _case to ambient
T_a = Ambient temperature

Inserting the values:

P_q = 0.875 W
P_{xmit} = 2.400 W
P_{load} = 1.000 w
θ_{ca} = 30 ‘c/w
T_a = 45‘c

into equation 2 gives:

$T_c = (0.875 + 2.400DC - 1.000DC)30 + 45$
$=71.25 + 42DC$

Inserting into equation 1 the values:

T_j = 105°C
P_{max} = 0.4 W
θ_{JC} = 65 °C/W

gives:

$105 = (0.4)\ (65)DC + T_c = 26DC + 71.25 + 42DC$

so DC = 0.50 and T_c = 92°C.

Thus, the maximum transmit duty cycle at which our example transceiver is allowed to operate is 50%. If operated at a higher duty cycle, the junction temperature of the hottest device in the transceiver will exceed 105°C, the maximum we assumed was permitted. If a higher transmit duty cycle is necessary, a heat sink could be provided for the transceiver to reduce θ_{ca} (the thermal impedance from case to ambient).

Figure 50-11 is a graph of the equations presented above. It shows the relationship between duty cycle and transceiver power and T_j–T_c. Note that when case temperature is 92°C and duty cycle is 50%, the junction temperature is 105°C.

50.3.10 Analog example 2. Figure 50-12 shows another example terminal analog front end. For this example, a voltage-mode transceiver has been chosen. It has been designed to interface with a direct-coupled stub. Please note that this is only an example; there is no reason that this terminal could not have been designed to interface with a transformer-coupled stub. The only difference would have been the deletion of the fault-isolation resistors and a different turns ratio in the isolation transformer.

The transceiver has a voltage-mode transmitter and a receiver with a preset threshold. It includes none of the extra functions mentioned in 50.3.3.3 (e.g., over-temperature protection or an internal watchdog timer).

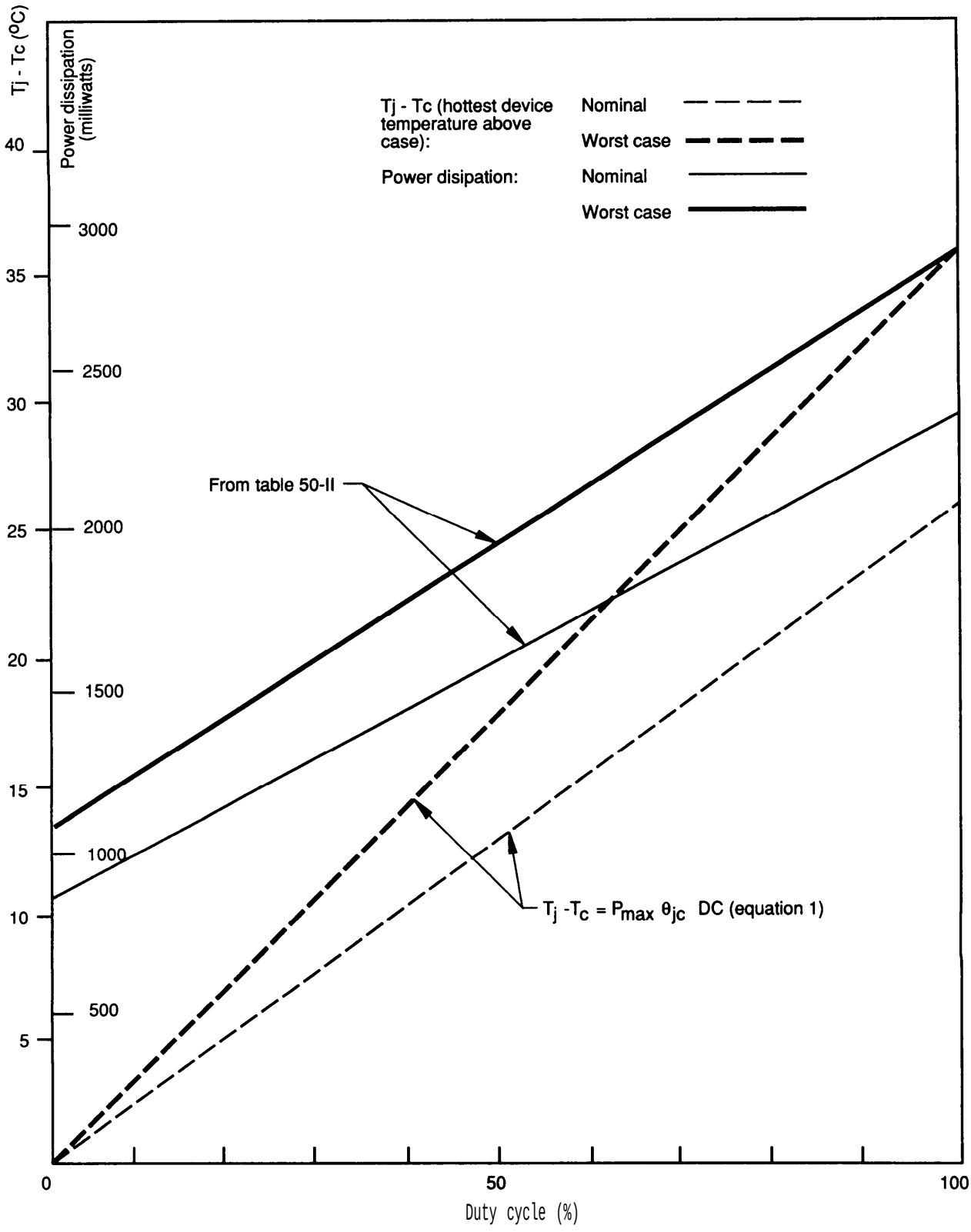


Figure 50-11. Transceiver Temperature and Power Vs. Duty Cycle

This type of transceivers Iess common than the current-mode type included in analog example 1 (see 50.3.9), but several vendors do provide pin-compatible transceivers that could be used in this circuit.

50.3.10.1 Transmitting. The encoder initiates a transmission in the same manner as in the previous example. There are, however, differences in the output characteristics. The voltage output onto the bus (which is the same as the stub because it is direct coupled) is nominally $7V_{p-p}$ The rise and fall times of this waveform are typically 220 ns. As in the previous example, it is important to ensure that the data inputs to the transmitter are balanced in time (positive to negative) to minimize the output offset.

50.3.10.2 Receiving. The receiver in this example functions in a manner similar to the receiver in the previous example. Due to the fact that it is direct coupled, though, the nominal receiver threshold is typically 1.0 V_{P-P} This particular transceiver has an option to select the receiver input voltage threshold but, as implemented in this example, the threshold is set to the default value.

The input impedance is calculated in the same manner as in the previous example. The transformer and transceiver present the same impedances. In this case, however, the transformer has a turns ratio of 1:1 instead of 2:1, so the transceiver impedance will not be reduced by a factor of 4, and the fault-isolation resistors of 110 ohms add directly to the input impedance.

The input impedance at 75 kHz is thus 500 + j2500 ohms for a magnitude of 2500 ohms. Input impedance at 1 MHz is 500–j2400 ohms for a magnitude of 2400 ohms. Both these values meet the required 2000 ohms minimum.

Table 50-111. Transceiver Power and Thermal Specifications, Analog Example 2

	+5V		+15V		-15V	
	Typ	Max	Typ	Max	Typ	Max
0% duty cycle (mA)	30	45	40	60	40	60
25% duty cycle (mA)	30	45	70	90	70	90
100% duty cycle (mA)	30	45	160	180	160	180

Thermal impedance, hottest device to case:	90%C/W
Thermal impedance, case to air:	20%C/W
Power dissipated by hottest device at 100% duty cycle (decreases linearly to 0 MW at 0% duty cycle):	400 mW (typ) 550 mW (max)

Table 50-IV. Total Power Consumption, Analog Example 2

	Total Power	Dissipated	
		By load	Internally
0% duty cycle (mW)	1350	0	1350
25% duty cycle (mW)	2250	240	2000
100% duty cycle (mW)	4950	950	4000

Note : Values are rounded to 50 mW

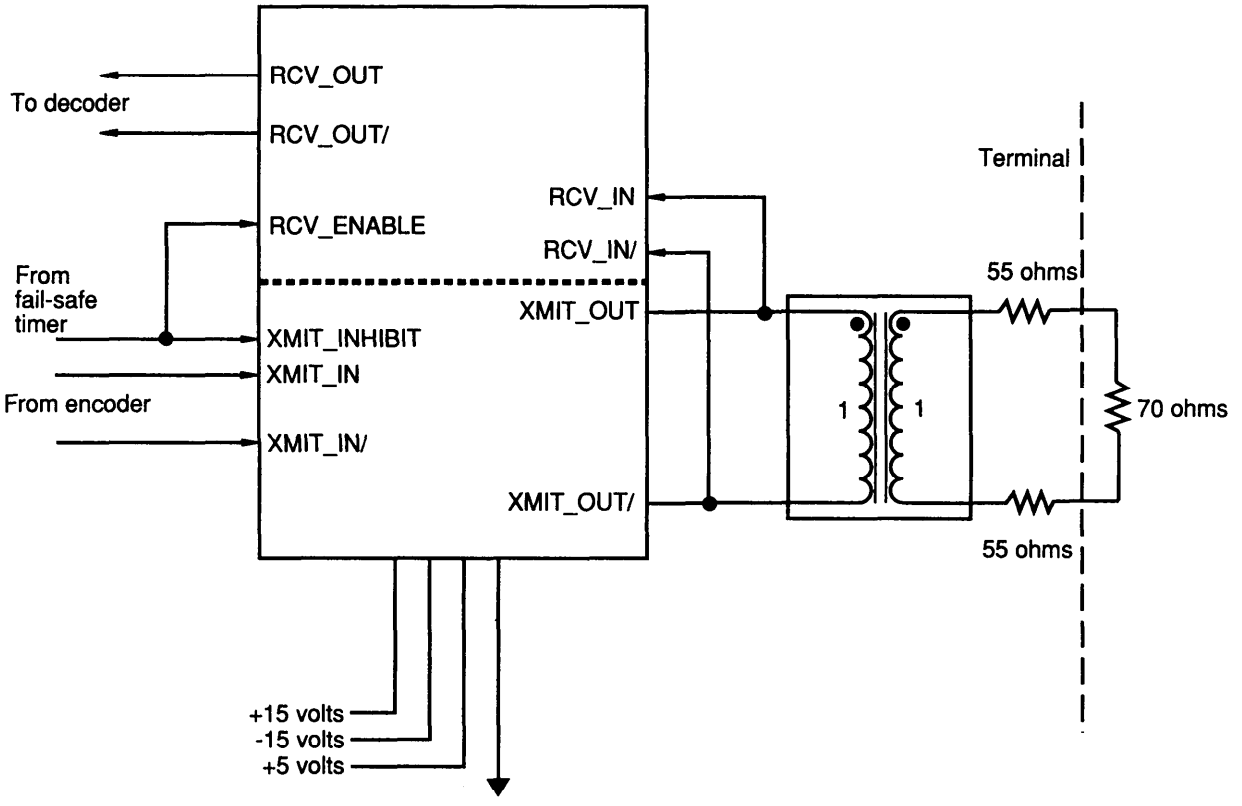


Figure 50-12. Example Terminal Front End Design Using a Voltage-Mode Transceiver

50.3.10.3 Power and thermal considerations. The voltage-mode transmitter in this example uses both high-level (±15V) power supplies as the source for the driver. The power consumption is significantly greater than that for a current-mode transmitter.

The power and thermal specifications for the transceiver in this example are shown in table 50411.

The power consumption at different transmit duty cycles, and the portions that are dissipated internally and by the load, are calculated similarly to the previous example. In this case, we assume an output voltage of 30 V_{P-P}, a load impedance of 145 ohms resistive (typical for the 1553B bus including fault-isolation resistors), and rise and fall times of 220 ns (and thus an RMS voltage of 0.78 * V_{PEAK}), the power dissipated in the load is as given in table 50-IV.

The maximum allowable transmit duty cycle is calculated in the same fashion as in the first example. Assuming the same constraints (T_a = 45°C, T_j = 105%C), the maximum allowed duty cycle is 37%. For operation at higher duty cycles, an increased cooling effort would be required (e.g., heat sinks, forced air, etc.).

50.4 DIGITAL SECTION.

50.4.1 Encoder/decoder The functions of an encoder/decoder are as follows (see figure 50-13):

Decode (receive).

a. Detect and decode the sync waveform to identify the word type (command/status or data).

b. Detect and decode each data bit, verifying that each is a valid Manchester-coded bit.

c. Verify that all words have the correct number of bits (i.e., sync plus 16 data bits plus parity).

d. Decode the parity bit and verify that parity is odd. This could possibly be done in the protocol control unit block (see figure 50-1 and paragraphs 50.5 and 50.6) but is typically done in the decoder.

e. Decode the terminal address field of a command word (i.e., the first five data bits). Compare it to the terminal address that has been defined for the terminal. Also compare it to 11111, the broadcast address. Further discussion of the terminal address is presented in the RT requirements section (50.5.1), even though this function is typically performed by the decoder part rather than the protocol control unit.

   NOTE: ABC must decode the terminal address field of returned status words to verify that the proper RT responded, but this function is not typically performed in the decoder.

   For RT-to-RT messages, it is desirable that the receiving RT decode the terminal address in the transmitting RT's command word and status word to validate the message. This also is typically not performed in the decoder.

The decoder outputs each word to the protocol control unit as it is received, along with information indicating that the word is valid, the type of sync (command, status, or data), and perhaps other information about the message, such as whether this word is a broadcast command word or a mode command word.

Encode (transmit).

a. Form the proper sync waveform for the word to be transmitted.

b. Encode each data bit into valid Manchester code.

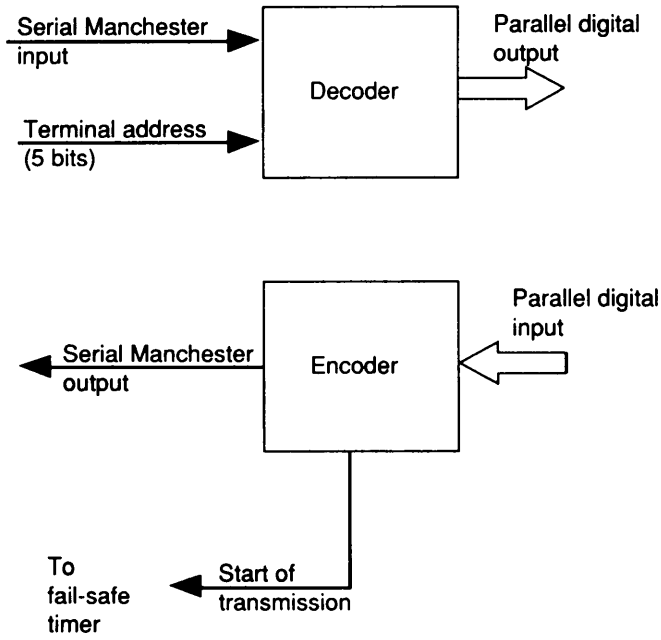


Figure 50-13. Encoder/Decoder Functions

c. Generate the proper (odd) parity bit and add it to the end of the word.

d. Send the word serially at the correct rate (1-MHz bit rate) to the transmitter.

The encoder is commanded by the protocol control unit to output each word in turn. The protocol control unit must indicate the type of sync with which to start the word (command, status, or data) and when to send it (immediately, or perhaps after the completion of sending the previous word).

The encoder/decoder function of the majority of terminals being designed today is normally performed by an off-the-shelf integrated circuit (IC) part. The decoding function is one of the most critical in the design of the terminal, and the requirements do not vary a great deal from one terminal to the next, making this a logical place for a standard part. The design of discrete encoder/decoders is not discussed in much detail in this section. Much of the information about the internal workings of these parts is proprietary to their manufacturers. Some of the general considerations in their design are discussed next.

50.4.1.1 Clock rate. The signal from the 1553B bus is asynchronous with any clock in the terminal because a Manchester code is, by its nature, self-clocking. That is, all Manchester-encoded bits have a zero-crossing in the middle, and it is to this zero-crossing time that the data is referenced. The clock signal that the terminal uses to decode the signal determines the resolution with which the incoming signal can be examined. If all 1553B signals had perfect timing, a sampling frequency of 2 MHz, which would guarantee one sample every half-bit time, would be adequate. However, 1553B requires that terminals operate properly for signals with zero-crossings displaced by up to 150 ns from their proper places. Different manufacturers use different sampling frequencies; 12 MHz and 16 MHz are the most common.

50.4.1.2 Zero-crossing susceptibility. The input to the decoder from the receiver is two signals, RCV_OUT and RCV_OUT/, that are nominally complements of each other. Actually, however, RCV_OUT is true when the bus signal is above the positive threshold, and RCV_OUT/ is true when the signal is below the negative threshold. As discussed in 50.3.7.2 and shown in figure 50-8, the transitions in RCV_OUT and RCV_OUT/ will occur a little before and after, respectively, the actual zero-crossing of the signal on the bus. To synchronize properly with the midbit zero-crossing of the sync field, the decoder must determine when this zero-crossing occurred from RCV_OUT and RCV_OUT/. The decoder usually attempts to choose a time halfway between the transitions of its inputs. Its mechanism of doing this is usually proprietary. There are decoders that use only one of the two receiver signals. Such a decoder will be quite susceptible to zero-crossing distortion on its input (i.e., a bus signal that has its zero-crossings displaced from their ideal positions). Among those decoders that do use both receiver signals, some are more successful than others at detecting the actual times of zero-crossings. About all that can be said here is that every terminal design must be evaluated as a whole and not as a receiver and decoder separately.

50.4.1.3 Noise. The effect of noise on the bus signal was discussed from an analog standpoint in 50.3.7.2. In short, good performance of the terminal in the presence of noise on the bus depends on input filtering and the proper setting of the input voltage thresholds. The decoder must be designed to function correctly in the presence of noise that gets through the analog section. Noise spikes that are not filtered out may appear as more than one zero-crossing in a bit time. The decoder should sample and process the signal in such a way as to tolerate perturbations of this sort without being so tolerant as to accept noise as valid data. Note that there can be certain noise perturbations that are not properly handled, but, for noise such as described in the 1553B noise test (4.5.2.1.2.4 and 4.5.2.2.2.4 of 1553B), there shall be no more than one word error in 107 words. This condition alone is responsible for most of the difficulty in decoder (and receiver) design.

Tests and analyses have determined that, to the probability of one in 10^7, random noise on the bus (with the characteristics defined for the noise test) can look like a sync waveform and two data bits. A properly designed decoder, therefore, does not indicate the presence of a word on the bus until it detects at least a sync waveform and two or three valid data bits.

The discussion of the 1553B noise test in 50.3.7.2 covered most of the considerations involved in running the test successfully. Much of this discussion covered the setup of the actual noise source and the insertion of the noise into the input of the terminal in the proper manner. Of all the portions of a terminal, the design of the receiver has the most important effect on the noise test results. The decoder is not unimportant, however. The choice of the part used for the decoder certainly affects the noise performance. Since off-the-shelf parts are normally used for both the receiver and the decoder, the only real way to know how a terminal performs is to test it.

50.4.1.4 Word errors.. A word in 1553B is delimited by the sync waveform at its beginning. The midbit zero-crossing of the sync waveform is the timing reference for decoding the entire word. After synchronizing its operation with this midbit zero-crossing, the decoder knows when each of the other bits is supposed to occur. Several word error conditions may be defined:

a. **Manchester** error–if, at anytime, the decoder detects a bit in which both halves are at the same state (i.e., with no midbit zero-crossing), this is a Manchester error.

b. **Bit count** error–if the word ends (i.e., either another sync waveform is seen or there is no signal) and there have been more or fewer than 20 bit times (i.e., sync, 16 data bits, and 1 parity bit), this is a bit count error.

c. **Parity** error–if, after the 17 data bits are received (i.e., the 16 data bits and the parity bit), the parity is not odd (i.e., the total number of ones in the 17 bits is not odd), this is a parity error.

The decoder may or may not inform the protocol control unit of the presence of an error. A command word with an error maybe completely ignored. The protocol control unit does need to know about an invalid data word, but this is commonly done by not indicating that it is valid.

50.4.1.5 Terminal address. Every terminal that is acting as an RT has a unique terminal address that can range from 00000 (binary) to 11110 (binary). Note that a unique terminal address of 11111 (binary) is not allowed because this address is reserved for broadcast commands. The terminal address is uniquely an RT function, so discussion is deferred until the RT section (50.5.1), even though the terminal address decoding function is usually done in the encoder/decoder.

50.4.2 Fail-safe timer. MlL-STD-l553B requires (4.4.1.3) that every RT or BC contain a hardware timer to prevent any transmission on the bus from exceeding 800 µs. Because no valid transmission is longer than 660 µs, only a failure in the terminal could result in a transmission of 800 µs or longer. The fail-safe timer is required to prevent such a failure from causing a continuous transmission on the bus and thus rendering it (the bus) unusable for other transmissions.

Typically, the fail-safe timer output is connected to the XMIT_INHIBIT input of the transmitter. The encoder or protocol control unit would start the timer at the beginning of every transmission by the terminal, setting the timer output false (i.e., the transmitter is allowed to transmit). When the timer times out, XMIT_lNHIBIT is set true, turning off the transmitter. Note that, in a nonfailed terminal, the transmission will always have been completed prior to the timer timing out, so this timeout will have no effect.

The difference between the maximum transmission time that must be allowed (660 µs) and the required fail-safe timeout (800 µs) was made wide enough that analog timer circuits might be used to implement this function. For a temperature range of –55°Cto+125°C, however, the allowed timeout range of 660 to 800 µs may not be wide enough for a proper worst case design without using an expensive circuit with a comparator, a precision capacitor, and perhaps a voltage reference. Also, common one-shot timer circuits are notorious for not functioning as their specifications would indicate.

A digital implementation of the fail-safe timer is also possible. All terminals include a clock for their other functions, and a few stages of clock division will give a clock of an appropriate frequency. A frequency on the

order of 16 kHz (which is a period of 62.5 µs) has sufficient resolution to produce a timeout time in the required range with a 4-bit counter.

The digital implementation has a few minor disadvantages. It probably requires more parts, but with modern programmable or custom circuit logic design, this is not too significant. There is the possibility in any clocked circuit that the clock could stop and thus preclude the operation of the circuit. Unless the fail-safe timer clock is the only clock that fails, the rest of the terminal would also be nonoperational, and it would be unlikely that it would continue to transmit anything. Also, the reliability y of the digital counter circuit would probably be better than a one-shot timer.

In a dual-redundant design, it is possible to use one fail-safe timer for both channels, since only one channel is allowed to be active (i.e., transmitting) at a time. Many terminals are in fact designed in this manner. With only one fail-safe timer, it could fail and shut down both redundant channels. For this reason, it is recommended that there be a separate fail-safe timer for each of the redundant channels. The designer should evaluate his system requirements and circuit failure probabilities to determine if separate fail-safe timers are necessary in his specific design.

50.4.3 Redundancy. The majority of 1553B systems are dual redundant. Notices 1 and 2 require at least dual-redundant operation for Air Force avionics applications (more than dual redundancy is permitted). The requirements for operation in this mode are stated in the standard. However, there are applications where nonredundant terminals are satisfactory, and there are others where more than dual redundancy is required. The standard is designed to accommodate redundancy, so there is usually no major impact on the design of the terminal other than the inclusion of the proper number of transmitters, receivers, and encoder/decoders.

The last sentence in the previous paragraph made an assumption that only the analog portion, the encoder/decoder, and address decoding functions would be duplicated for each redundant channel. This is not necessarily the case, but most of the available parts are designed for this level of redundancy. Figure 50-14 gives three examples of dual-redundant terminals with different portions made redundant. Any of these approaches to redundancy are acceptable. If system requirements dictate a higher level of confidence, it is possible to have terminals that are totally redundant. That is, there could be two (or more) entirely separate terminals to implement the redundant sections of what is functionally a single terminal. The coordination of the two terminals in the manner required by 1553B would add substantial complication. If this type of design is contemplated, careful thought should be given to the actual improvement of reliability that would result. Typically, the complications of this approach outweigh the benefits.

1553B requires that if a data bus system is to be dual redundant, it shall operate in a dual standby redundant mode (see 4.6.3 of 1553B). This requires that only one bus can be active at any given time. It also requires that a terminal (RT or bus monitor) should be able to accept an overriding command on the other bus (i.e., the bus that is not currently in use) at anytime. There is no requirement in 1553B that a BC should be able to issue such an overriding command, however, and BCs frequently do not implement this capability. Implementation of the superseding valid command requirement requires that an RT or bus monitor must be constantly decoding traffic on both buses. Seethe RT section (50.5.4) for further discussion.

Of the available 1553 ICs, most are designed to implement dual-redundant terminals and, some, quadruple-redundant terminals. Therefore, a nonredundant terminal built from these parts typically requires that several features or pins be Ieft disconnected. This is usually well defined in the documentation of the parts and should cause no problems. A triple-or quadruple-redundant terminal should also be simple to implement. The user must be sure that the parts chosen do support his system requirements, but most manufacturers have versions of their parts that support more than dual redundancy.

50.4.4 Notice 1 and Notice 2 effects. The effects of the two 1553B notices, and how they differ from 15536, are discussed in section 90. Those differences that affect terminal design are also discussed here. More details about those requirements that are specific to one type of terminal (RT, BC, or bus monitor) are given in the section on that type of terminal.

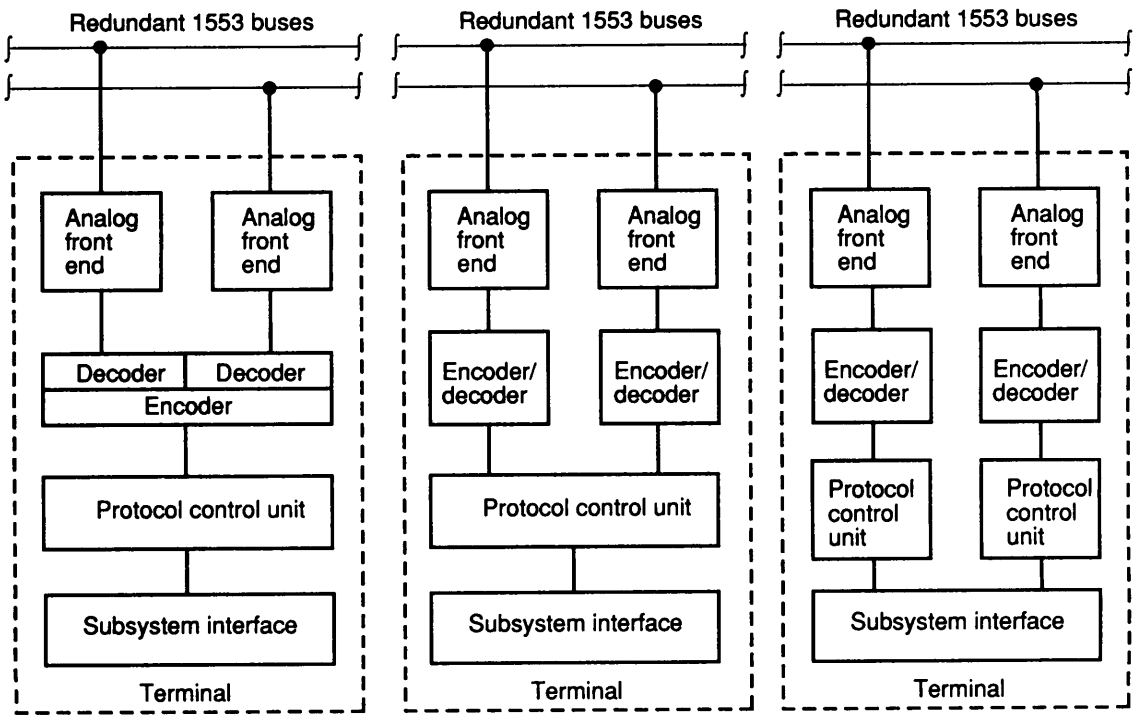


Figure 50-14. TypesofTerminal Redundancy

50.4.4.1 Notice 1. Notice applies to all Air Force aircraft internal avionics applications (per section 20 of Notice 1). The requirements therein that are applicable to terminal design areas follows:

a. Certain mode commands (dynamic bus control, inhibit terminal flag bit, override inhibit terminal flag bit, selected transmitter shutdown, and override selected transmitter shutdown) may not be issued by BCs, although the capability to do so is not prohibited. RTs, however, may still implement them.

The Air Force believes that switching from the current BC to a backup BC using the dynamic bus control mode command is too risky, so it is prohibited.

b. Broadcast commands may never be issued by BCs, although the capability to do so is not prohibited. RTs may implement the capability to accept data from a broadcast command, or they may ignore them. In either case, the terminal address of 11111 (binary) is still reserved for broadcast and may not be used for any other purpose.

The problem with broadcast commands is that there is no built-in mechanism to verify that the data were transferred properly. The Air Force feels that they violate the "command-response" nature of 1553, in which every command is concluded with a corresponding response unless an error occurred.

c. BCs must be capable of issuing mode commands with either 00000 or 11111 (binary) in the subaddress mode field. RTs, however, are only required to be able to recognize 00000 (although they are encouraged to be able to recognize 11111 also). For RTs, this is a loosening of requirements, since paragraph 4.3.3.5.1.7 of 1553B requires that "a subaddress/mode field of 00000 or 11111 shall" indicate a mode command. This change results from 1553(USAF), the very first version of 1553, which only required that 00000 be recognized as a mode command indicator. With this change, 1553(USAF) RTs comply with the standard in this respect.

Some RTs can only detect a subaddress/mode field of 00000 as the mode command indicator, and some can only detect 11111. ABC, in order to function with RTs that are designed in either of these manners, must be capable of issuing mode commands that the RT recognizes.

d. If a BC implements any mode commands, it must implement all the mode commands (except those that are prohibited above). An RT may implement only as many mode commands as its design requires. RTs are still permitted to not implement mode commands and, therefore, are permitted to not recognize a subaddress/mode field of 00000 or 11111 as defining a mode command.

e. All systems (for Air Force avionics use) must use the dual standby redundant design defined in the standard. More than dual-redundant operation is permitted but, if used, must be structured in pairs of dual standby redundant buses.

50.4.4.2 Notice 2. Notice 2 applies to all dual standby redundant applications for the Army, Navy, and Air Force (per section 30.2 of Notice 2). Notice 2 replaces all the sections that were changed in Notice 1, and most of the requirements of Notice 1 are also contained in Notice 2. The requirements in Notice 2 that are applicable to terminal design are as follows:

a. All Air Force internal aircraft avionics applications are required to be dual standby redundant (and hence the requirements of Notice 2 apply to all Air Force applications), unless higher levels of redundancy are deemed necessary, in which case they are permitted. There are no specific requirements, as in Notice 1, for more than dual redundancy.

b. RTs are required to be assignable any terminal address from 00000 to 11110 (binary), and changing the address must not require the modification of any part of the RT or the opening of any unit containing the RT. Also, no single point failure may cause an RT to assign itself a false address. This requirement, which is discussed further in the RT section (see 50.5.1), is typically accomplished by the addition of a parity bit on the terminal address inputs and a parity test circuit within the RT.

c. BCs must be capable of issuing mode commands with both 00000 and 11111 (binary) in the subaddress/mode field. RTs are required to be able to recognize both 00000 and 11111. There is also the requirement that 00000 and 11111 cannot convey different information, i.e., they must be treated totally equivalently by both BCs and RTs.

d. BCs are required to implement ail mode commands, although the dynamic bus control mode command may never be issued in an Air Force application. RTs are required to implement at least four mode commands (transmit status word, transmitter shutdown, override transmitter shutdown, and reset remote terminal). Note that this requires all RTs to recognize mode commands (by 00000 or 11111 in the subaddress/mode field).

e. There are requirements defined for response to reset remote terminal and initiate self test mode commands. Previously, these mode commands could be used in any manner that the system designer desired. These requirements are discussed in the RT section (50.5.7.2).

f. RT use of several of the bits in the status word is further defined. None of the definitions of the bits are changed, but certain of the bits are required in certain cases. In particular, the existence of busy conditions (and thus the use of the busy bit) is discouraged; if used, it is restricted. This also is discussed in the RT section (50.5.7.2).

g. Broadcast commands are not completely prohibited; broadcast mode commands are permitted. RTs are still permitted to implement the broadcast option. However, an RT must be capable of distinguishing between a broadcast and non-broadcast message to the same subaddress. The broadcast terminal address of 11111 (binary) is still reserved for broadcast and may not be used for any other purpose.

h. RTs are required to implement a data wrap-around function. The subaddress 1111 0 (binary) is suggested for this function, but it is not required.

i. BCs must be capable of issuing all defined message formats, including broadcast commands. Previously, these message formats were defined, but any given system could use only those that the system desired. RTs must implement all nonbroadcast message formats except mode command with data word. An RT is not allowed to distinguish between data associated with an RT-to-RT command and data associated with an RT-to-BC or BC-to-RT command.

j. The receiving RT in an RT-to-RT message transfer is required to check the response time (and the proper response) of the transmitting RT. If the first data word in the response occurs later than 60 µs after the (receive) command to the receiving RT, the message is invalid. It is also recommended (but not required) that the receiving RT verify the proper occurrence of the transmit command and the transmitting RT's status word and to treat the message as invalid if the transmit command and status word are not proper (e.g., if the terminal address fields do not match).

k. In Navy applications, all terminals are required to have both direct- and transformer-coupled stub connections externally available (although only one or the other could be used at one time). For Army and Air Force applications, all terminals must have (and use) transformer-coupled stubs, but may also have direct-coupled stub connections if desired.

l. All terminals are required to limit the amount of spurious output they produce when power is applied or removed. This is discussed in paragraph 50.3.7.3.

50.5 REMOTE TERMINAL REQUIREMENTS. A remote terminal (RT) is the most common type of terminal. Any 1553B bus system contains only one bus controller (BC) (at a time) but up to 31 RTs. Also, expendable stores (devices carried by an aircraft and normally used up during a mission, like bombs or missiles) typically contain only RTs; depending on the type of store, there maybe thousands of RTs manufactured for every BC. Because of this, there has been more effort put into the production of IC parts to implement RTs in an inexpensive and space-efficient manner.

The most important design characteristic of an RT is that it may not initiate any message traffic; it is totally controlled by messages it receives from the bus (and which were issued by the BC). Various schemes have been used by RTs to indicate to the BC that the RT would like to transfer data. The service request bit in the status word is provided for this application. All these schemes depend on the fact that the BC must poll (communicate with, in some manner) each RT on a regular basis.

50.5.1 Terminal address. Every RT must have one (and only one) assigned terminal address, except that an RT that implements the broadcast option also recognizes commands with 11111 in the terminal address field. There are 31 possible unique terminal addresses, 00000 to 1111 0 (binary), so 31 possible RTs can be attached to a bus. Exactly how a terminal address is to be assigned to an RT is not specified by 1553B. Available IC parts typically have five or six (see b. below) discrete inputs for the setting of their terminal addresses. In use, these pins are tied high or low as appropriate for the terminal address desired. Other RTs do not contain these input pins but rather an internal register that is loaded under software control (typically at power-on) with the desired terminal address.

Some existing RTsare hard-wired internally to a patticular terminal address. This approach creates problems with system reconfiguration or with the use of an RT in another system at a later date. Notice 2 adds requirements to reduce these problems. It is recommended that all RTs be designed to meet the requirements of Notice 2, even if this is not a specification requirement. These added requirements are as follows:

a. The terminal address is required to be established through an external connector that is part of the system wiring. No physical modification or manipulation of the unit may be required to change the terminal

address. Therefore, if an LRU is moved from one location in a system to another, the terminal address assignment of the RT automatically changes with the location. Also, the same RT (LRU) can be used in more than one system and have a different terminal address in each.

b. No single-point failure may cause the RT to validate a false terminal address (i.e., to think its terminal address is other than the one intended), and an RT may not respond to any commands if it has determined that its terminal address assignment is invalid. No particular method of validation is specified. The common method of validating the terminal address assignment, however, is a parity bit for the terminal address, making the terminal address effectively six bits rather than five.

Thus, an error (e.g., a broken wire) in any one of the six terminal address inputs causes a parity error, and the RT knows that its terminal address input is invalid. In this case, the RT will not respond to any commands. In particular, the error will not cause the RT's terminal address to be set incorrectly, and the RT will not respond to commands addressed to another terminal.

Because there is never a response to a broadcast message, the requirement above that an RT "not respond" if its terminal address assignment is invalid says nothing about its action in the event of a broadcast message. An RT is not prohibited from receiving and acting on a broadcast message if its terminal address assignment is not valid. In fact, many decoders will ignore the terminal address entirely in the presence of a broadcast command.

c. It is permissible for the RT to read and validate its externally set terminal address at power-up and then ignore the terminal address inputs. It is also permissible for the RT to read and validate the terminal address for every command. IC parts that implement both types of reading of the terminal address are available. Both approaches have their advantages. A terminal that only validates its address at power-up will be unaffected by failures in the terminal address wiring that happen later. However, problems that perturb the terminal address wiring could perhaps perturb other things too, and it would be desirable to declare an error. Also, if the terminal address is read only once and stored in a register and the register should become perturbed, the RT could start responding to commands with the wrong terminal address. The decision on when the terminal address is read must be made by the system and RT designers.

50.5.2 Protocol control unit requirements.

50.5.2.1 Response to commands. An RT must be able to detect (at all times and, for a dual-redundant system, on both 1553 buses) the presence of a command word that is valid for the RT. Upon detection of this command, it must be able to start the required response at a time between 4 and 12 μs after the command (or any data words with the command). Note that this time is measured from the midbit zero-crossing of the parity bit of the last word in the BC's transmission to the midbit zero-crossing of the sync waveform of the first word of the response (time T in Figure 8 of MlL-STD-l5539). This corresponds to an actual 'dead time" between words of 2 to 10 μs, because the last half of the parity bit is 0.5 μs long and the first half of the sync waveform is 1.5 μs long. In 1553A, interword times were measured as dead time, so these times measured in 1553A terms are 2 μs shorter than those specified in 15539 terms.

An RT may not accept any command which is not valid. An RT has the option not to accept a command which is not legal. Valid and legal commands are defined as follows:

a. Valid command-A command to a given RT is valid if (see 4.4.3.3 of 15539):

(1) The word begins with a valid command sync waveform.

(2) There are 16 data bits, all of which are valid Manchester.

(3) There is a parity bit that indicates odd parity.

(4) The terminal address in the command matches the terminal address of the RT (or 11111 if the RT implements the broadcast command option).

b. Legal command-A command to a given RT is legal if it is valid and if it is included in a defined set of commands for the RT (see 4.4.3.4 of 1553B). For example, a particular RT could define as legal only the two commands: transmit SA=OO100 WC=OOOO1 and receive S A=OO101 WC=11111 (in this notation, SA is the subaddress/mode field of the command word and WC is the word count field, both in binary). It is not required that an RT implement illegal command detection, in which case all valid commands are legal and must be responded to, in form, per the requirements in 1553B. In fact, most RTs do not check for illegal commands. This matter is discussed further in paragraph 50.5.5.

In general, most of the messages that an RT sees on the bus are meant for another RT. A word is not a valid command if it does not start with a command sync. A word with command sync is not a valid command (for this RT) if it does not contain the terminal address of the RT. It therefore follows that the RT can usually stop paying attention to a word after the sync waveform and (perhaps) one or more bits of the terminal address (the first five bits of the word). When the tests of terminal address validity have failed, further validation of the word is not required.

A word that has not been detected as invalid after the first five bits (i.e., it has command sync and the first five bits are valid Manchester and match the terminal address of the RT) must be read in its entirety. If it is valid (the rest of the bits are valid Manchester and the parity is odd), the RT must take the appropriate action. The response (if required) must start within the required 4-12 μs. To be able to respond quickly enough, it is desirable that the decoder do this checking, bit by bit, as the word is being received.

A further complication is the requirement in 15536 that there be no contiguous words following the command word (for a transmit command) or the specified number of data words (for a receive command) transmitted by the BC. Due to noise considerations (see 50.4.1.2) most decoders cannot detect the presence of an incoming word until two or three bits past the sync waveform. The RT is required to validate the command by verifying that there are no following words (for a transmit command; for a receive command, this requirement applies after the data words). For a decoder that operates in the above manner, therefore, the response to a command cannot start until 5 to 6 μs dead time (which is 7 to 8 μs when measured from zero-crossing to zero-crossing) after the end of the command. Add to this the time required for the RT to actually start the response, and the response time typically becomes closer to the 12 μs maximum than the 4 μs minimum.

Note that the response time required by 1553A was much shorter (2 to 5 μs dead time, equivalent to 4 to 7 μs zero-crossing to zero-crossing). Mainly because of the issue mentioned in the previous paragraph, most RTs designed for 1553B do not meet the 1553A response time requirement.

50.5.2.2 Status word. An RT responds to all valid commands addressed to it (except for broadcast commands) with, as a minimum, its status word. The bits in the status word are defined in 15536. Some of the bits might not be used (i.e., always set to 0) in a given RT, but any bit that is used is required to be used in the manner defined in 1553B. The reserved bits must not be used at all (i.e., they are required to be set to 0). The status register is included in most of the available IC protocol control unit parts, and most of the bits that are used (message error, broadcast command received, terminal flag) are set by the part without any additional circuitry.

A distinction must be made between the status register in the RT and the status word transmitted on the bus. In most (but not all) cases, the status register is required to be reset immediately after the receipt of a valid command, before the status word for that message is transmitted. The status register is then set to represent the status of the RT at that time and the status word is transmitted. An exception is that the status word transmitted with either a transmit status or transmit last command mode command must represent the state

of the status register for the previous valid command. Thus, the status register must not be reset for a transmit status or transmit last command mode command.

It should be noted that some off-the-shelf components are channel oriented. For a dual redundant RT, for example, some of the status word bits would reflect the condition of only one of the busses. Some of the status register inputs are supplied by the user (e.g. terminal address, subsystem flag bit, busy bit, service request bit, and dynamic bus control acceptance bit). In this type of part, though, the other bits are channel oriented and are not controllable by the user. These include the message error bit, broadcast command received bit, and terminal flag bit. While not meeting the full intent of 1553B, wherein the status word should reflect the state of the entire RT, these components have found applications in RT designs and the systems designer needs to be aware of their existence.

A summary of the status word bits (message error, instrumentation, service request, busy, subsystem flag, broadcast command received, and dynamic bus control acceptance) and their uses follow.

a. **Message error bit.** All RTs must implement the message error bit. This bit must be set to 1 for several error conditions that are defined in 1553B. It is strongly recommended that this bit not be set for any other reason. Most of these conditions also require that the transmission of the status word be suppressed. When there is no response (i.e., no status word is returned to the BC), the BC may determine if the message error bit was set by sending the RT a transmit status or transmit last command mode command. For an RT that does not implement either of these mode commands, there is no way for the BC to determine, after a no-response to a command, the value of the status register bits in the offending RT. Note that Notice 2 requires the implementation of the transmit status word mode command.

   Implementation of the message error bit is included internally to most available IC parts, and no external circuitry is needed. However, many parts do include the option of setting the message error bit externally. This would allow, for example, the addition of circuitry to set the message error bit upon the detection of an illegal command. See 50.5.5 for more discussion of illegal commands.

b. **Instrumentation bit.** The purpose of the instrumentation bit is to enable the differentiation of status words and command words, which are otherwise differentiated only by their position in a message. This bit in the status word is required by 1553B to always be set to 0. The equivalent bit position in a command word is the first bit of the subaddress. If all command words were to have 1 in this bit position (thus eliminating 15 of the available subaddresses and the use of 00000 as a mode command indicator), it would always be possible to identify status words asdistinct from command words. This feature is seldom used because of the reduction of allowable subaddresses.

c. **Service request bit.** The purpose of this bit is to inform the bus controller that the RT wants the BC to service it in some manner. In some applications (but not required by 1553), the BC would be required to send the RT a transmit vector word mode command when it (the BC) sees a status word with the service request bit set. The RT's vector word then defines the type of service that is desired. In other applications, the BC needs only to see the service request bit to start a predefine event or sequence of events; no additional information is needed.

   Implementation of the service request bit is included internally to most available IC parts, but the signal indicating that service is required must be applied externally (i.e., from the subsystem).

d. **Busy bit.** A busy RT is one that is functional but cannot transfer data to or from the subsystem on command from the bus controller. An RT that is busy should set the busy bit in its status word responses on the bus. In response to a transmit command, a busy terminal has no words to transmit, so only the status word is transmitted. In the case of a transmit mode command (transmit vector word, transmit last command, or transmit BIT word), the data might be available in the terminal, but it is still prohibited to send the data word if the busy bit in the status word is set.

It is recommended that a terminal be designed so that it cannot ever become busy. Notice 2 states this explicitly, but it is still required that, if an RT is busy, the busy bit must be set. This should keep the BC from assuming that data were transferred to the subsystem when they in fact were not.

e. **Subsystem flag bit.** This bit indicates that there is some fault condition in the subsystem. It is obvious, therefore, that the input for this bit cannot come from anywhere in the RT but must come from the subsystem. It is also obvious that 1553 can say nothing further about the nature of the fault. It is the responsibility of the system designer to specify a message or messages for the subsystem to inform the bus controller of the nature of the fault. This function is useful when the subsystem has failed but the terminal is OK (e.g., if the subsystem software has died).

f. **Terminal flag bit.** This bit indicates that there is some fault condition in the RT. Remember, the RT is only that portion of the LRU necessary to communicate with the 1553 bus. Typically (although not specifically required by 1553B), this bit is set upon a failure in built-in test (BIT), which might have been requested by an initiate self test mode command. The BIT register, which is transmitted to the bus controller upon the receipt of a transmit BIT word mode command, might be used to contain information about the fault. Some of the available IC parts use this bit for particular purposes and do not allow the terminal designer to control it. Others allow the designer to specify the fault conditions that can set it. The designer must ensure that, if there is a specification requirement for the use of this bit, parts are selected to meet these system requirements.

g. **Broadcast command received bit.** This bit is set by an RT that implements broadcast commands any time that a valid broadcast command has been received. Because there is no response to a broadcast command, the setting of this bit allows the bus controller to subsequently check that the command was received properly. It can do this by sending the RT a transmit status word or transmit last command mode command. Implementation of the broadcast command received bit is included internally to most available IC parts, and no external circuitry is needed.

h. **Dynamic bus control acceptance bit.** This bit is used only by an RT that can also become a BC when commanded by a dynamic bus control mode command. Notice 1 and Notice 2 (for Air Force applications only) prohibit the issuance of the dynamic bus control mode command by the bus controller. Therefore, RTs in Air Force applications that are required to meet Notice 1 or 2 need not implement this bit (but implementation of it is not prohibited). If not implemented, it must always be set to 0. Notice 2 does require the implementation of this bit in any RT that implements dynamic bus control. Implementation of the dynamic bus control acceptance bit is included internally to most available IC parts, but there must be an external input indicating that the subsystem (and a BC) has agreed to take over the task of controlling the bus.

50.5.2.3 Mode commands. An RT that implements mode commands is requijred to know that a subaddress/mode field in a command word equal to 00000 or 11111 (binary) defines a mode command and that, in this case, the word count field is to be treated as the mode code rather than the number of words. RTs that are not required to meet Notice 2 are not required to implement any mode commands, but they should still recognize that these subaddresses are special. Such an RT may treat mode commands as illegal and respond with only a status word in which the message error bit is set. Otherwise, the RT should respond in form (with at most one data word), but the commanded functionned not be performed and the data word need not contain valid information. Undefined mode commands may be handled in several ways; see paragraph 5.2.1 .1.1 of the RT Validation Test Plan (section 100 of this handbook). BCs are required to use subaddress/mode fields set to 00000 and 11111 only for mode commands; the bus controller is responsible for not sending a mode command to an RT that does not implement mode commands. Note that Notice 2 requires RTs to implement mode command detection.

RTs that implement mode commands are not required to implement all mode commands (Notice 2 requires four defined mode commands). If an RT is sent a mode command that it does not implement, 1553B does not specify what it should do. It is recommended (and most RTs follow this recommendation) that nonimplemented mode commands should be responded to in form (i.e., with a response whose format is correct, even though the data associated with it is not valid or the requested action does not take place). A nonimplemented mode command is an illegal command, and it therefore is permitted that an RT respond to it with only a status word in which the message error bit is set. Most decoder ICs available today do not include the detection of illegal commands, so to make an RT respond in this manner would involve extra circuitry. There are several newer decoders, however, that do include this feature. When using one of these, it is recommended that any nonimplemented mode commands be treated as illegal.

There are 15 mode commands defined in 1553B. Each of the 15 maybe used or not, but, if used, it must be used for the purpose and in the manner defined in 1553B. The others are reserved or undefined and may not be used at all. Nine of the used mode commands have no associated data word, three must be sent with a data word, and the other three cause the transmission of a data word. Of these last three, only one (transmit vector word) could involve data from the subsystem; all the other defined mode commands involve data and actions only within the RT (i.e., the terminal hardware as opposed to the subsystem).

For a given RT, some mode commands are not applicable and hence cannot be implemented. RT requirements to implement mode commands are discussed next.

a. **Transmitter shutdown and override transmitter shutdown.** These mode commands (which are required by Notice 2) are used in a dual-redundant RT to cause the transmitter on the other channel to be shutdown. The status word must be sent in response to the command, and then the other channel's transmitter must be shutdown. Nothing is stated in 1553B about the receiver. it is therefore permitted, but not recommended, that the receiver continue to receive data and the RT continue to pass these data to the subsystem but not to respond with a status word or any data words on the 1553 bus. The reason that it is not recommended is that it results in the transfer of data to the subsystem with no confirmation to the bus controller (i.e., no response). The BC should be designed so it does not talk to an RT on a bus that it (the BC) has previously shutdown, however, so this is probably not a major concern.

   A nonredundant RT cannot implement transmitter shutdown or override transmitter shutdown (or the selected versions either) because they only apply to the not-in-use channel, and a non redundant RT never has a channel not in use. In this case, 1553B does prohibit use of these mode commands.

b. **Selected transmitter shutdown and override selected transmitter shutdown.** A dual-redundant (or nonredundant) RT does not need to implement selected transmitter shutdown or override selected transmitter shutdown, because these are designed for systems with at least three redundant channels. Their use on dual-redundant systems is not prohibited by 1553B, but the transmitter shutdown and override transmitter shutdown mode commands are provided for this case.

   Both the selected transmitter shutdown and override selected transmitter shutdown mode commands must be accompanied by a data word that specifies the channel to be shut down. Because 1553B does not specify the manner in which this data word is to be coded, this information must be included in the system specification. The status word must be sent in response to the command, and then the transmitter for the specified channel must be shutdown. A command to shut down the transmitter on the channel currently in use (i.e., on which this mode command was received) must be ignored. Nothing is stated in 1553B about the receiver. it is therefore permitted, but not recommended, that the receiver continue to receive data and the RT continue to pass this data to the subsystem but not to respond with a status word or any data words on the 1553 bus. The reason that it is not recommended is that it results in the transfer of data to the subsystem with no confirmation to the bus controller (i.e., no response). The BC should be designed so it does not talk to an RT on a bus that it (the BC) has previously shut down, however, so this is probably not a major concern.

c. **Dynamic bus control.** An RT that does not have the capability to become a BC cannot implement the dynamic bus control mode command. This is obvious because this mode command instructs the RT to become the BC on the bus. Note that, for Air Force applications, Notices 1 and 2 prohibit the issuance of this mode command by a BC, although it is not prohibited from being implemented in an RT. The exclusion of this mode command does not preclude an LRU from changing from an RT (or a bus monitor) to a BC on the bus. It simply means that the change must be commanded by some other means than commands on the 1553 bus. This matter is discussed further in the paragraph on backup bus controllers (50.6.3).

d. **Synchronize.** The synchronize (without and with data word) mode command causes some event inside the terminal (or subsystem) to be synchronized with the receipt of this mode command. For instance, a counter could be started or updated, a time register could be loaded, pointers to data areas in subsystem memory could be changed, or whatever.Even though 1553B specifies that it is the RT that shall synchronize, common use includes the synchronization of other subsystem functions as well. The functions that can be synchronized with this mode command are not specified in any way by 1553B. it is therefore obvious that the RT hardware could include a discrete output "SYNC" that is not connected to anything, and this would be a proper implementation of this mode command.

e. **Transmit vector word.** This mode command is commonly used to inform the bus controller of the condition that caused the RT to set the service request bit in a previous status word. The vector word information (i.e., the type of service requested) generally comes from the subsystem. If used in this manner, the BC should not send the transmit vector word mode command if the RT has not set the service request bit in a status word.

1553B does not specify how (if at all) the vector word is to be used, so the common use above is not required. Some systems use the vector word for other information, and nothing precludes the BC from sending the transmit vector word mode command at anytime. Some systems poll the vector word on a regular basis without the necessity of the RT requesting service via the service request bit in a status word.

How this mode command is used depends on the high-level system protocol used. Note that it allows nonperiodic traffic to be implemented on the 1553 bus.

f. **Initiate self test.** This mode command is meant to initiate a built-in self-test of the RT (not of the subsystem). The test to be performed is not defined, and its definition is up to the system and RT designers. Some of the available IC parts define the self-test to be performed (i.e., the self-test is performed by the part, and the designer has no control over it), but some do not. If a given RT specification requires a certain RT self-test, make sure the parts chosen allow this kind of test.

While the RT is performing its self-test, it is typically not able, for a period of time, to respond to commands on the bus in the manner required by 15536. This time period and the not-per-1553B actions allowed are not specified. The open-ended nature of this requirement has created some problems in existing RT designs. Notice 2, therefore, adds some requirements. It is recommended that RTs follow these requirements even if Notice 2 is not a specification requirement for the RT. The requirements added by Notice 2 areas follows:

(1) The RT is required to respond to the mode command (with a status word) before starting the self-test. This is stated in 1553B, but it is not clearly stated that the status word must be sent first.

(2) During the self-test, the RT may respond to commands in one of only three ways. It may not respond, it may respond with the busy bit in the status word set (with no data words), or it may respond normally. In any of these three cases, the RT may also terminate the self-test. If the RT sends any data in response to a transmit command, this data must be valid. The RT may not transmit any spurious signals on the bus as part of its self-test.

Notice 2 does not say anything about the data sent to the RT with a receive message. If, during the performance of its self-test, the RT does not respond, or responds with only a status word in which the busy bit is set, it is recommended that the data not be transferred to the subsystem. It is recommended that the RT respond normally only if the data are also transferred normally to the subsystem.

(3) The self-test function may take no more than 100.0 ms; the RT must have the results of the test by then (unless the self-test was terminated by a superseding valid command) and must be operating normally (i.e., to the requirements of 1553B).

g. **Transmit BIT word.** This mode command is meant to provide the results of the self-test commanded by the initiate self test mode command. The bits of this word are not defined in 1553B; it is up to the system and RT designers to define them. Some of the available IC parts define the self-test and therefore the bits in this register, but some do not. If a given RT's specification requires a certain type of RT self-test, make sure that the parts chosen allow this kind of test.

h. **Reset remote terminal.** Receipt of this mode command must cause the RT to reset to its initial power-upstate (required by Notice 2). The RT must respond with its status word before resetting. Like the initiate self test mode command, the time allowed for the reset function, and the actions the RT can take during the reset, are not defined. The open-ended nature of this requirement has created some problems in existing RT designs. Notice 2, therefore, adds some requirements. It is recommended that RTs follow these requirements even if Notice 2 is not a specification requirement for the RT. The requirements added by Notice 2 are as follows:

(1) The reset function may take no more than 5.0 ms; the RT must be operating normally (i.e., to the requirements of 1553B) after this time period.

(2) During the reset, the RT may respond to commands in one of only three ways. It may not respond, it may respond with the busy bit in the status word set (with no data words), or it may respond normally. If the RT sends any data in response to a transmit command, this data must be valid. The RT may not transmit any spurious signals on the bus during the reset process.

Notice 2 does not say anything about the data sent to the RT with a receive message. If, during the reset process, the RT does not respond, or responds with only a status word in which the busy bit is set, it is recommended that the data not be transferred to the subsystem. It is recommended that the RT respond normally only if the data are also transferred normally to the subsystem.

i. **Inhibit terminal flag bit and override inhibit terminal flag bit.** Receipt of the inhibit terminal flag bit mode command causes the RT to set the terminal flag bit in all transmissions of its status word to 0 (the nonfailed state) regardless of the actual state of the terminal. Receipt of the override inhibit terminal flag bit mode command must return the operation of the terminal to normal. Implementation of this mode command is included internally to most available IC parts, and no external circuitry is needed.

j. **Transmit status word.** This mode command (which is required by Notice 2) causes the RT to respond with only its status word. No other action is performed. One major use for this mode command is to allow the bus controller to read the value of the status word bits following a no-response. Many error conditions require the RT to set the message error bit in the status word and then suppress the transmission of the status word. The BC is thus able to read the status word. Another major use is to verify the proper receipt of a broadcast message, since there is no status word response to the message itself. It is important to note that the status register bits should not be reset upon receipt of this mode command. Implementation of this mode command is included internally to most available IC parts, and no external circuitry is needed.

k. **Transmit last command.** This mode command causes the RT to transmit (as a data word) the last valid command word that it received. It is intended for error-handling routines, so the bus controller can tell

which was the last command that was properly received. As is the case for the transmit status word mode command, the status register bits should not be reset upon receipt of this mode command. implementation of this mode command is included internally to most available IC parts, and no external circuitry is needed.

Although not required by 1553B, it is recommended that all mode commands that make sense for an RT be implemented. Those mode commands for which there is no need in a given RT (e.g., transmit vector word), if not implemented, should be treated as illegal commands, since the system specification should preclude such a mode command from ever being sent to the RT.

50.5.3 Subsystem Interface requirements.

50.5.3.1 Subsystem data interface. The information that passes through the RT must be transferred to or from the subsystem in some fashion and must retain its integrity. The function of the RT is only to format this information as required by 1553B (that is, it changes the data from 1553B format to or from a format that the subsystem can read). The manner in which the information is transferred is not specified in the standard. Nonetheless, there are some common types of interfaces and methods of ensuring data integrity.

DMA interface. The most commonly used interface is a direct memory access (DMA) interface to RAM memory in the subsystem (see figure 50-15). The exact details depend on the type of memory system (probably, but not necessarily, a microprocessor system) being used. For this type of system, the address in RAM memory into which to place each word must be defined.

Frequently, the transmit/receive (T/R) bit and subaddress of the command word are used to address blocks of 32 words of RAM. There is usually both a transmit and a receive block for each subaddress. The (1 to 32) words in the message go into (or come from) sequential addresses in this block. There is no necessity to reserve 32 words for each subaddress, and a simple lookup table could reserve only as many memory locations as were necessary for each subaddress. In a simple system, the T/R bit and subaddress might be used directly as the six most significant bits (MSBs) and the word position (0 to 31) as the five least significant bits (LSBs) of an 11 -bit address field. Some RTs could be even simpler. For instance, if an RT can only receive, the additional 1024 addresses for transmit data (T/R bit= 1) are not needed. Avery simple RT could use fewer than five bits of the subaddress or could always use messages shorter than 16 words, so it would not need the entire address space. Simplifications to this extent are not recommended, though. They severely restrict any other application for an RT designed in this way. The “other application” could even be a modification of the requirements for the current application.

In a somewhat more complicated system, the more significant bits (e.g., in a 16-bit system, the five MSBs) could be either hard-wired in the RT, be selectable by discretes at the RT interface to the subsystem, or be programmable by the subsystem. This would have the effect of mapping the 2048-word (equals 2^{11}) block to any location in RAM but only on an even 2048-word boundary. Alternatively, there could be a word provided by the subsystem that the RT would have to add to each of the 2048 addresses it generated, thus allowing mapping of the block into any location in RAM, with no block boundary restrictions.

If this degree of mapping flexibility is needed, a more common approach is a lookup table (either in hardware (PROM) in the RT or in software in the subsystem) that translates each six-bit T/R and subaddress (or even each 11-bit T/R and subaddress and word position) into a different (potentially noncontiguous) actual RAM address. It is not necessary to reserve 32 words for each subaddress, only the actual number of words in the message. This saves substantial memory space in a system that uses many messages shorter than 32 words and is thus desirable.

In addition to the transfer of data to the subsystem, there must be a control interface. This could be as simple as a discrete (a microprocessor interrupt, for instance) to tell the subsystem when a message has been fully written into RAM. It would also include whatever method the subsystem has of defining the DMA addresses. It could also include a method for sending the subsystem (or allowing the subsystem to read) the command

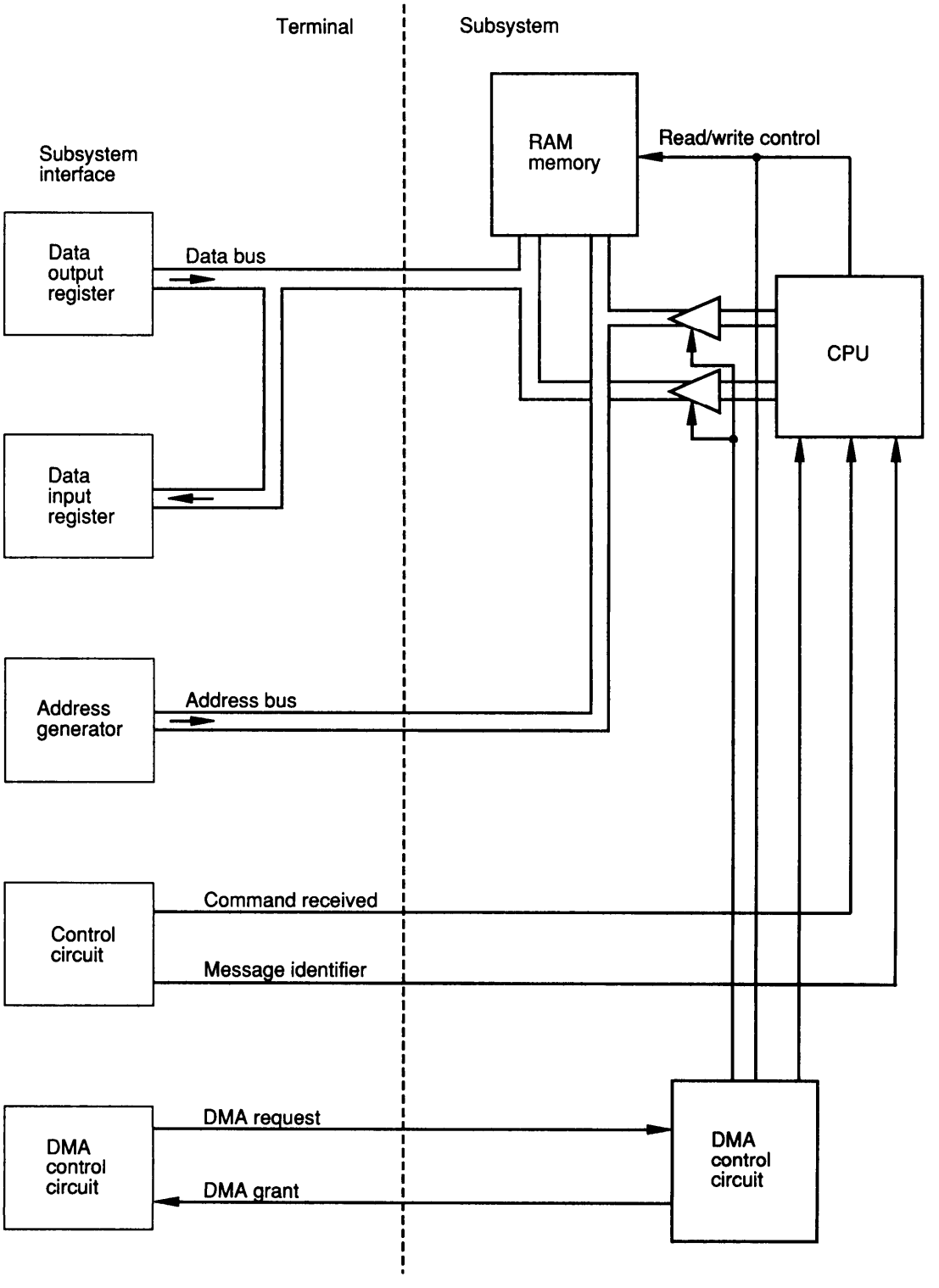


Figure 50-15. DMA Subsystem Interface

word of the message. This allows the subsystem to know what data has been read or written, or what action is being commanded, in the case in which the message is really a command (e.g., a mode command) rather than a data transfer.

Other types of interface. Some RTs (usually older designs) have only a single-word interface (see figure 50-1 6). That is, they provide (or read) data one word at a time from the subsystem as it is received (or needed to transmit) on the 1553 bus. The subsystem is therefore responsible for knowing what each word is, from the command word and the word position in the message, and manipulating the data properly. This system is generally useful only for simple systems, as keeping track of much data in this manner could get very complicated very quickly. In another sense, however, a system of this sort could be thought of as merely partitioning the RT from the subsystem in a different place. In this case, the points mentioned in the previous discussion (on a DMA interface) could still apply, but they would apply to the subsystem design and not to the RT design.

The control interface between the RT and the subsystem in this case would consist mainly of the command word, or some subset of the command word (e.g., the T/R bit and subaddress), so the subsystem knows what to do with the data words it is being sent (or knows which words to provide).

Data buffering and message validation. No matter how data are transferred between the RT and the subsystem, some method must be provided to ensure message integrity. None of the data in a message can

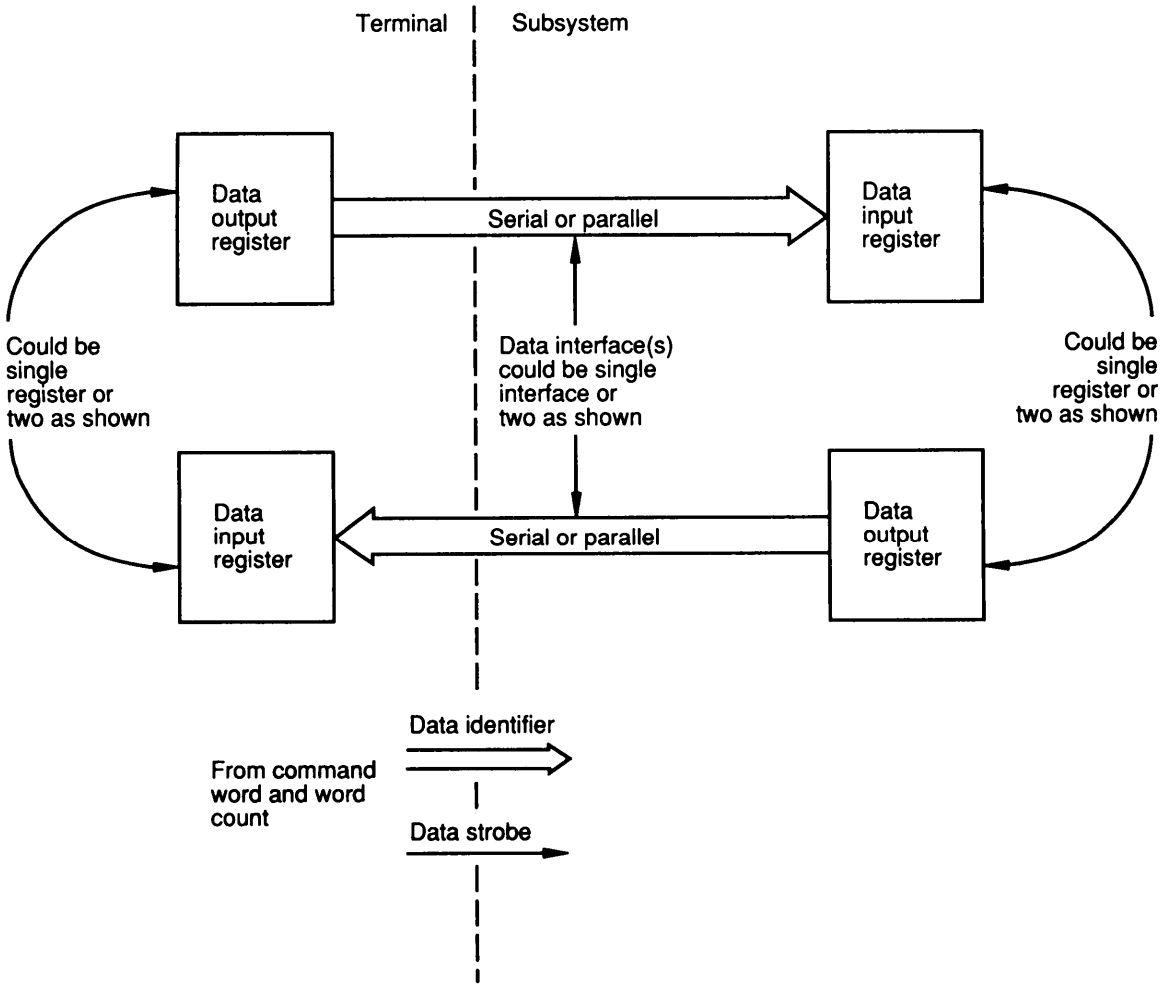


Figure 50-16. Single- Word Subsystem Interface

be used until the entire message has been validated. There must also be no possibility of getting a portion of a block from one message and the rest from another.

Because data are handled differently for receive and transmit messages, there are really two different requirements. In the case of a receive message, the RT stores data somewhere, usually in the subsystem, and the design of the RT and subsystem has to ensure that none of the data can be used until the entire message is complete and valid. One way that this can be accomplished is with a validity 'lag word". The RT would set this tag word to the invalid state when it starts transferring data to a subsystem and only set it to the valid state when the message is complete and valid. Invalid data can exist in the subsystem memory, but software must examine the tag word before any of it is used.

For transmit messages, the RT reads the data, usually from the subsystem; it is up to the subsystem to ensure that all data blocks accessible to the RT are complete and consistent (i.e., all the data are from the same data set or block) when they are read by the RT. Because the RT could be required to read data at any time (i.e., asynchronously to any event in the subsystem), the data that are readable by the RT must be valid at all times. An alternative could be to set the RT busy at those times when this condition cannot be met, but this is not desirable.

For both transmit and receive messages, there is a need for buffering the data. Double buffering, the most commonly used method, is a method of allowing the subsystem to access the data in one message block and the RT to access the data in a different message block. The task of controlling the buffers is sometimes performed by the subsystem, frequently in software. If the latter is the case, the RT does not need to concern itself with this buffering. Some possible schemes in which the RT would be involved are presented next.

In some subsystem interfaces, the subsystem provides a DMA address pointer to the RT. The RT then uses the pointer to calculate the DMA address for transferring the data for each message to or from subsystem RAM. In a system of this type, the subsystem could obviously change this pointer between two (or more) areas of RAM upon being notified of a valid message. That is, the subsystem would be accessing data in one part while the RT accesses data in the other part. In the event of an invalid or incomplete message, the subsystem is never notified of a valid message, the pointer is never changed, and the next (presumably valid) message is transferred to or from the same block of RAM as the previous invalid message.

This approach would be difficult for transmit messages because the subsystem would have to set the pointer to the correct value between the time the command word was received and the time the first word of data would be fetched by the RT, potentially a very short time. Another difficulty of this approach is that there are usually multiple subaddress blocks in RAM, and the subsystem would have to keep track individually of which is the latest information in each of them. An advantage is that no data have to be moved, only a pointer changed, so it takes much less time to change the data soon enough for the next message.

A more practical method of implementing double-buffering by changing the DMA address pointer (as discussed above) is to use a register in the RT to define the valid DMA section for each message the RT is required to process, a maximum of 60 (could be 90 if Notice 2 is a requirement, broadcast is used, and broadcast data are kept separately). This register would have one bit for each message (subaddress and T/R), assuming that only two buffers are maintained for each message subaddress. The RT would use this bit to set the DMA address pointer to one of two values, depending on the value of the bit, either as a direct part of the DMA address (e.g., the next most significant bit) or as part of stable lookup. The subsystem would write to this register, ensuring that the bit for each receive message pointed to the block of RAM that the subsystem was not using and that the bit for each transmit message pointed to the most recent complete and valid block of data.

The subsystem can implement physical double-buffering (as opposed to the "virtual double-buffering" described above) by actually moving the data into and out of the locations where the RT DMAs them. For receive messages, the subsystem would move the data to another location when the RT indicates that the block of data is valid. For transmit messages, the subsystem would move the data block into the RT-accessible

location when it is complete. In both these cases, something would have to be done to prevent partial blocks from being transferred. As the words could only be transferred to or from RAM one at a time, a complete message transfer could take along time. The length of time this could take makes this approach uncommon.

In a system in which there is only a single-word interface between the RT and the subsystem, any buffering must be done in the subsystem. The RT always sends and gets information from the same location in the subsystem. This location could be a DMA address or, more likely, a discrete interface of some sort. Note that this sort of interface should only be used in very simple systems where the data interface would also be expected to be quite simple.

Another method of ensuring message validity is for the RT to buffer the message internally (e.g., in a first-in-first-out [FIFO] register). The RT in this case would not inform the subsystem of the presence of a receive message, nor transfer the data, until the message is complete and valid. As a minimum, the RT would have to buffer 32 data words and the command word (or other message identifier). In the case of an RT-to-RT command, the status word from the transmitting RT might also have to be stored, depending on system requirements. The subsystem would have to be capable of transferring the message from the RT before the receipt of another message could cause any part of the message buffer to be overwritten. This is frequently not feasible but would have to be evaluated in each case.

This approach would also work for transmit messages. The subsystem would have to be capable of reading the command word, determining the proper data, loading the first word of the response before the RT needs to transmit it, and loading the other words at a minimum rate of one per 20 µs. The subsystem would also have to ensure that partially updated messages are not transferred, but because the subsystem would be in charge of the transfer, this should not be a problem.

50.5.3.2 Subsystem control interface. Much of the control interface between the RT and the subsystem is of necessity defined by the type of data interface discussed in the previous paragraph. Other interface requirements are discussed here.

Terminal address. The terminal address interface could be considered to be part of the subsystem interface. It is discussed in 50.5.1.

Valid message notification. The RT's transfer of data on the bus is controlled by the messages received on the bus, not by the subsystem. Depending on the intelligence of the RT, there might have to be a mechanism for the RT to tell the subsystem about the receipt of a valid command or message. This is typically done with a discrete. In many systems, this discrete is used by the subsystem as an interrupt. When it becomes true, the subsystem will do whatever is necessary to service the message.

Data identification. In systems in which the data interface does not provide the identification of the data, there needs to be another interface for this. An example would be the provision of the subaddress field of the command word to the subsystem as five discretes that are valid along with the discrete that indicates a valid message.

Status word bits. Certain bits in the status word are provided by the subsystem, so there must be an interface for these data. This status bit information is generally provided to the RT from the subsystem in the form of discretes, but could also be written to a register in the RT. The bits affected are listed below.

a. **Service request bit.** The subsystem causes the service request bit in the status word to be set when it (the subsystem) wants to cause the bus controller to issue some command to the RT. It is not defined whether the RT should set the bit in only one status word transmission or in every status word transmission until the specified action takes place in response. It is also not defined what should cause the subsystem to reset the request (i.e., the discrete or whatever is used) for the service request bit. Commonly, the RT keeps transmitting the service request bit in every status word until the required servicing of the RT has taken place, but this must be defined in the system specification.

b. **Busy bit.** In the event the subsystem is unable to support data transfer with the RT, it should cause the RT to set the busy bit in its status word transmissions. The notification from the subsystem, as well as the busy bit in any status words sent, should stay set until the condition that is causing the busy condition is no longer true.

It is also possible that the subsystem is unable to support data transfer only for certain messages. For example, if data from a particular message (i.e., a particular subaddress) have not yet been used, and the subsystem desires to prevent its being overwritten, the RT could be set busy only for that particular subaddress. Note that, in some systems and with some data, the subsystem does not care if it misses some data blocks (e.g., navigation information); it only needs the latest information. For other data, every data block must be read (e.g., mission data uploading).

The subsystem should preferably be designed so there are never any busy conditions and, therefore, never any need to set the busy bit. Notice 2 states this explicitly and also defines the conditions in which the busy bit may be set. According to Notice 2, the busy bit may only be set in response to particular commands from the bus controller (i.e., commands specified for this RT that can potentially cause a busy condition, so the bus controller can determine when a nonfailed RT can become busy and when it cannot), or as a result of fault conditions within the RT or subsystem. It is recommended that RTs and subsystems be designed to transfer data quickly enough to eliminate busy conditions, even if Notice 2 is not a requirement for the system. Thus, the busy bit would be used sparingly if at all.

c. **Subsystem flag bit.** In the event of a fault condition in the subsystem that could potentially result in invalid data, the subsystem should cause the RT to set the subsystem flag bit in all status word transmissions. The bit in the status word, as well as the notification from the subsystem, should stay set until the fault condition is no longer present.

It is important to remember the difference between the subsystem flag bit and the terminal flag bit. The terminal flag bit is only set in the event of a fault in the terminal, while the subsystem flag bit is only set in the event of a fault not in the terminal portion of the system.

d. **Other status word bits.** The setting of all the other status word bits is a function only of the RT. That is, the subsystem can have no affect on the value of the rest of the bits. Seethe previous discussion of the status word bits in 50.5.2.2.

Mode commands. Certain information provided in response to mode commands is provided by the subsystem. Therefore, there must bean interface for this data. Most mode commands do not involve any subsystem interface because they involve only the RT. Those that do (or could possibly) are discussed below.

a. **Synchronize (with and without data word).** The definitions in 1553B for these mode commands (4.3.3.5.1.7.2 and 4.3.3.5.1.7.1 2) specify that they are for synchronizing the RT to the bus controller. Exactly what it is that is synchronized and the meanings of the bits in the data word are not specified, this definition being Ieft to the system designer. A common use, however, is to reset (synchronize without data) or preset (synchronize with data) a time tag counter in the RT.

In some applications, however, these mode commands have been used to synchronize functions in the subsystem rather than the RT. Thus, there needs to bean interface. Typically, the RT sets a discrete called “SYNC true for some specified time when this mode command is received (i.e., SYNC is a pulse). The subsystem could use ‘SYNC” as either a discrete or an interrupt.

There could also be a data word passed along (for the synchronize with data word mode command). Typically, this data word would be passed to the subsystem (if required) in the same manner as other data words. Even though there are many mode commands that share the same subaddress (00000 or 11111), there is no problem with the use of the subaddress for addressing because synchronize with data word is the only receive mode command that has a data word that needs to be passed to the subsystem.

b. **Transmit vector word.** The vector word contains information from the subsystem or RT to the bus controller. Typically the vector word defines the condition that caused the service request bit in the status word to be set, or, in other words, the type of service that is required. Thus, if the subsystem is the source of the request for service, it must also be the source of the vector word. Conversely, if the RT is the source of the request, the RT must be the source of the vector word.

The vector word interface with the subsystem is typically the same as for all the other data words. Even though there are many mode commands that share the same subaddress (00000 or 11111), there is no problem with the use of the subaddress for addressing because transmit vector word is the only transmit mode command with a data word that needs to be read from the subsystem. If the subsystem data interface was not of the DMA type, the RT would probably store the vector word in a register so it would be available any time a transmit vector word mode command is received.

50.5.4 REDUNDANCY. Most RT designstoday are dual redundant. MlL-STD-1553B defines a particular mode of dual standby redundant operation in paragraph 4.6.3. The commonly available VLSI parts all support this mode of operation. Notice 1 and Notice 2 (for Air Force applications only) require at least dual-redundant operation and, in particular, the dual standby redundant mode of operation defined in 1553B.

The requirements defined in 1553B for dual standby redundant operation areas follows:

a. The RT must respond to a command on the bus on which the command was received.

b. Only one bus can be actively transferring data at any given time.

c. An RT, while processing a message, must continually monitor the other bus for a valid command. If one occurs, the RT must stop processing the current command and immediately start processing the new command on the other bus. The new command is referred to as a superseding command.

Most of the commonly available IC parts supporT this mode of operation. It is only necessary to include the proper quantity of hardware (i.e., bus interfaces and encoder/decoders) on both buses. When they are interconnected in the proper fashion (as defined in the specifications for the parts used), dual redundancy is provided.

Note that an RT must also be able to properly respond to superseding commands on the same bus, but obviously there are only certain times within a message when a message on the same bus can be detected. About the only time when a superseding command could be detected is during a receive command. The transmitting BC could interrupt the data words, insert an intermessage gap of at least 4 µs, and then send a new command. Note that the requirement for an intermessage gap of at least 4 µs only applies if the superseding command is on the same bus as the previous message.

In the event that more than dual redundancy is required or desired for a given application, some of the available IC parts support up to quadruple redundancy (i.e., four redundant channels). There is no mode of operation defined in 1553B for more than dual redundancy. Therefore, the requirements for a multiply-redundant RT must come from the individual system specification. Some general comments may be made, however. The most common implementation is a simple extension of the dual-redundant requirements presented above. That is, the RT will monitor all the buses involved at all times and always process the most recently received valid command. Another approach is to create a quadruple-redundant RT from a pair of dual-redundant RTs, in which case, the system is really a dual-redundant system in which each channel is also a dual-redundant system. This approach is mandated by Notice 1 (20.7 of Notice 1) for more than dual redundancy. Switching between these redundant RTs would be controlled by the subsystem.

50.5.5 Illegal commands. RTs are allowed, but not required, to detect illegal commands and respond to them with only a status word in which the message error bit is set (4.4.3.4 of 1553B). Illegal commands are valid commands that are not part of a set of commands specified for use with that RT. Note that an RT that does

not implement illegal command detection must respond in form to all valid commands. That is, the format of the response must meet the requirements of 1553B even if the data content is meaningless or the requested action (e.g., for a mode command) did not take place. The RT designer may assume that the bus controller is smart enough not to send an inappropriate command. His only responsibility is to ensure that no invalid transmissions take place on the bus in the event that an inappropriate command is received.

In general, illegal commands are defined at the subsystem level, not the RT level, so definition of illegal commands should not be designed into hardware of the RT. Rather, if illegal command detection is implemented, the set of illegal commands for the RT should be programmable by the subsystem. Alternately, the set could be included in a PROM in the RT; this PROM would be changed in the RT any time the set of legal commands changed, or for a different application. The definition of which commands are illegal must be included in the system specification.

Illegalization can be done on several levels. An RT can detect as illegal only commands that do not match a set of legal subaddresses, without respect to word count. Going further, all word counts except those used for each subaddress can be considered illegal. Note that the term subaddress as used here should be understood to include the T/R bit, so that there are effectively 60 different subaddresses, 30 for receive and 30 for transmit. If broadcast commands are used and Notice 2 is a requirement, the 30 broadcast subaddresses must also be treated separately. Mode commands that are not implemented or used can also be considered illegal.

To implement illegalization on a subaddress level only is not difficult. It requires only a table of all possible subaddresses with a legal/illegal flag for each. Many of the available 1553 ICs provide for an external input to implement this feature. The illegalization of unused mode commands can be implemented in a similar manner, and the parts that implement the first feature typically implement this feature, too. Illegalization of commands down to the word count level, however, is less common, as the table of legal commands must of necessity be much larger (2048 entries versus 64).

Note that detecting an illegal command (when illegal command detection is implemented) is the only case that causes an RT to transmit its status word with the message error bit set. In other cases, conditions that cause the message error bit to be set also cause the suppression of the transmission of the status word. The state of the message error bit is then accessible only with a transmit status word or transmit last command mode command.

An RT may might or might not care if it receives an illegal command. MIL-STD-1553B (4.4.3.4) states “It is the responsibility of the bus controller to assure that no illegal commands are sent out.” The RT is, however, given the option of monitoring for them.

In many cases, the RT doesn’t care if it receives illegal messages. In atypical design in which data are DMAed to the subsystem, all data from unused subaddresses, transmit or receive, are written (or read) from a common memory space, the “bit bucket.” These data are never used by the subsystem, so they can not affect its operation. This scheme also conserves subsystem memory, since RAM space does not have to be resewed for all subaddresses. But if message requirements for the RT ever change, the mapping hardware in the RT would have to be modified.

For this last reason, many terminals are designed for easier expansion and do map data from all subaddresses to different areas of subsystem memory. For this type of design, an illegal command could take data from or overwrite a memory location which was being used for some other function. In this case, the designer must be aware that an illegal command could cause problems.

Several reasons that an RT designer would want to monitor for illegal commands are discussed below.

a. The primary concern is that an illegal command could cause misleading information and thereby jeopardize safety. An example of this would be an RT in a display device. If an illegal command were

received, it might cause erroneous information to be displayed. The operator could act on this information, with potentially disastrous consequences.

b. The ability of an RT to detect illegal commands has provided great assistance during systems integration and test. The setting of the message error bit in the status word response is easily detected by most 1553 test equipment, whereas responding "in form" is very difficult to detect.

c. Illegal command detection has been used as part of maintenance and test. Certain commands (such as the reset remote terminal or initiate self test mode commands) maybe extremely useful on the ground during tests or maintenance, but could cause disastrous effects during a mission. Some hardware designs have included a "weight-on-wheels" input to the illegal command detection circuitry to illegalize these commands while in the air but make them legal while on the ground.

50.5.6 Data wrap-around. Many RTs include a data wrap-around function in which data words sent to the RT with a receive command are sent back to the BC with a subsequent transmit command. Notice 2 requires all RTs to implement such a capabiiity. Notice 2 only requires that the data wrap-around function work properly if a transmit command to the data wrap-around transmit subaddress follows immediately (i.e., with no intervening valid commands to that RT) a receive command to the data wrap-around receive subaddress, and both commands are for the same number of data words. That is, there is no requirement that the RT permanently store the data words. There is no prohibition, however, to an RT wrapping around data even though the receive and transmit commands are not adjacent or the number of data words are not equal.

Notice 2 suggests, but does not require, that subaddress 11110 (30 decimal) be used for both the receive and transmit subaddresses for this function. The reason for this is that this subaddress historically has been used for data wrap-around. Some of the available 1553 ICs implement this function using subaddress 30, with no provision to select any other subaddress. If any other subaddresses are specified, the selection of IC parts that are available is much smaller.

The data interface with the subsystem determines to a large measure how this function can be implemented. If the RT includes a message buffer in its hardware, the data wrap-around function can be implemented by reading back the buffer in response to a transmit command with the wrap-around subaddress (typically 30). It is not required (by Notice 2) that the RT check that the data in the buffer were sent to the RT to the receive wrap-around subaddress. It is recommended, though, that this be a condition on the operation. That is, it is recommended that a transmit command to the wrap-around subaddress should only readout the buffer if the immediately previous command was a receive command to the receive wrap-around subaddress. Note that this recommendation is for an RT that includes a message buffer in its hardware which always contains the latest message.

A similar method could be implemented even in those RTs that do not normally buffer messages in hardware. A special hardware buffer could be included only for the data wrap-around test. Transmit commands to the transmit wrap-around subaddress would write to this buffer, and receive commands to the receive wrap-around buffer would read from it. This approach adds substantial circuitry to the RT, so it is not recommended unless it is deemed absolutely essential by the system designers that the wrap-around test involve only the RT and not any part of the subsystem.

The methods presented above do not involve the subsystem in the performance of this function in any way. Technically, the requirements in Notice 2 state that only the RT should be involved in the data wrap-around function. In practice, many systems do use portions of the subsystem in the performance of this function. In fact, to accomplish the intent of the test, the same data paths that are used for normal messages should be used for the wrap-around function. This would normally include the data buffers in the subsystem. All the other possibilities presented below do involve some part of the subsystem.

In a system with a DMA data interface to RAM in the subsystem, the wrap-around function must necessarily involve writing to RAM and then reading back from RAM. If the system includes a DMA pointer lookup table,

it would be easy to point the receive wrap-around subaddress to the same block of RAM as the transmit wrap-around subaddress. This would automatically implement wrap-around. There would also be no limitation as to intervening commands or the number of data words.

In a DMA system without a DMA address lookup table (i.e., one in which the DMA address is formed directly from the T/R bit and subaddress of the command word), things area little more complicated. The RT could be designed with special processing such that the T/R bit portion of the DMA address is always in one state for commands to the wrap-around subaddress, receive or transmit. This assumes that the receive and transmit wrap-around subaddresses are the same. Alternatively, the subsystem could be required to move data from the receive wrap-around subaddress RAM block to the transmit wrap-around subaddress RAM block on receipt of the valid and complete receive command.

In a system with a simpler single-word subsystem data interface, the subsystem would have to be responsible for providing the correct data in response to a valid command to the transmit wrap-around subaddress. The design of the subsystem would determine how this could be accomplished.

50.5.7 Notice 1. and Notice 2 considerations. The additional requirements in Notice 1 and Notice 2 to 1553B were discussed previously (50.4.4). Those items that affect the design of RTs are discussed further here.

50.5.7.1 Notice 1. Notice 1 applies to all Air Force aircraft internal avionics applications (per section 20 of Notice 1). The requirements therein that affect the design of an RT (as opposed to general requirements) are as follows:

a. Certain mode commands (dynamic bus control, inhibit terminal flag bit, override inhibit terminal flag bit, selected transmitter shutdown, and override selected transmitter shutdown) may not be issued by BCs. Therefore, it is not necessary for an RT to implement them. Their implementation is not prohibited, however, and it is recommended that an RT be designed so that it does implement all mode commands.

b. BCs are prohibited from issuing broadcast commands, but an RT has the option of implementing the capability to accept data from a broadcast command should it ever receive one. An RT may also ignore broadcast commands. Either approach is acceptable, and no general recommendation can be made. If there is a chance that the RT would be used in an application in which broadcast commands are used, then the RT should probably be designed to accept them. Although the terminal address 11111 (binary) is reserved for broadcast commands, some of the IC parts available do accept 11111 as a terminal address. If one of these parts is used, it is very important that 11111 never be set as the unique terminal address input to the RT.

c. An RT is required to be able to recognize that a subaddress of 00000 identifies a mode command. An RT is encouraged to be able to recognize 11111 (binary) also. The requirement in 1553B (4.3.3.5.1.7) could be interpreted as allowing an RT to be designed to accept only 11111 as the mode command indicator. This section of Notice 1 clarifies the requirement. It is recommended that all RTs be designed so that they treat either 00000 or 11111 as a mode command indicator.

50.5.7.2 Notice 2. Notice 2 applies to all dual standby redundant applications for the Army, Navy, and Air Force (per 30.2 of Notice 2). The requirements therein that affect the design of an RT (as opposed to general requirements) are as follows:

a. RTs are required to be assignable any terminal address from 00000 to 11110 (binary), and changing the terminal address must not require the modification of any part of the RT. Also, no single-point failure may cause an RT to assign itself a false terminal address. This is discussed in the terminal address section (50.5.1).

b. RTs are required to be able to recognize subaddresses of both 00000 and 11111 as indicating a mode command. There is also the requirement that 00000 and 11111 cannot convey different information (i.e., they must be treated totally equivalently by the RT).

c. RTs are required to implement at least four defined mode commands (transmit status word, transmitter shutdown, override transmitter shutdown, and reset remote terminal). This does not prohibit an RT from implementing all the other mode commands, and it is recommended that all RTs be so designed.

d. There are requirements defined for response to reset remote terminal and initiate self test mode commands. These requirements are discussed in 50.5.2.3.

e. Most of the bits in the status word are defined as either required or prohibited. Implementation of the message error bit is required. The instrumentation and reserved bits must always be set to 0. There are additional requirements on the busy bit, which are discussed in 50.5.2.2.

The rest of the additional requirements are pretty much common sense, but the requirements are stated to decrease ambiguity. If the RT implements the broadcast option, the broadcast command received bit must be implemented. If the subsystem has the capability of self-test, the subsystem flag bit must be implemented. If the RT has the capability of self-test, the terminal flag bit must be implemented.

It is recommended that an RT be designed to implement all status word bits that make sense for the application. Most of the available VLSI IC implementations of RTs do implement all the status word bits.

f. Broadcast mode commands are permitted to be sent by the BC. The real value of this capability is for broadcast synchronize (with and without data word) mode commands. With this mode command, all RTs on the bus can be simultaneously synchronized and thus synchronized to each other.

An RT is not required to accept broadcast BC-to-RT (receive) commands, but is not prohibited from having the capability. For ease in design, most existing designs that accept broadcast mode commands also accept broadcast receive commands.

An RT that implements receipt of broadcast receive commands must be capable of distinguishing between a broadcast and nonbroadcast message to the same subaddress for nonmode commands. This information must also be provided to the subsystem. A simple method of notifying the subsystem that the command being acted upon is a broadcast command is to provide the command word to the subsystem (it has 11111 in the terminal address field). Another method is to have a discrete indicating that the current message is a broadcast message. Some implementations do not provide this capability (of notifying the subsystem of the broadcast or nonbroadcast status of a message), so they are required (by Notice 2) not to implement broadcast receive commands.

g. RTs are required to implement a data wrap-around function. That is, the RT is required to be able to receive a message with its maximum number of data words (typically 32) and then to transmit them back. The subaddress 11110 (binary) is suggested, but not required, for both the transmit and the receive subaddresses for this function.

The requirement, as it is written, requires that this function be provided in the RT, as opposed to the subsystem. Some terminals implement it using the subsystem. For practical purposes, and because the dividing line between the RT and the subsystem is frequently blurred, this is acceptable. Implementation of data wrap-around is discussed in 50.5.6.

h. An RT is required to implement (as a minimum) all nonbroadcast message formats except mode command with data word. An RT is not allowed to distinguish between data associated with an RT-to-RT command and data associated with an RT-to-BC or BC-to-RT command. Since most of the VLSI ICs available today for the design of RTs do not permit the subsystem to know whether the data were from an RT-to-RT command or not, this second requirement is generally of no consequence.

There are requirements in some applications of 1553B, however, in which this could be a problem. In MIL-STD-1760A, for instance, two subaddresses(19 and 27) are restricted to nuclear critical data, and the use

of RT-to-RT data transfer for these data is prohibited. The requirement mentioned above, that the RT not distinguish between normal (i.e., RT-to-BC or BC-to-RT) and RT-to-RT data, makes this impossible. That is, MlL-STD-l760A requires that RT-to-RT messages be distinguished from BC-to-RT messages (and rejected if they are to subaddresses 19 or 27), but 1553B Notice 2 prohibits this. Although the common VLSI ICs do not support this requirement, there are IC parts under development that will.

i. The receiving RT in an RT-to-RT message transfer is required to check the response time (and the proper response) of the transmitting RT. If the first data word in the response occurs later than 60 µs after the (receive) command to the receiving RT, the message is invalid. It is also recommended, but not required, that the receiving RT verify the proper occurrence of the transmit command and the transmitting RT's status word and to treat the message as invalid if the transmit command and status word are not proper.

   This requirement could cause design problems, as not all the available 1553 terminal ICs implement this type of check, and those that do would not necessarily meet this specific requirement. There are, however, IC parts under development that will.

50.5.8 RT design example. The Redescribed in this example is a dual-redundant RT with a single-message subsystem interface. It has a modified DMA subsystem data interface and notifies the subsystem every time a valid message is received. It supports all the 1553B message formats (except broadcast) and all mode commands (except dynamic bus control).

50.5.8.1 General description. Figure 50-17 is a block diagram of the example RT. The major components are four VLSI ICs: two encoder/decoders, a protocol control IC, and a subsystem interface IC. The RT also includes two FIFOs, a RAM, a clock oscillator, and two one-shots (fail-safe timers). Note that these are all actual, available ICs. By including the FIFOs and the RAM in the subsystem interface block in the overall terminal block diagram (figure 50-1), the partitioning of the example matches closely the general block diagram.

This RT is a dual-redundant terminal for transformer-coupled stubs. Design of the analog section (transformer and transceiver) was covered in 50.3, which also included two design examples, so it is not discussed in this section.

The encoder/decoders and the protocol control unit IC connect together with several control signals and a 16-bit parallel bus. These parts are designed to be used together, so the interfaces between them will not be discussed in detail. The same 16-bit bus is also used to transfer data to the subsystem interface section.

50.5.8.2 Subsystem interface. This example uses a general microprocessor backplane bus interface. Eleven bits of addressing are required, and the data are provided on a 16-bit parallel data bus. The data read/write control signals are common, so this RT could probably be used with many types of subsystem interfaces (i.e., microprocessor backplane buses) with little modification.

Subsystem data interface. There is a 2K by 16-bit data RAM included as part of the RT for the data. The data RAM is mapped in 32 word blocks by the T/R bit and subaddress fields (six bits) of the message command word. There are thus 2^6 (64) blocks of 32 words, which comes to 2K words.

The data RAM may be accessed by either the RT or the subsystem. The input RT_SELECT is provided to allow the subsystem processor access to this memory. It may be controlled by the processor, either by a discrete or by the logical OR of selected higher-order address bits, to map the data RAM into the processor's address space.

The subsystem uses the signals DATA_SELECT and WRITE to control the data RAM; the output ACKNOWLEDGE becomes true when the RT grants access to the data RAM. The data RAM is addressed by the subsystem by the 11-bit address bus (2^{11} equals 2K) and the data words are provided on the 16-bit data bus.

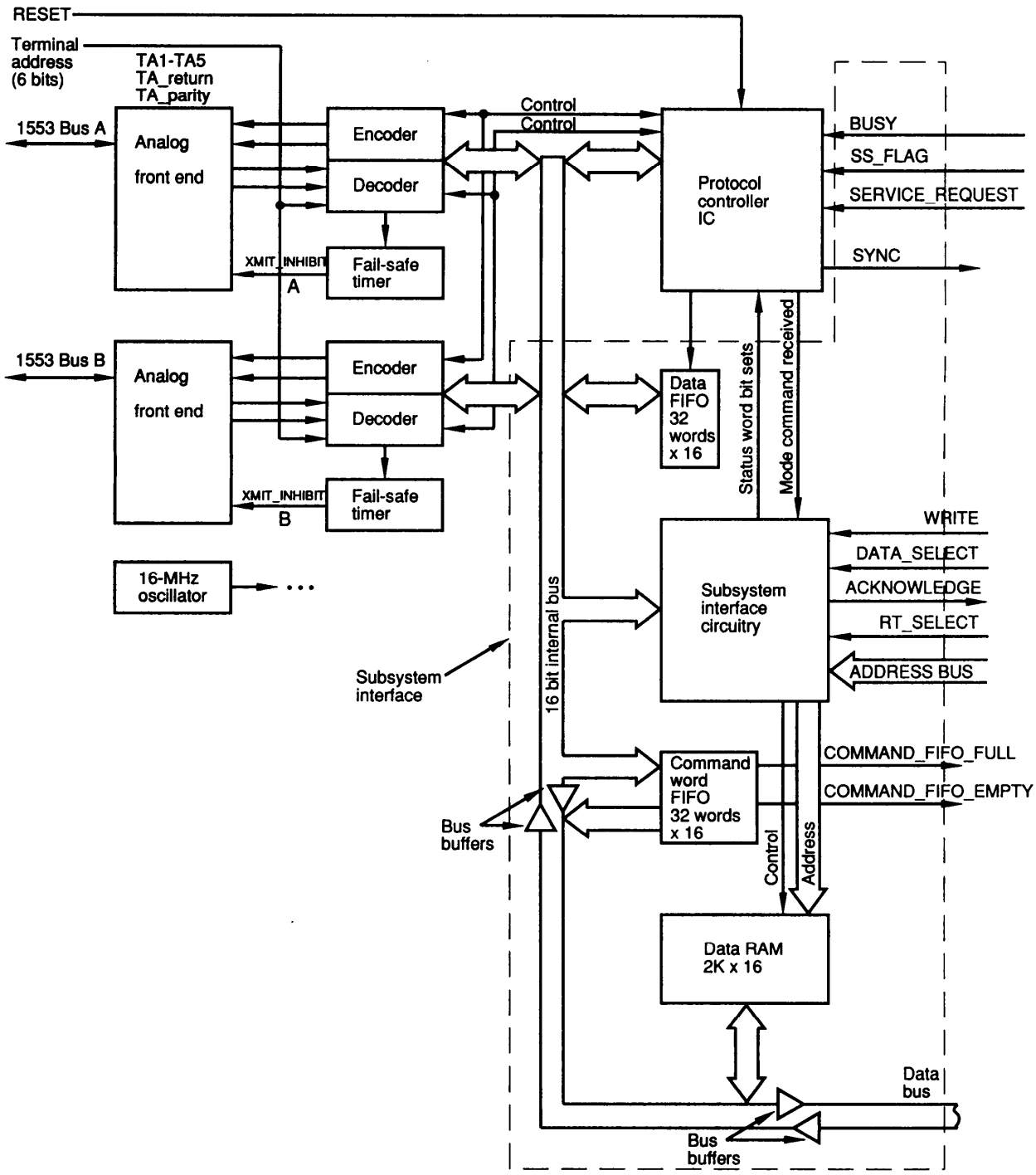


Figure 50-17. Block Diagram of Example RT

The RT stores data words in the data FIFO as a message is being received. After the message is complete and valid, the data words in the data FIFO are transferred to the data RAM. If the subsystem is accessing the data RAM at the time, the RT waits until the access is complete. While the RT is transferring data words to the data RAM (a maximum of 40 µs for a 32-word message), the subsystem will not be allowed access to it.

Upon receipt of a valid transmit command, the RT transfers the required data words from the data RAM into the data FIFO. This transfer also takes a maximum of 40 µs. The RT assumes that the proper data have been written into the data RAM by the subsystem at some time in the past.

Command words. Command words are loaded by the RT into the command word FIFO on receipt of every valid command. This FIFO can hold 32 command words. The signals COMMAND_FIFO_EMPTY and COMMAND_FIFO_FULL are provided to keep the subsystem informed about its status. The subsystem reads the command word FIFO by reading address 0 of the RT's data RAM.

Mode commands. The RT handles most mode commands automatically. It provides the required actions and data words with no intervention by the subsystem. Because the subsystem generally has no interest in these mode commands, the command is not written into the command word FIFO. Thus, no notice is given to the subsystem that a command has been received.

The two exceptions are synchronize (with and without data word) and transmit vector word. The data word received with the synchronize mode command (mode code 17) is mapped into the RAM as if it were the 17th data word insubaddress 11111 (binary). There is also an output SYNC to the subsystem which pulses for 250 ns upon receipt of a valid synchronize (with or without data word) mode command (mode codes 17 or 1). The data word for the transmit vector word mode command (mode code 16) is mapped into the RAM as if it were the 16th data word insubaddress 11111 (binary). For these two mode commands, the command word is written into the command word FIFO and thus the subsystem is made aware of their receipt.

Double buffering. There is no double buffering of the data implemented by the RT. If double buffering is a requirement, the subsystem must copy the data in the RT's data RAM into its own memory and implement multiple buffer areas on its own.

Note that the data FIFO performs some of the functions of a double buffer. The data FIFO stores the partial message as it is being received. Partial messages are never accessible to the subsystem because they are not transferred from the data FIFO to the data RAM until the entire message is complete and valid.

Subsystem control interface. The RT indicates to the subsystem that a valid message has been received by loading the command word into the command word FIFO and setting COMMAND_FIFO_EMPTY false.

The only other control inputs from the subsystem are the three discretes BUSY, SS_FLAG and SERVICE_REQUEST. These three discretes cause the corresponding bits to be set in the RT's status word responses as long as the discretes are true. Also, in the case of BUSY, the RT will not send any data words in response to any transmit commands.

50.5.8.3 **Other interface.**

Reset. The input RESET will reset the RT to its power-up default state. The RT will await the presence of a valid command with its terminal address. Note that the 2K data RAM will not be cleared by the RESET input.

Terminal address. The RT's uniqueterminal address is controlled by the seven terminal address inputs: TA1 to TA5, TA_PARITY and TA_RETURN. TA1 to TA5 form the actual terminal address. TA_PARITY must be set to odd parity. That is, the total number of 1s in the six bits, TA1 to TA5 and TA_PARITY, must be odd. Each input is set to 0 by connecting it to TA_RETURN and to 1 by leaving it open (i.e., connected to nothing). A failure of one of the terminal address inputs will cause the parity check to fail. The RT is thus prevented from reading an incorrect unique terminal address and from responding to the wrong commands.

The RT will read the terminal address inputs every time a command word is received. Only if TA_PARITY is correct and the terminal address inputs match the first five bits of the command word will the RT proceed with the processing of the command word. A failure in the terminal address inputs will thus be detected by the RT no matter when it occurs.

50.5.8.4 Clock. The RT requires a 16-MHz clock, and a 16-MHz oscillator is provided to generate it.

50.5.8.5 Fail-safe timer. There are two fail-safe timers, one for each of the transceivers. They are implemented by one-shot multivibrators connected to the XMIT_INHIBIT inputs of the transceivers. The timer is set to time out in about 725 µs (the minimum and maximum timeout values fall close to the required values of 660 µs and 800µs). A protocol controller IC output starts the encoder for each transmission. This same signal is used to start the appropriate fail-safe timer. If it ever times out, the transceiver will be shutdown via its XMIT_lNHIBIT input.

50.5.8.6 Normal operation. The RT reads and decodes every word it sees on the 1553 bus. The word is shifted serially into a 40-bit shift register in the decoder at a 2-MHz rate. Thus, each bit in this register represents one half-bit time. When the first six bits in this register (representing 3 µs of data) form a valid sync, the rest of the word is checked for valid Manchester encoding and for parity. If the sync is a command sync, the first 10 bits (which represent the first five decoded bits) are checked against the five terminal address inputs. These first five bits are also checked to see if they are 11111, indicating a broadcast command. If OK, the word and a flag indicating that it is a valid command or data word are passed to the protocol controller IC. Another flag is available indicating that the word is a valid broadcast command, but this flag is not connected in this design. Thus, the RT will not recognize broadcast commands.

There is also a flag to the protocol controller IC indicating on which bus channel the command was received. Thus, the protocol controller IC is able to send the response on the correct bus.

The protocol controller IC then interprets the command word. A receive command is followed by 1 to 32 data words. A transmit command requires the RT to fetch and send 1 to 32 data words. A mode command causes the RT to perform some special function.

Receive command. For a receive command, the data words that follow are loaded into the data FIFO as they are received. Each is checked for validity by the decoder. The protocol controller IC knows how many there are supposed to be from the word count field of the command word. Only when the message is complete with the correct number of data words is the message declared valid. The words in the data FIFO are then transferred to the data RAM starting at:

RAM address = subaddress * 32.

At the same time the data words are being transferred to the data FIFO, the protocol controller IC provides the status word to the encoder. The encoder in turn encodes it and transmits it on the bus.

Transmit command. For a transmit command, the data words are provided by the RT. The proper number of data words (defined by the word count field of the command word) are read from the data RAM to the data FIFO starting at:

RAM address = subaddress * 32 + 1024.

Note that no check is done by the RT on the validity of these data words. The RT assumes that the subsystem has written the data words into the data RAM at some time in the past.

The protocol controller IC provides the status word to the encoder while the data words are being transferred to the data FIFO. The encoder, in turn, encodes it and transmits it on the bus. The data words are then transferred from the data FIFO to the encoder and transmitted. This continues until the data FIFO is empty.

Wrap-around command. A receive command to subaddress 11110 (binary) is interpreted as a wrap-around command. The data words are received normally and loaded into the data FIFO, but they are not transferred to the data RAM at the conclusion of the message. If the subsequent valid command to this RT is a transmit command to subaddress 11110, and if the word counts are the same for the two commands, the data FIFO is not loaded from the data RAM. The data words from the receive command are then sent out on the bus. It is permissible for the bus controller to send the receive command and not follow it with the transmit command. In this case, however, the stored data words are lost and the test must be restarted.

Note that subaddress 11110 is reserved for this function and, therefore, may not be used for data transfer with the LRU. The protocol controller IC has a pin that maybe used to disable this mode of operation, but this has not been done in this design.

Mode command. For a mode command, the RT's actions depend on the particular mode command. Most mode commands are processed by the protocol controller IC with no external help. The protocol controller IC maintains registers internally for the last command word, the status register, and the BIT register. These are transmitted in response to the relevant mode commands.

The initiate self test mode command causes the RT to check the fail-safe timers. The result is stored in the BIT register bit 0. The reset remote terminal mode command causes the RT to return to its power-up default state. All internal registers and the data FIFO are cleared. The data RAM, however, is not cleared. The synchronize and transmit vector word mode commands are discussed above (see 50.5.8.2). The other mode commands cause some change in the mode of operation of the protocol controller IC.

RT-to-RT command. For an RT-to-RT command, if the RT is the transmitting RT, nothing different is done. The RT sends its status word and the required number of data words on the bus. If the RT is the receiving RT, the next word on the bus is checked to see if it is a transmit command to another RT. If so, the protocol controller IC reads the terminal address. It then waits for the other RT to send its status word and the required number of data words. The status word is not stored anywhere, but the data words are handled just like for a normal receive message. If the status word has the wrong terminal address, or if the number of data words is incorrect, the protocol controller IC declares the message invalid.

50.5.8.7 **Error handling.** There is little the RT has to do in the event of an erroneous (invalid) message. Invalid commands are totally ignored; they never get passed from the decoder to the protocol controller IC. Invalid data words in a receive message cause the protocol controller IC to stop processing the message, clear the data FIFO, and start looking for another command word. The same is true if there are too few or too many data words. In any case, the message error bit in the status register is set and the status word is not transmitted, as required by 1553B.

There are no errors to handle in a transmit message (assuming the command word is valid); the subsystem interface IC will transmit whatever is present in the data RAM. It is of course possible that these data are not proper, but this would be a subsystem problem, not an RT problem. The RT has no way of knowing the validity of the data.

The RT checks RT-to-RT messages for the proper terminal address of the transmitting RT (assuming this RT is the receiving RT). If there is an error, the message error bit is set in the status register and the status word is not transmitted.

The RT checks the two commands (one receive and one transmit) involved in a wrap-around test for the same word count. If the second (transmit) command word count does not match the first, the message error bit is set in the status register and the status word is not transmitted.

The RT does not implement illegal command detection except for unused or reserved mode commands. For these messages only, the status word (only) is transmitted with the message error bit set.

50.5.8.8 RT design example summary. The example RT discussed in this section is one of moderate complexity. Some of its limitations are discussed here.

Its memory addressing for data transfer is fixed and is a direct function of the message subaddress and T/R bit. Each message type is also assigned 32 words in memory regardless of the message length. There is no scheme for multiple buffering of the data.

On the other hand, all mode commands and message formats are handled properly (i.e., per the requirements of 1553B). A data wrap-around testis provided using subaddress 11110 (binary). Partial messages are never passed to the subsystem in the event of an error in the latter part of a message. Indication of the reception of each message is provided to the subsystem but there is no requirement for the subsystem to do anything with this information.

50.5.9 Multiple-message RT design example. The example BC presented in 50.6.6 is also capable of acting as an RT. Most of the information presented on the operation of the BC also applies to its operation as an RT. See 50.6.6.6 for a brief discussion on the operation of this terminal as an RT.

50.6 BUS CONTROLLER REQUIREMENTS. Many of the aspects of remote terminal (RT) design that have already been discussed also apply to bus controllers (BCs). The major difference is that a BC is controlled by its subsystem interface whereas an RT is controlled by commands received on the bus. An effect of this is that the standard says much less about how a BC must operate than it does for an RT. In fact, there is only one paragraph of requirements in 1553B (4.4.2) for BCs, and its only real requirement is that there be only one BC on a bus at a time.

Because there are, typically, one BC and many RTs on a bus, there are many fewer BCs than RTs built. Also, expendable stores (devices carried by an aircraft and normally used up during a mission, like bombs or missiles) tend to have RTs and not BCs, which further increases the ratio of RTs to BCs built. Thus, there are fewer choices in parts with which to implement a BC. The more modern and more integrated parts are the exception to this, as these parts tend to incorporate both BC and RT functionality, and one or the other can be selected.

ABC initiates messages on the 1553B busby transmitting a command word. For RT-to-BC messages, the BC must receive any data words sent in response to the command word and transfer them to the subsystem. For BC-to-RT messages, the BC must transfer the required number of data words from the subsystem and transmit them on the 1553 bus. For RT-to-RT messages, no data words are required to be exchanged with the subsystem. Note that, even though it's not required, many BCs do indeed read data words from RT-to-RT messages and pass them to the subsystem. An example of a system design that requires the BC to read RT-to-RT message data is presented in 50.6.3.1.b. (This example is a method for a backup BC to stay informed about the state of the system.) It is recommended that the BC does monitor the RT-to-RT message for proper format, even if it does not read the data (Notice 2 states this explicitly; see 50.5.7.2).

There may or may not be a need to transfer status words or other status information to the subsystem, depending on system requirements. The BC is also responsible for checking the response on the bus for correctness and, in most systems, for passing an indication of this correctness to the subsystem. Note that, for a correctly transferred message, the indication of correctness passed to the subsystem might be nothing at all; only incorrect messages might need to be indicated.

50.6.1 Subsystem data interface. The subsystem data interface does not need to be any more complex than for an RT, and generally isn't. The only difference is that data words are transferred to the subsystem for transmit messages and from the subsystem for receive messages, which is opposite from an RT.

There are some additional options available to a BC that are not available to an RT. Because the BC initiates the message, it can specify at that time exactly where the data words returned are to be placed. Assuming a DMA interface, the DMA address for the first word in the message can be written into a register or memory

location accessible to the BC. This would give the subsystem software very explicit control over the data. It would be possible for the subsystem to allocate only as many memory locations as there were words in the message.

50.6.1.1 Mode command data storage. For mode commands, there is an additional complication for BCs that does not apply to RTs. For an RT, there was only one transmit and one receive command that needed to exchange a data word with the subsystem. Thus, even though all mode commands have the same subaddress, it was satisfactory to use the subaddress and T/R bit fields to address these words in memory. BCs have to deal with all mode commands that pass a data word (three transmit and three receive mode commands), so the addressing scheme used to define the data location must be be more complex.

One possibility is to use the word count field, as in this case it is really the mode command identifier. Mode codes 16 through 21 have an associated data word. If a block of 32 words is assigned to every subaddress, the designer could simply assign subaddress block 00000 words 16 to 21 for this function. Note that mode commands with a subaddress of 11111 (binary) should probably be mapped into this same memory block. If a scheme is used that assigns only the required number of words for each subaddress, these six data words could be assigned to the six locations for subaddress 00000 (and 11111). Still another possibility is to use six registers (in a separate area of memory, perhaps) for these data words.

50.6.1.2 Status word storage. Because the bits of the status word can indicate message validity (in particular, the subsystem flag bit), some applications store it along with the data words in the memory buffer. Other applications store the status word separately, if it is stored at all. This allows multiple blocks of 32 data words to be stored contiguously in memory. Contiguous data storage is useful if these many data words all represent one item of information. The designer should analyze the overall system requirements and determine which method of storage is best.

In most systems, the data are available at all times to the subsystem software. The software must determine the validity of the data (e.g., by looking at the subsystem flag bit or any validity bits associated with the data words) and which of any multiple buffers to use. It is also possible, if data integrity is an overriding concern, to move completed buffers to and from another memory location for use. However, the rather high penalty of having to copy each message discourages most users from applying this technique.

50.6.2 Subsystem control interface. The subsystem control interface for a BC is normally more complex than that for an RT because the entire operation of the BC must be controlled. Items that always need to be passed include the command words (1 or 2) for the message and the data words (0 to 32) that are sent or returned (or pointers to this information). Note that there are two command words in an RT-to-RT message. Typically there is an interface to cause the message to be initiated and, generally, an indication if the message was completed without error or not. There normally has to be some interface to control the mode of operation of the BC. Examples of modes of operation would be whether (and in what circumstances) to retry failed messages and on which bus of a redundant bus system to initiate the message.

Because the BC controls the bus, it needs to perform more control functions than an RT. This doesn't mean that the BC necessarily has to be more complex or intelligent, but generally it is. Due to the complexity of a typical BC application, a BC's interfaces are commonly structured as registers that the subsystem writes to and reads from. In microprocessor terms, these registers would exist in the subsystem's I/O space.

Several control functions that are commonly performed by the BC rather than the subsystem are discussed next.

50.6.2.1 Automatic retries. As mentioned above, the BC is required to detect improper responses. A BC can be designed to autonomously initiate the message transfer again (to retry) if certain responses are detected. The bus on which the retry will take place (for a redundant bus system) needs to be specified. This would generally be programmable by the subsystem. The maximum number of retries also needs to be specified. The value could also be programmable but, more frequently, is fixed in the design. Most commonly,

there is only one retry attempted, and it is done on the opposite bus (of a dual-redundant pair). There is a lot of debate on whether this is a good approach, and it needs to be evaluated for each system design. It is probably a good idea in this case that the BC be designed to switch to the opposite bus and then stay on that bus, rather than returning to the other bus for its next message. This prevents bus traffic from being doubled forever if one of the redundant buses fails completely.

The particular improper responses that are to trigger a retry attempt must be defined. Conditions that could occur and that would logically cause a retry are listed here. The requirement for a retry in each of these conditions should be evaluated, and the set of events that will trigger a retry defined, for each system. This list is not meant to be complete, only suggestions:

a. No response.

b. Message error bit set in a status word response.

c. Word or message format errors in the response (e.g., a Manchester error or an incorrect word count).

d. Illegal (unused) bits set in a status word response.

e. Busy bit set in a status word response.

f. Other (defined) bits set in a status word response.

The most common improper response is no response (when a response is expected). Almost all systems that implement automatic retries will retry in the event of a no-response error. The other conditions listed above are somewhat less common but are listed in approximately the order of their commonness.

Any scheme for implementing retries must ensure that any data received from the retried message are not corrupted by being mixed with the data from the first attempt. This would normally not be a problem because the BC must do this anyway for separate messages. If the BC treats the second attempt as something other than an entirely new message, however, consideration must be given to this issue. (Seethe section on data buffering, 50.5.3.1).

50.6.2.2 Multiple message sequencing. Some BC designs have the capability to automatically initiate multiple messages from one subsystem instruction. This is generally implemented with a transaction table, or a list of messages (transactions) and their associated parameters (modes of transmission, data addresses, etc.). This list can exist either in the BC itself, in which case it must be written to the BC by the subsystem, or in subsystem RAM, in which case only an address pointer needs to be written to the BC.

Inclusion of a multiple message feature relieves the subsystem of some of the work necessary to transfer data on the 1553 bus at the expense of a more complex design for the BC. In essence, some of the intelligence of the system is moved from the subsystem into the BC, typically making the BC an I/O processor of the subsystem microprocessor. Much of the rest of the BC design section will assume that the BC has the capability to handle multiple messages automatically via a transaction table in subsystem RAM.

Message list generation and chaining. The interface between the BC and the subsystem processor for the transfer of data is shared memory (RAM). Mapping of the data within the memory is usually a function of the subsystem and its particular needs. However, the generation and chaining of the messages to be transferred on the data bus is an integral part of the BC design.

The list itself can be stored either in shared memory (and accessed by DMA) or in a set of registers in the BC. Stated a different way, the list can be located either in the subsystem's memory space or in its I/O space. In order to allow the message list to be arbitrarily long and complex, it is normally located in shared memory; the subsystem designer must allocate sufficient memory space to the list for his application. The designer must also ensure that a message list once the BC has been commanded to start it. If it is necessary to interrupt

or modify the list of messages, the subsystem must ensure that the modification is made in a manner that will not confuse the BC.

Various methods have been developed for generating message lists. Two methods have been most commonly used: stacks and linked lists. Each has its advantages and disadvantages.

a. **Message stacks.** The stack method is the simplest to implement and allows for the implementation of minor and major frames by use of separate stacks for each minor frame. The subsystem processor simply reinitializes the stack pointer to the appropriate stack each time the particular minor frame is to begin. An example of the stack method of message list generation is shown in figure 50-18. In the example, the stack pointer indicates (points to) the message address pointers for a particular frame. The message address pointers then indicate the address in common memory where the actual message is to be read from or written to.

   The disadvantage of the stack method is the difficulty of inserting a new message into an existing stack. A typical application would be to insert an error recovery procedure into the message stream upon detection of an error condition, or to insert an aperiodic message based on an operator input. This would require the subsystem processor to build a new stack with the added message and change the message pointer. When the added message (new frame) was complete, the subsystem would have to reinitialize the stack pointer to the original stack.

   A stacked message list is generated by having the subsystem processor build a list of address pointers in memory accessible by the BC. The stack is initialized by setting the stack pointer to the particular message list for each message sequence (message frame).

b. **Linked lists.** In a linked list architecture, each message points to the next message to be transmitted. An example of a linked list architecture is shown in figure 50-19. This method makes it easy to insert messages into the middle of a particular minor frame's message stream. The BC software replaces the forward pointer of the particular message with the address of the message to be inserted. The last message to be inserted would then point to the next message in the original list.

   A disadvantage of the linked list method is the difficulty of using multiple instances of the same message within the same frame. To accomplish this, multiple copies of the message must be inserted at separate

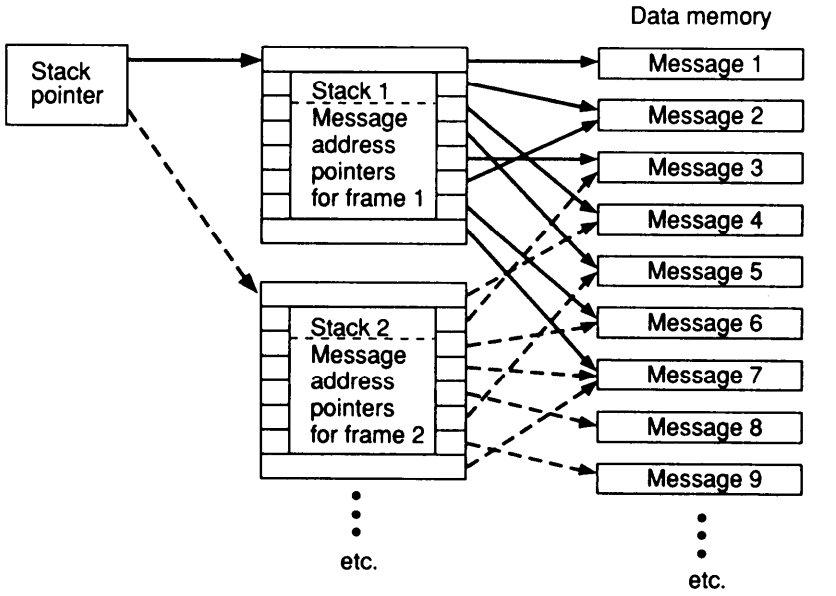


Figure 50-18. Message Stack Architecture

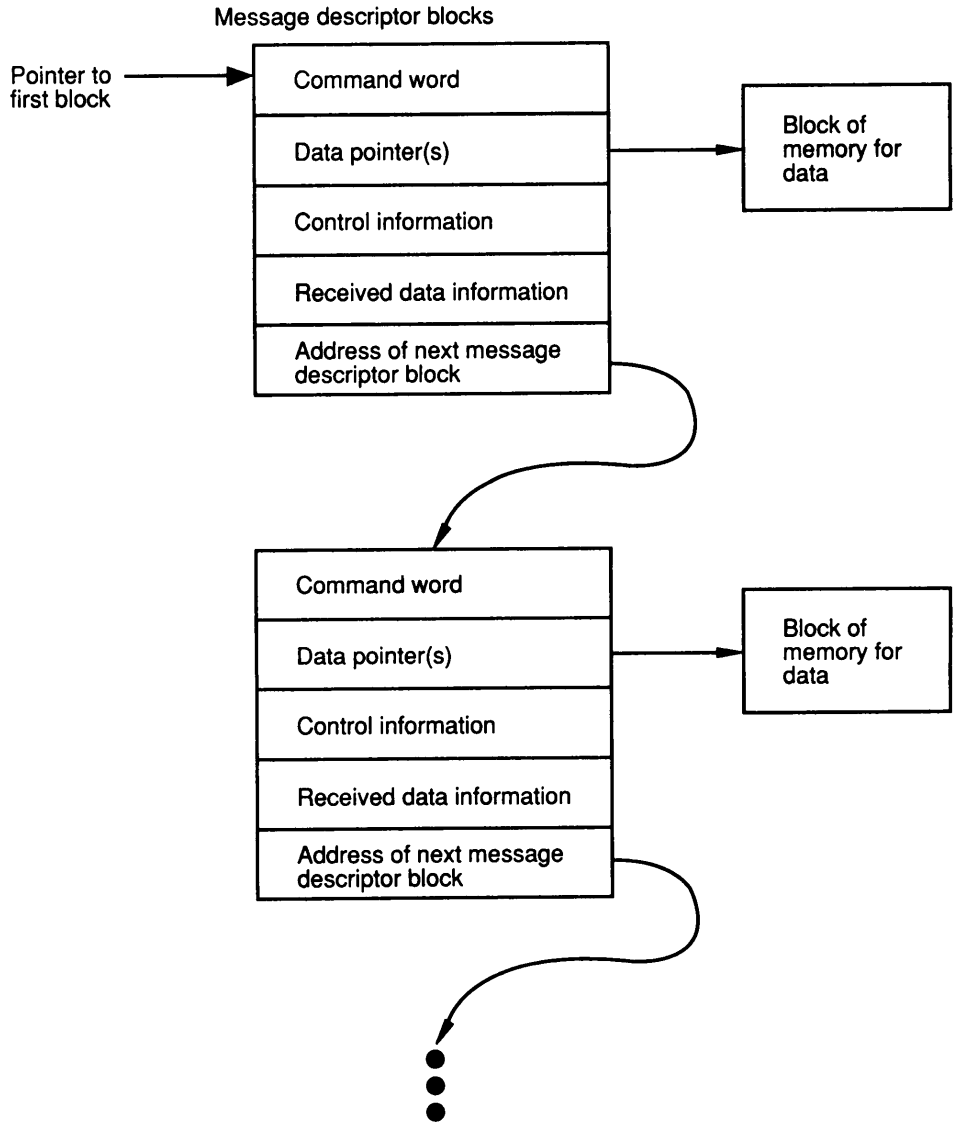


Figure 50-19. Linked List Architecture

memory locations. This requires more memory and more subsystem overhead to maintain the integrity of the messages. The linked list is also more complex to generate. The subsystem software must place the address of the next message in the body of each individual message block. Because these messages may be scattered throughout memory, the possibility for errors will increase.

Data latency. In either case discussed above, the table entry for a message contains a pointer to the RAM address for the data that the BC then DMAs either to or from this address as appropriate. The subsystem must write data into these RAM locations prior to issuing the command to start the message sequence. The subsystem has no knowledge of the time each message accesses these data and, hence, has much less control of data latency for the messages on the bus. Data latency means the age of the data or how long it has been since the data were measured or calculated to the point where they are used. For some data, this is not a problem, but for others it is. Many systems can accept large amounts of data latency as long as the latency is known, but a transaction table scheme typically causes a large uncertainty in the data latency. In a transaction-table-driven system in which data latency is of concern, special provisions must be made for messages with latency requirements.

In time-critical functions (e.g., flight control data), it is often necessary to "time tag" the data such that the subsystem software has an indication of the age of the data. In some applications, the tagging of the data occurs at the source; a tag word is inserted (usually as the first data word) into the message along with the data. The time tag word would be handled by the terminal just like any other data word and passed to the subsystem for processing. Note that this requires that the RT clock be synchronized with a clock in the BC. This is usually accomplished by use of the synchronize mode command.

In other applications, the LRU receiving the data time stamps the data itself using its clock as the tag. This tagging is done either by the BC or, if the BC does not have access to the system clock, by the subsystem processor from within an interrupt service routine. The tag word is then stored either with the data words or in some other defined location.

Asynchronous message insertion. The BC maybe required to send an aperiodic message. This could perhaps be caused by an operator command or by data within a data word. The subsystem processor must modify the current message stream to include this message. Typically, this is accomplished in one of the following ways:

a. Place a message instruction at the bottom of the current message block or the top of the next message block.

b. Insert the message by a special BC instruction as the next message out.

The BC should be able to activate tasks based on events that can occur over the bus. These could include minor cycle synchronization, arrival of a message, and completion of a message. The subsystem processor typically performs this task.

The message arrival or transmission event can usually be signaled by interrupting the subsystem processor. This can usually be controlled by a bit in a BC control register. The processor must determine the cause of the interrupt and then pass control to the proper routine. This routine will then schedule tasks that have been waiting for the event.

50.6.2.3 Message error handling and recovery. The BC is responsible for managing errors on the bus. The BC can usually perform retries of failed messages as discussed in 50.6.2.1; the particular events that cause the retry are usually programmable by the subsystem processor. If the retry procedures fail to achieve a valid transmission, then one of three courses of action is available to the BC:

a. The BC may perform further diagnostic tests, messages, or other recovery functions.

b. There may be a specific error recovery routine (i.e., message block defined for the BC) that will be executed once the subsystem processor has determined the reason for the BC error interrupt.

c. The subsystem processor's bus control software can perform general error management by determining the type of error, type of message, and source and destination of the message.

Many different error management schemes exist based on the system requirements and individual designer's choice. Three examples are given to show the variety of possible error management routines:

a. Delete communication with that RT until the conclusion of the major cycle, at which point a test message (e.g. transmit status word mode command) is sent to the RT to re-establish communications. The results of the test message weighted by some recovery algorithm (e.g., five correct responses in a row) will allow the resumption of communication with the RT.

b. Ignore the failure and proceed. This moves error recovery from the BC to the subsystem software, which will determine if a problem exists that requires additional action. The subsystem software must determine

when the nonarrival of data becomes important and must then do whatever it can to acquire alternate sources of data if any exist. The inclusion of a tag word with each message is valuable in this mode because it allows the subsystem to know the age of the data. The problem encountered in ignoring faults in communication are twofold:

(1) Data may not be gathered about the device failures.

(2) Multiple failures can cause excessive transmission delays.

A variation on this is to perform error retries up to some maximum number. At that point, discontinue retries and finish the transmissions necessary to complete the block of messages in progress.

c. Respond immediately to the failure and initiate simple retry procedures. The BC could command a self-test of the relevant RT or cause a message block to be retried from the beginning. The subsystem would have to decide when a device is faulty and reconfigure the system as necessary to continue operation.

50.6.2.4 Status word analysis. The BC, either internally or in the subsystem software, must analyze each bit in the status word to determine if any extra processing action must be taken. The BC may examine the status word and execute a predetermined action (e.g. an automatic retry or an interrupt of the subsystem).

In systems with terminals designed to different 1553 versions, the BC must know which RT is which version and analyze the status word bits appropriately. For example, because 1553A allowed the message error bit to be set when the status word was returned following message transmissions, that bit must be checked for each 1553A-type transmission. Because of the large inventory of government-furnished equipment (GFE), the mixing of versions may exist for many years.

Error handling may be performed by the BC or in the subsystem processor bus control software. The BC must be responsible, though, for detecting that a message has not been successfully completed. Unsuccessful completion of a message could be due, for example, to a bit error, word count error, Manchester waveform error, or no response to a command. Some typical error conditions and typical recovery actions areas follows:

a. **Message error bit set or no response.** The BC will typically request the RT's status word again (transmit status word mode command) or simply retry the message. The most commonly used procedure is to retry once on the opposite bus before trying the next message in the list. Repetitive retries add to data latency times of critical messages and hence must be carefully thought out. Many variations are available once it has been determined that the retry of the message has failed.

b. **Busy bit set.** A busy condition is normally handled the same as an error (message error bit set or no response). A retry could be quicker than the analysis to determine that the device was busy rather than that an error had occurred.

c. **Service request bit set.** The BC could interrogate the RT to determine the specific service desired (transmit vector word mode command) and present thedatatothe subsystem processor. Alternately, the setting of the service request bit could cause the BC to initiate a predefine action.

d. **Terminal flag or subsystem flag bits set.** These typically indicate faulty equipment and are generally passed on to the subsystem. The terminal address might also be passed to the subsystem so it can identify the faulty terminal. Because the message was received with no errors, the subsystem software could use the subsystem flag bit as one of its validity checks in determining whether to use the data.

e. **Dynamic bus control acceptance or broadcast command received bits set.** These bits are normally passed to the subsystem processor as special conditions.

50.6.3 Backup bus controllers. Often, 1553B system designs include one or more terminals that are normally not BCs but, under defined circumstances, can become the BC on the bus. Such terminals are termed backup bus controllers. The controller in active control of the data bus is referred to as the primary controller. All other terminals capable of assuming control of the data bus are referred to as backup BCs.

MIL-STD-1553B does not go into any detail regarding the level of redundancy required for the bus control function. In a redundant bus system wherein dual (or more) redundant buses are provided to maintain communications in the event of a single-point failure, multiple (backup) BCs might also be desirable.

During the time a backup BC is not the controller, it could be an RT or a bus monitor. Note that a bus monitor is allowed to have an assigned unique terminal address, in which case it in effect acts as both an RT and a bus monitor. The dynamic bus control mode command is provided in 1553B to command an RT with the capability of being a BC to become the BC on the bus to which it is connected. Notices 1 and 2, though, prohibit the use of this mode command for Air Force avionics applications. The reason for this prohibition is the potentially disastrous consequences of an error in the receipt of this mode command or of mistaking another command as this mode command. Note that there is nothing in 1553B that prohibits the transfer of bus control to a backup BC. Only use of the dynamic bus control mode command to cause control of the bus to switch to a new BC is prohibited (in Air Force avionics applications). Alternate schemes to transfer control of the bus by means of separate signals are acceptable.

50.6.3.1 Hot backup BC. A hot backup BC is one that keeps itself continually informed about the state of the system. While the primary BC controls the operation of the data bus, the backup BC may monitor the data bus and the operations of the primary BC to determine if its operations are valid. In the event of a failure in the primary BC, the backup BC should, as a goal, be able to assume control with no interruption in the system's operation and no requirement for reinitialization. To accomplish this, the backup BC must be aware of the system's "state of affairs." This means that the backup BC must know what operational mode each of the terminals is in, what processing state the mission computer is in, what state the man/machine interfaces are in, and so on. In short, it must know what the primary BC knew about the system operation and status.

There are several ways that a hot backup BC can be kept aware of the state of the system. Three options are discussed next.

a. **State variable transfer.** The primary BC can transfer its state variables to the backup BC(s). The backup BC acts as an RT.

   On a continuous cycle, the primary BC transfers to the backup BC the system's state variables, which is the current state of every terminal and function being performed. This transfer usually occurs during normal bus dead time (when all other messages have been transferred). The backup BC acts as an RT, and the state information sent to it in BC-to-RT messages. The number of messages is typically limited to a few per minor frame. The overall number of messages required to complete a single update of the system's state is a function of what data are required to be transferred. This method is usually applied between primary and backup BCs of different designs. Using this method, the backup BC is always up to date (or at the most a few frames old) on the system's status. Use of this method increases bus loading, but as the update rate can spread over several major frames, the loading can be minimized as required.

b. **RT-to-RT message transfers.** All relevant bus traffic can be structured as RT-to-RT messages to which the backup BC listens. The backup BC acts as the receiving RT for the RT-to-RT messages.

   All transmit commands on the data bus occur as RT-to-RT transfers with the receiving terminal being the backup BC. As the BC is allowed to collect all data, this method allows both the primary and backup BC to collect the data at the same time. Receive commands are typically issued as BC-to-RT commands. While the overhead of an additional command and status word (RT-to-RT transfers) will increase bus loading, it will usually be less than that realized using the state variable transfer method. The primary

difference is that the backup BC receives the same raw information as the primary BC and from this can establish its own knowledge of the state of the system. Some system designs implementing this method have used the end of the frame dead time to exchange status between all BCs such that checks can be made on the system's status. This method can also be used as a check on the primary BC's calculations (i.e., a voting system of two or more).

c. Bus monitor. The backup BC can act be a bus monitor and monitor the transactions on the bus.

The backup BC monitors all information on the bus and determines the system state of affairs itself. The standard defines the bus monitor as a "terminal assigned the task of receiving bus traffic and extracting selected information to be used at a later time." Therefore, as long as the backup BC does not act upon the data monitored (i.e., perform internal operations or calculations), but merely uses it to determine the system status, this method is allowable. Depending upon the design of the bus monitor, it may be necessary for the BC to collect all the bus traffic and later filter it within the subsystem. Alternatively, it can collect only selected messages. In either case, this method adds no overhead to the bus loading. This method would also allow the backup BC to check the status of the primary BC because the backup BC collects the same raw information as the primary.

An RT (or bus monitor) must have the capability to be both an RT (or bus monitor) and a BC for it to take over control of the bus. This can be accomplished either by one terminal that is reconfigurable as either type, or by an LRU that includes two separate terminals connected to the same 1553 bus stub in the LRU. In the second case (and potentially in the first case also), it is up to the subsystem to control which terminal in the LRU is active. An RT and a BC absolutely cannot both be active on the same stub at the same time. In both cases, the subsystem must treat the terminal as the proper type of terminal at the proper time. That is, the subsystem must cause the RT terminal to go inactive during the time that the BC is active, and vice versa. The system design must ensure with a high degree of confidence that the previous BC no longer acts to control the bus.

50.6.3.2 Other types of backup BC. A hot backup BC is not the only type of backup BC that can be built. A key characteristic of the hot backup mode of operation is that the backup BC keeps track of the operation of the primary BC and it (the backup BC) decides when it should take over the bus.

All three schemes discussed above require that a backup bus controller is also an RT and/or a bus monitor. A system that is designed with a backup BC that is only a BC would avoid some of the problems mentioned above. There would have to be a separate interface to keep the backup BC updated about the state of the system. Alternately, the system could accept the penalty that the system would have to be reinitialized when switchover occurs. The subsystem would still have to ensure that the BC stays inactive except when it has been commanded to control the bus. The requirement that the previous BC no longer acts to control the bus is the same in either case.

50.6.3.3 Controlling the switchover. Once the decision has been made to switch to a backup BC, the switchover must somehow be accomplished. The switchover can be initiated by the current BC, by the backup BC that is going to become the primary BC, or by some other controller. In any case, the method used must guarantee that there is never more than one BC on the bus at any time.

The dynamic bus control mode command is provided for this purpose. The current BC would send it to the terminal that was to become the new BC. This obviously requires that the current BC be operating properly. That is, that the switchover is not a result of the failure of the current BC. Its use is also prohibited for Air Force avionics applications by Notices 1 and 2.

A backup BC could be designed to require "stay-dormant" messages at some periodic rate. If the current BC did not send the stay-dormant message when required, the backup would assume that the BC was dead and take over the bus. The question becomes, how would the backup BC shutdown the current BC? One way is to shut off its power through an interface with the system power controller.

50.6.4 Controller synchronization. Two or more processors (e.g., the primary and backup BCs) may require knowledge as to what state the system is in or "what time" it is. Additionally, some systems might need more data than can be transferred with the allowed 30 subaddresses. This may require that message subaddress meanings be changed between minor cycles, or some other extended addressing scheme be employed.

System state information or minor frame timing is typically passed using the synchronize mode command. Synchronization is a method of signaling each processor that a defined event is occurring. Receipt of this mode command could cause the reset of an internal clock, either to zero or to the value contained within the data word (synchronize with data). Perhaps it could cause the subaddress memory map to change to the version indicated by the data word. It could also indicate that the previous set of transmissions have been completed. This would allow tasks to begin processing on a complete set of data that arrived during the last minor cycle. This function is completely application dependent and is therefore left to the system designer's choice.

In any case, the subsystem processor is typically responsible for performing some function (e.g., reset of a clock or changing an address pointer for a command block) upon detection of the synchronize mode command.

50.6.5 Notice 1 and Notice 2 considerations. The additional requirements in 1553B Notice 1 and Notice 2 are discussed in 50.4.4. Those items that affect the design of BCs are discussed further here.

50.6.5.1 Notice 1. Notice 1 applied to all Air Force aircraft internal avionics applications (per section 20 of Notice 1). The requirements therein that affect the design of a BC (as opposed to general requirements) are as follows:

a. BCs are prohibited from issuing certain mode commands (dynamic bus control, inhibit terminal flag bit, override inhibit terminal flag bit, selected transmitter shutdown, and override selected transmitter shutdown). The capability to do so is not prohibited, however, and it is recommended that BCs be designed with the capability of issuing all mode commands.

b. BCs are prohibited from issuing any broadcast commands, although the capability to do so is not prohibited. The terminal address of 11111 (binary) is still reserved for broadcast and may not be used for any other purpose.

c. BCs must be capable of issuing mode commands with both 00000 and 11111 (binary) in the subaddress/mode field. The reason for this is to allow the BC to communicate with RTs that have implemented only one of these choices. In particular, it maybe necessary to use 00000 for some RTs and 11111 for other RTs on the same bus. In this case, the system specification must define which is which.

d. if a BC implements any mode commands, it must implement all the mode commands (except those that are prohibited above). Note that it is still permissible (in Notice 1) for a BC not to implement any mode commands. This is not recommended for new design, however.

50.6.5.2 Notice 2. Notice 2 applies to all dual standby redundant applications for the Army, Navy and Air Force (per section 30.2 of Notice 2). The requirements in Notice 2 that affect the design of a BC (as opposed to general requirements) are as follows:

a. BCs must be capable of issuing mode commands with both 00000 and 11111 (binary) in the subaddress/mode field. A BC may not use 00000 and 11111 to convey different information. The capability to use both is to be used only to communicate with RTs that have limitations in the detection of the mode command indicator (some RTs can only detect one or the other).

b. BCs are required to implement all mode commands, although the dynamic bus control mode command may never be issued in an Air Force application.

c. Broadcast commands are not completely prohibited; broadcast mode commands are permitted. The broadcast terminal address of 11111 (binary) is still reserved for broadcast and may not be used for any other purpose.

Broadcast mode commands can provide great time savings and reduced overhead, particularly in the case of the synchronize mode command. The user must beware of the effects of other broadcast mode commands, however, such as reset remote terminal.

d. BCs must have the capability to issue all defined message formats, including broadcast commands. Previously, these message formats were defined, but any given system could use only those that the system designer desired.

50.6.6 BC design example. The intelligent BC described herein has an extensive set of capabilities and features. It can be set to operate as either a BC or an RT (backup controller) under software control of the subsystem processor. It can also operate in a system in which multiple BCs interface with a single host processor.

Efforts have been made to keep all of the interfaces with the subsystem processor as standard as possible, so no special requirements would be placed upon it. The processor selected for this design example is a MIL-STD-1750 processor with extended memory addressing.

The BC's protocol logic is designed to have sufficient autonomous capabilities to handle bus traffic and error processing with minimal burden on the subsystem processor.

50.6.6.1 General description. Figure 50-20 is a block diagram of the example BC. It is a dual-redundant terminal for transformer-coupled stubs. The subsystem interface is designed for easy connection to a

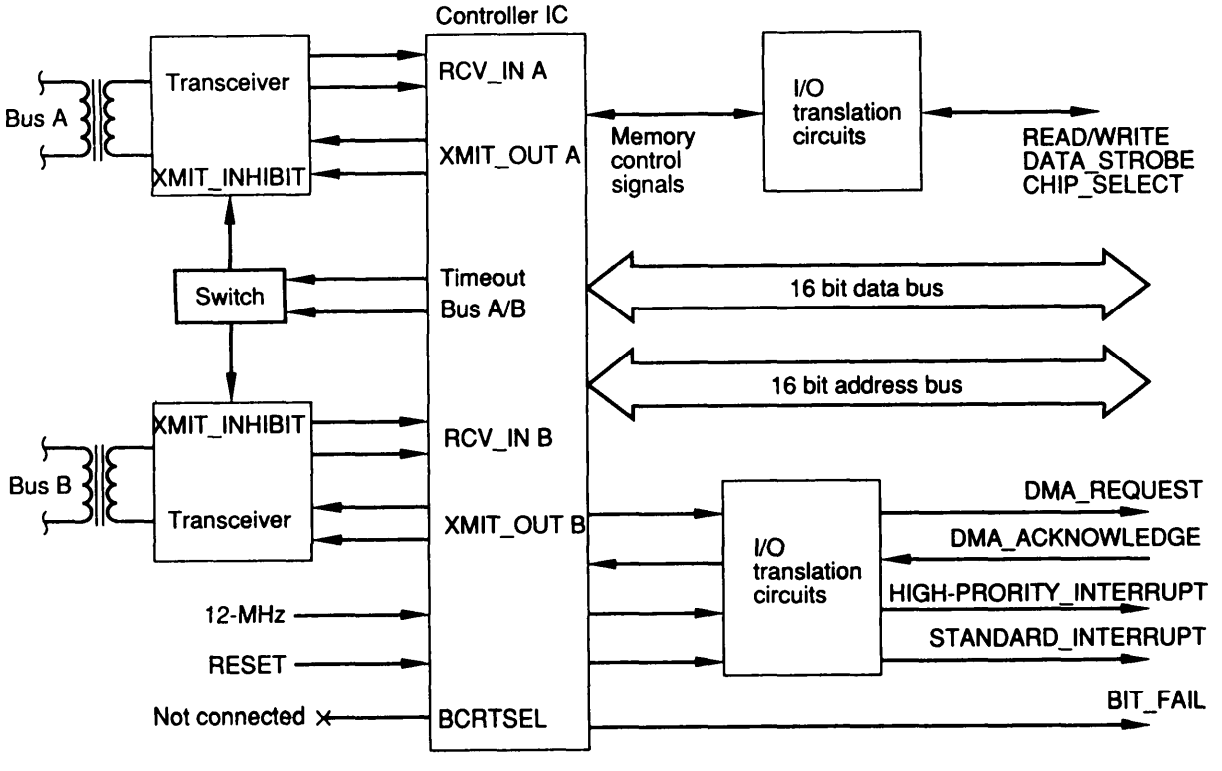


Figure 50-20. Block Diagram of Example BC

microprocessor system. It contains address and data buses, DMA arbitration signals, and two levels of interrupts. The BC also has clock and reset inputs and a fail-safe timer output.

Design of the analog section (transformers and transceivers) was covered in 50.3, which also included two design examples, so nothing further about it is discussed in this section.

Most of the remainder of the terminal is contained in one monolithic CMOS IC. Figure 50-21 is a block diagram of this IC, which was designed for a generalized DMA subsystem interface. Most actual interfaces will require some minor manipulation of the signals. A pulse might have to be lengthened or shortened or changed to a level. Delay might have to be introduced. The logic levels of a signal might have to be reversed (i.e., an inverter added). In short, the detailed timing requirements of the interface signals must be examined carefully and any inconsistencies taken care of.

The design is based on a state machine architecture. It provides automatic message transfers, interrupts to the subsystem processor, and general status information regarding the BC's operation. The subsystem interface is based on a series of registers accessible to both the BC logic and the subsystem processor. Message chaining is accomplished via a linked list scheme. The primary features of this BC areas follows:

a. **Multiple message processing.** The BC autonomously processes any number of messages that may be stored within a 64K memory space.

b. **Automatic intermessage delay.** When programmed by the subsystem processor, the BC can delay a specified time before executing the next message within the sequence.

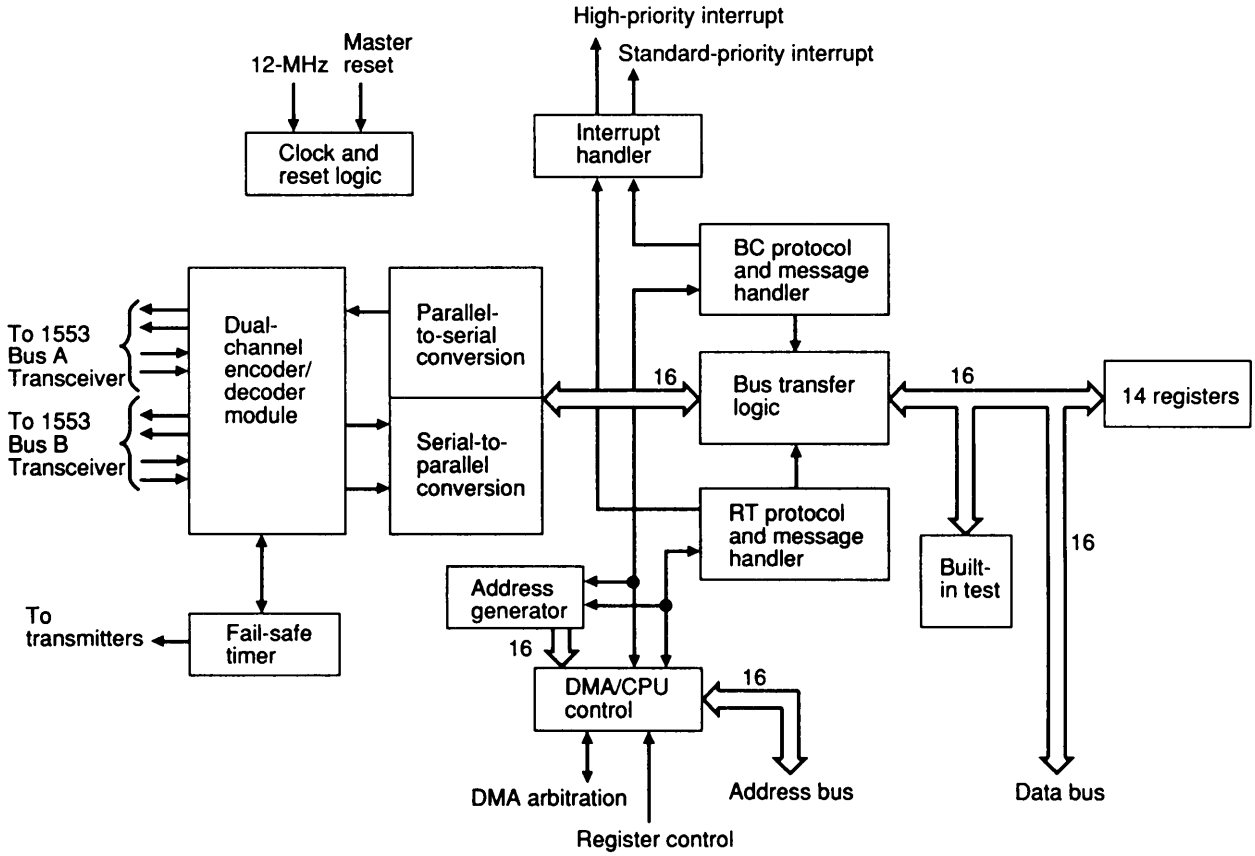


Figure 50-21. BC IC Block Diagram

c. **Automatic polling.** When polling, the BC interrogates the various RTs and compares their status word responses to the contents of a polling compare register. The BC can then interrupt the subsystem if a mismatch in the status word occurs.

d. **Automatic retry.** The BC can automatically retry a message on busy, message error, and response timeout conditions. The BC is capable of retrying up to four times on the same or alternate bus.

e. **Programmable interrupt selection.** The subsystem processor can select various events or conditions to cause an interrupt on one of two interrupt outputs (high and standard priority).

f. **interrupt history list.** The BC provides an interrupt history list that records, in the order of occurrence, the events that caused the interrupts.

g* **Selectable data storage.** Address programmability within the BC provides flexible data placement anywhere within a 64K block of subsystem RAM, making access to it convenient for the subsystem software.

50.6.6.2 Bus interface. The bus interface is two dual-redundant, transformer- coupled stubs.

50.6.6.3 Miscellaneous interfaces. The BC requires a 12-MHz clock of 50% duty cycle. It also requires a reset signal that is held low for a period of time after power is turned on to initialize the hardware.

50.6.6.4 Subsystem interface. The primary interface between the subsystem processor and the BC is shared memory and a series of control and status interface registers. These registers are contained within the BC circuitry. The use of registers for control functions is preferable to common or shared memory locations due to the frequency of access required by the BC. Because the registers are contained within the BC circuitry, the BC has rapid access to them without waiting for DMA to subsystem memory and without tying up the subsystem's internal bus.

Other interfaces include interrupt signals from the BC to the subsystem processor and discrete signals from the subsystem processor to the BC. The latter interfaces are kept to a minimum because they generally require special control or decode logic within the subsystem processor. Initialization and monitoring of the BC's operation is accomplished by using the BC's control and status registers that maybe accessed by the subsystem processor. The BC passes bus message data (data words) to and from shared memory by DMA. Once initialized by the subsystem, the BC uses DMA to read command blocks from shared memory and then executes them. The BC contains circuitry compatible with common subsystem processors' DMA arbitration circuits, making these transfers possible with little or no additional hardware.

BC interface registers. The BC has a set of 14 interface registers (12 of which are used in the BC mode) to control its operations and report status to the subsystem processor. Other functions that these registers serve are address pointers, masks (interrupts, polling compare), and control functions (e.g., BIT start, reset, RT timer reset). Table 50-V lists the registers and their functions. Each register's function is also explained in the following paragraphs.

Table 50-V. BC Interface Registers

Reg	Register function
0	Control
1	Status
2	Current command block
3	Polling compare
4	BIT word (also self-test results)
5	Current command executed
6	Interrupt log list pointer
7	High-priority interrupt enable
8	High-priority interrupt status/reset
9	Standard interrupt enable
11	BIT start command
12	Reset command

To read from or write to a register, the subsystem sets the CHIP_SELECT and DATA_STROBE inputs true and applies the register address on the address bus (only the four LSBs are significant). The subsystem applies or reads the data from the data bus. To the subsystem processor, this appears just like reading or writing to any other memory address.

a. **Control register.** This register is written by the subsystem processor and defines the BC's functional operation. The control register is used to initiate (start) the BC and to define the operational characteristics. Note that some of these characteristics are global in that they apply to all messages. An example is the automatic retry function. While retry can be selected (enabled) on a message-by-message basis from the control block, when performed, it must be the same for all messages (e.g., retry once on the alternate bus). Functions which can be controlled by the control register are:

   (1) Retry on busy, message error, and/or response timeout

   (2) Retry count - number of times to retry.

   (3) Bus select - bus A or bus B.

   (4) Retry on same or alternate bus.

   (5) BC or RT mode.

b. **Status register.** The BC writes to this register to indicate its present status. The status register is used to inform the subsystem processor about the operation of the BC and provide flags about what error conditions might have occurred.

c. **Current command block register.** Written by the BC, it contains the address of the command block (see 50.6.6.5) for the current message.

d. **Polling compare register.** Written by the subsystem, it contains the value of the RTstatus word response that will cause a polling interrupt.

e. **BIT word register.** Written by the BC, it contains BIT results, which are defined and written to by the BC.

f. **Current command register.** Written by the BC, it contains the command currently in progress on the bus.

g. **Interrupt log list pointer register.** Written by the subsystem, this pointer defines the point in memory where the BC writes interrupt information for each interrupt.

h. **High priority interrupt enable register.** Written by the subsystem, the bits in this register define which events shall cause a high-priority interrupt.

i. **High priority interrupt status/reset register.** The BC writes to this register when a high-priority interrupt occurs to indicate the event that caused it.

j. **Standard interrupt enable register.** Written by the subsystem, the bits in this register define which events shall cause a standard priority interrupt.

k. **BIT start command.** Not a register. The subsystem writes to this register address to start the BC's BIT routine.

l. **Reset command.** Not a register. The subsystem writes to this register address to reset the BC.

DMA interface signals. The BC contains DMA interface circuitry to access subsystem memory via DMA. It requests access to the address and data buses by setting DMA_REQUEST true. The subsystem will give this access when it can and will so indicate by setting DMA_ACKNOWLEDGE true. The BC then transfers the words it wants and, when done, releases DMA_REQUEST.

Memory interface signals. The BC and the subsystem interact to control memory in the subsystem (via DMA) and the registers in the BC using the following signals:

a. **READ/WRiTE.** This signal controls whether the access of memory taking place is a read or a write access. It applies both to subsystem memory via DMA and to BC register accesses. If CHIP_SELECT is true, the access is of the BC registers, and if it is false, the access is of the subsystem memory.

b. **DATA_STROBE.** DATA_STROBE controls when the data are actually read or written.

c. CHIP_SELECT. If CHIP_SELECT is true, the BC (as opposed to the subsystem RAM) is selected as the source or destination of the read/write data.

Other subsystem interface signals. There are several other interface signals for the subsystem:

a. **HiGH-PRiORITY_iNTERRUPT.** This signal will go true if any of the programmable events specified in the high-priority interrupt enable register happen.

b. **STANDARD_INTERRUPT.** This signal will go true if any of the programmable events specified in the standard interrupt enable register happen.

c. **BIT_FAIL.** This signal is set true if the BIT test of the BC that was commanded by writing to the BIT start command register has failed.

50.6.6.5 BC architecture. The BC architecture is based on a linked list command block structure and internal programmable registers. Shared memory (up to 64K words) can be used to communicate control information, message data, and status and error information.

Command blocks and message linking. Each message is defined by a command block as shown in figure 50-22. Note that the command block is not a set of registers but is located in shared memory. The command

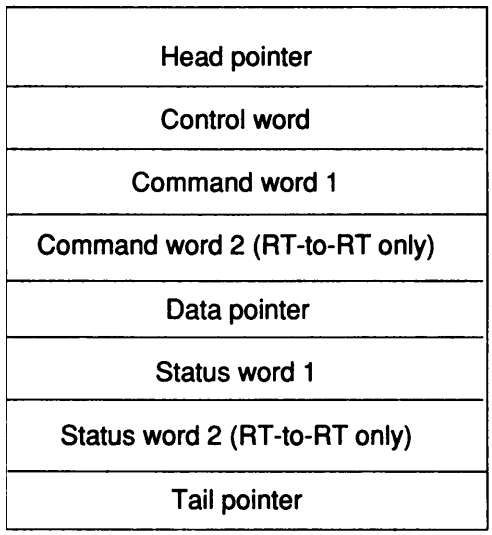


Figure 50-22. Command Block Format

block contains the linking pointers, message control word, message command words, the pointer to the data area in common memory, and locations for the returned status words.

This command block architecture is basically a double-linked list. The chaining methodology is shown in figure 50-23. Note that, in addition to the standard next-message pointer (tail pointer), there is a previous-message pointer (head pointer). This double linking structure links each message block to the previous and successive blocks, and it supports multiple message tasking and scheduling by being able to loop back through a series of messages. The address of the first command block in the linked list is written by the BC into the current command block register before the list of commands is started.

Each command block contains the following:

a. **Head pointer.** This word contains the address of the previous command block.

b. **Control word.** This word is bit programmable and defines the options for the message. Note that bit 15 is written by the BC, but that all the other bits are written by the subsystem. The format is shown in figure 50-24 and is further defined below.

The functions of each bit field in the control word areas follows:

(1) **Message error (bit 15).** This bit is provided by the BC based on the processing of the message. If a message error occurs, then the BC will set this bit.

(2) Skip (bit 14). When set, the BC will skip this message (command block) and execute the next in the chain. This feature allows easy removal or insertion of messages (e.g., very low data rates or aperiodic).

(3) **Interrupt and proceed (bit 13).** When set, the BC will issue a standard interrupt to the host after completion of the message. This bit is used to inform the subsystem processor when a particular message has been processed by the BC.

(4) **Polling enable (bit 12).** Enables a polling operation in which the BC will issue a transmit status word mode command to the designated RTs (those within the command block). On receipt of the status

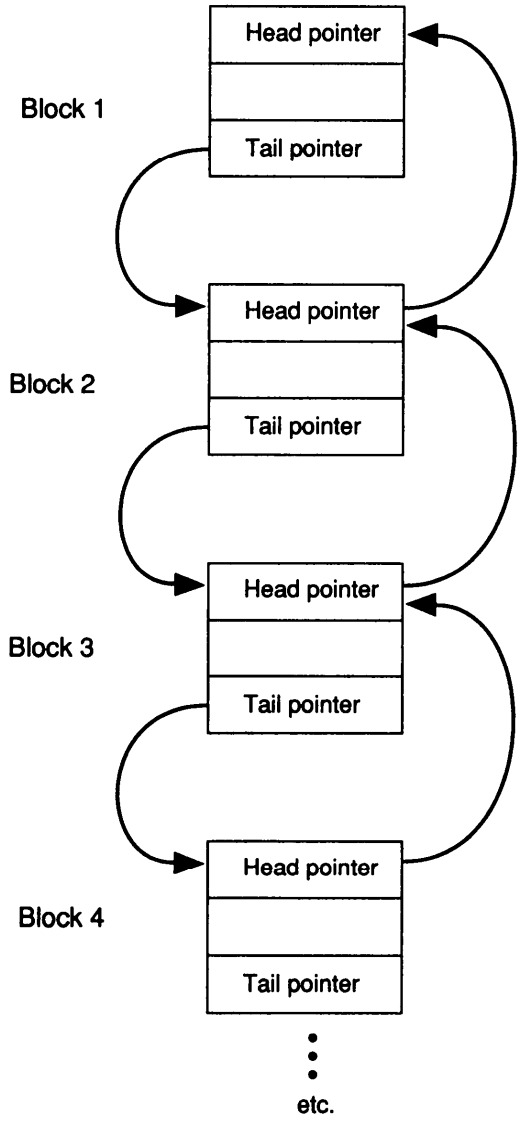


Figure 50-23. Command Block Chaining

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ME	SKP	IAP	PE	ARE	EOL	RRT	MRR	Time delay							

Figure 50-24 Control Word Format

word, if the polling bit is set, the BC will compare the returned status word with the contents of the polling register. If a match if found (e.g., looking for a set service request bit), then the subsystem processor is interrupted.

(5) **Auto retry enable (bit 11).** When set, an automatic retry of the message is performed based on the parameters defined in the control register (what causes a retry, which bus is it done on, how many times).

(6) **End of list (bit 10).** This bit is used to identify the end of the message list. On detection of this bit, the BC will halt its message chaining and issue an interrupt to the subsystem processor.

(7) **RT-to-RT (bit 9).** This bit informs the BC that the message is an RT-to-RT transfer and that it must utilize the second command word and second status word locations within the block.

(8) **Monitor RT-to-RT(bit 8).** When set, the BC will store the data transferred in an RT-to-RT message at the location contained within the data pointer. This allows the BC to selectively collect RT-to-RT data from the bus. If not set, the BC will ignore the data.

(9) **Time delay (bits O-7).** This field identifies a delay between the starts of sequential messages. This is useful in establishing intermessage gaps and minor or major frame timing loops. The delay is enabled by any nonzero value in the field.

c. **Command words.** The first command word entry contains the 1553 command word of the message. For RT-to-RT commands, the second command word entry contains the transmit command of the RT-to-RT command word pair.

d. **Data pointer.** The data pointer contains the address of the starting location in common memory where the BC is to read or write the data.

e. **Status words.** The first status word entry is the location where the BC is to store the status word response from the RT. The second status word entry is required for RT-to-RT transfers and would contain the status word of the receiving RT.

f. **Tail pointer.** The tail pointer contains the address of the next command block within the chain.

Functional operation. The BC offloads the subsystem processor of many of the typical bus control functions. After setting up all of the message blocks and the command blocks, the subsystem initializes the first command block by writing its address to the current command block register. Once set, the subsystem starts the BC by setting the start enable bit within the control register. Once started, the BC maintains the current command block register by updating it as the BC sequences through the command blocks. Interrupts are issued to the subsystem when errors or events that have been selected by bits the standard or high-priority interrupt enable registers occur.

Error and exception processing. The error and exception processing capability of the BC is based on an interrupt structure. The BC architecture allows for programmable events or conditions that will cause an interrupt, selection of interrupt levels (high or standard priority) based on the requirements or conditions, and a history of the interrupts to a user-defined level.

The BC's interrupt structure is based on (1) use of internal registers that enable generation of the interrupt, (2) control bits within the data structures (command blocks) and (3) use of an interrupt log list that will sequentially store a record of interrupt events within common memory.

The interrupt log list allows the subsystem processor to view the standard interrupt occurrences in chronological order. Each entry in the list consists of three words. The first word indicates the type of interrupt

made, the second word contains the command block pointer to the command block in which the interrupt occurred, and the third word is a tail pointer to the next address within the interrupt list.

The BC checks for errors on each message transaction. It compares the terminal address in each RT command word with the terminal address in the responding status word. Error bits within the status word are also tested. Bits within the status word are also compared to the polling register (if enabled). In addition, the BC monitors for response timeout and checks all data words and gaps for proper format in accordance with 1553B. Logic within the BC also checks for illogical commands (e.g., a broadcast command with the T/R bit set to transmit).

All interrupts, whether caused by an error or event, must be handled by software within the subsystem processor. The interrupt condition (flag) is cleared by the subsystem processor writing to the high-priority interrupt status/reset register.

50.6.6.6 Use of this terminal as an RT. The IC controller part that forms the major portion of the BC is also capable of being an RT. Minor modifications of the BC design will allow it to act as an RT instead of a BC. These modifications are detailed below.

There is a pin on the controller IC — BCRTSEL — that controls whether the terminal will act as a BC or an RT. This input is pulled up internally, and is left open (i.e., high) to select BC mode. The BC/RT mode is also selectable by a bit in the control register if desired.

As an RT, the terminal needs a terminal address. There are six pins on the controller IC to load the terminal address, five for the terminal address itself and one for parity. These pins load the terminal address at power-up or when the terminal is reset. Each pin is connected to ground for logic O and left disconnected for logic 1. There is also a terminal address register (register 10) that was not mentioned above. It can be loaded by the subsystem to define the RT terminal address. The subsystem can also read this register to verify the externally loaded terminal address. The rest of the bits in this register control the RT's mode of operation. The busy, service request, terminal flag, and subsystem flag status word bits can beset. The dynamic bus control mode command can be disabled.

Register 13 is another register that was not described above. It is the RT timer reset command which uses this register address. Writing to this register address clears the time tag timer. This is an eight-bit timer with 64-µs resolution; consequently, it cycles in 16 ms.

Register 2, which holds the command block pointer in the BC mode, holds an RT subaddress descriptor pointer when in RT mode. This pointer refers to [(2 • 32)+16]*4 = 320 words in memory (four words for each transmit and each receive subaddress and for each pair [transmit and receive] of mode codes). These words in memory describe where the data are stored, which subaddresses are to be considered illegal, which subaddresses are illegal just for broadcast messages, and if the subsystem is to be interrupted on receipt of a message to this subaddress. There is also a message status word that is stored for each message that includes the time tag, the word count, and a validity flag.

In operation, the RT processes valid commands it receives on the bus, exchanges the data with the subsystem memory locations defined in the RT subaddress descriptor block, and writes the message status word in the defined location in subsystem memory. If the proper bit in the RT subaddress descriptor is set, an interrupt is issued to the subsystem; otherwise, nothing further is done.

50.6.6.7 Design example summary. The BC presented in this example provides a great deal of flexibility and programmability that, in turn, offloads much of the bus control function from the subsystem processor. Its design does assume that it is operating with a processor in the subsystem. It requires a good deal of initialization from the subsystem, but it then operates autonomously.

50.7 BUS MONITOR OPERATION. The design of a bus monitor is quite similar to that of an RT. In fact, a bus monitor is essentially an RT that does not respond to any commands. The only real difference is that a bus monitor accepts messages with many terminal addresses. A slightly more complex bus monitor might accept commands whose terminal addresses match a defined subset (more than one) of all terminal addresses. Most of the information presented previously about RTs is thus applicable to bus monitors.

Typically, a bus monitor is used for instrumentation only. In fact, the only two circumstances in which a bus monitor may be used are defined in 1553B (4.4.4) as: "off-line applications (e.g., flight test recording, maintenance recording, or mission analysis) or to provide the back-up bus controller sufficient information to take over as the bus controller." This is in keeping with the basic design philosophy of 1553B in which there is a confirmation of the receipt of all messages. (Note: broadcast messages are the only other exception to this philosophy.) It is therefore prohibited to use a bus monitor in a system to simplify the transfer of data to multiple terminals in one LRU.

50.7.1 Bus monitor with an RT. Per 1553B (4.4.4), a bus monitor may also have an assigned terminal address. If so, the bus monitor must act as if it were an RT to commands containing this terminal address. Stated in another way, a bus monitor with an assigned terminal address would bean RT as well as a bus monitor. A bus monitor would typically have an assigned terminal address so that the bus controller on the bus would be able to control the operation of the bus monitor and the subsystem to which it is attached (e.g., a bus data recorder). This function is typically used for testing (self-test or production/acceptance tests), status polling of the bus monitor, or reprogramming of the bus monitor's functions. The bus monitor might also be programmable via commands over the 1553 bus as to what messages and/or data it monitors and collects.

The requirement in Notice 2 that terminal address inputs be checked for single-bit errors would not normally apply to bus monitors. In cases where the bus monitor has an assigned terminal address, though, the bus monitor effectively contains an RT. The terminal address of this RT must meet this requirement.

50.7.2 Bus Monitor types. There are basically three types of bus monitors. These are: a) the "collects all" monitor, b) the selective monitor, and c) the hot backup monitor. The first two types are used for the collection of data for off-line use. The third type is used in conjunction with a backup bus controller. Since a backup BC is allowed to be a bus monitor, it can use the bus monitor function to collect data so that it maintains its own record of the state of the system. It can thus more efficiently takeover the BC function when needed. Further discussion of the use of a bus monitor as a hot backup BC is presented in 50.6.3.1.

50.7.3 **Collection of data for off-line use.** As indicated above, a prime use of a bus monitor is to collect data for off-line applications. Typically, a bus monitor has been used for data collection during system integration and flight tests. More recently, bus monitors have been applied as parts of maintenance monitors and flight data recorders (e.g., crash recorders).

Note that 1553 does not define how much or what information the bus monitor must extract from the data bus. The system designer must therefore specify what data needs to be collected which in turn will define what the bus monitor must do.

A 'collects all" monitor is fairly simple. The bus monitor collects and stores whatever words (data, command, or status) appear on the bus.

A selective monitor may be programmed to collect only messages addressed to particular terminals, to collect data for particular subaddresses within a terminal, or to collect certain predefine pieces of data which may appear in any message. Selective monitors typically use a look-up table to determine if the data received are to be stored. This look-up table maybe permanent (e.g., in PROM) or programmable (e.g., in RAM). Some programmable bus monitors are capable of receiving their look-up tables via messages over the 1553 bus to an embedded RT within the bus monitor. In some systems, a bus monitor may even be dynamically programmed as a function of the system's status and operation.

In either a 'collects all" or a selective monitor, the data may be stored in memory (either in the bus monitor or in the subsystem), output to an external mass storage device (e.g., a tape recorder), or output to a telemetry transmitter.

50.7.4 Bus monitor design considerations. There are several other design decisions that the designer must make. Does all the data collected need to be stored? Are the command and status words needed or only the data words? Is there a requirement or necessity to store a tag with the data to indicate possible error conditions, which bus it was received on, or timing information?

Regardless of the type of bus monitor used, the bus monitor designer must pay close attention to three areas. These areas are: a) the amount of data to be collected, b) the timing of the data, and c) error conditions on the 1553 bus.

a. The amount of data to be collected will affect the amount of memory needed, either for permanent storage or as a temporary buffer. The rate at which these data are acquired will affect the required speed of the subsystem interface (e.g., a tape recorder or telemetry encoder). The slower the subsystem interface, the more internal buffer memory may be required. For systems with large amounts of data to store, the designer may wish to consider the use of data compression techniques to reduce the amount of memory or transfer time required. For intelligent bus monitors, the ability to store only abnormal data (e.g., data that are outside a range or a tolerance) may also reduce the amount of data to be stored.

b. Timing information about the monitored data is necessary to reconstruct the bus traffic. Due to the asynchronous nature of the 1553 data bus and the variation of response times and intermessage gaps, it maybe necessary for the bus monitor to time tag each message. The resolution and accuracy of the clock used in tagging the data is left to the bus monitor designer. The various U.S. military test ranges have established standards for aircraft instrumentation and telemetry. This group, called the Inter-Range Instrumentation Group (IRIG), has established a time base for all range data. This IRIG time base provides a 24 hour clock with resolution to 10 microseconds. The use of this time, however, requires a 40 bit clock within the bus monitor for tagging of the data.

c. The designer must decide what the bus monitor is to do about error conditions. Collecting and identifying data is relatively straightforward as long as there are no errors. The bus monitor should be able to differentiate between command words and status words (assuming the instrumentation bit is not used). An intelligent bus monitor could do this by being aware of and following the messages on the bus. It could expect or anticipate responses to command words and measure the intermessage-gap and response times in order to follow the message flow. The bus monitor, by following the message protocol, maybe able to differentiate between word types, determine error conditions, and identify timing problems. The bus monitor's handling of invalid or illegal messages must also be defined. Indicators for these conditions may be stored with the data for error analysis later. Examples of possible bus monitor options, not mutually exclusive, are:

(1) Process only valid, legal messages, just as if the bus monitor were an RT.

(2) Also store the data from illegal messages. This could only apply if the bus monitor were given enough information to know which messages are illegal for each RT.

(3) Also store as much data as possible from invalid messages, along with an indication that the message is invalid.

(4) For invalid messages, store only an indication that an error occurred in the message but not the message itself.

(5) For invalid messages, store only an indication of an error along with data indicating the type of error.

(6) Store time tag information along with all messages.

In particular, it is recommended that a bus monitor be designed not to store invalid or partial messages without any indication of an error. To do so forces the user of the data to analyze the messages to detect if message information is complete and consistent. Without sufficient timing or message protocol information, this analysis is frequently very difficult.

50.7.5 Bus monitor summary. Regardless of the type of bus monitor, its design is very similar to that of an RT. The analog front end and decoder sections should be identical, and the use of off-the-shelf components is easily accomplished. The design of the protocol control unit section and the subsystem interface are dependent upon the bus monitor's capabilities and intelligence. The subsystem interface is typically affected by the speed of the subsystem, which could be a bulk tape recorder, mass memory device, or telemetry encoder. The bus monitor designer needs to address the issues brought forward in this section and apply tradeoffs against the system requirements to determine the bus monitor's operational requirements.

50.8 COMPATIBILITY AMONG 1553 VERSIONS. There are terminals in use today that were designed to various versions of 1553: 1553A (although there are fewer of these than there used to be), 1553B, 1553B with Notice 1, and 1553B with Notice 2. The differences in the standard are discussed in detail in section 90 and earlier in this section (see 50.4.4), where the requirements for implementing them also were discussed.

This paragraph discusses how terminals designed to later versions of 1553 (most commonly, today, to 1553B Notice 2) operate with other terminals that were designed to an earlier version.

For the most part, terminals designed to meet the requirements of the various versions of 1553 will function properly together. Most of the requirements in Notices 1 and 2 of 1553B are additional restrictions and not really changes to requirements that previously existed in 1553B. Many of them simply make mandatory certain things that were permitted but optional in 1553B. Thus, a terminal that meets the requirements of Notice 2 will also meet the requirements of the basic 1553B. 1553A, however, included some requirements that make it more difficult to use 1553A terminals in current systems.

1553A allowed use of most status word bits and mode commands in any manner desired by the system designer. This creates obvious problems with newer terminals that use these functions in the manner defined in 1553B. These problems can only be resolved on a case-by-case basis, and there isn't much that can be done in the design of a terminal except to not implement any of the conflicting functions.

In addition to the non-uniformity of the status word bits, 1553A also required that the status word retransmitted for all non-broadcast messages. This included messages in which an error condition was detected by the terminal. 1553B bus controllers operating with 1553A terminals must therefore examine the status word returned by the 1553A terminal(s) to determine if an error existed instead of using the lack or suppression of the status word for this determination.

RTs designed to 1553A respond faster to commands (on the average) than 1553B RTs. This should create no problems, and the minimum response time did not change. Note that, even though the minimum response time is given as 2.0 µs in 1553A and 4.0 µs in 1553B, the difference is in the method of specifying the time, so these two specifications are equivalent.

In the case of a 1553A BC operating with a 1553B RT, there is **a** conflict. The 1553A BC expects a response before 7.0 µs (measured in the manner specified in 1553B), and the 1553B RT is not required to respond before 12.0 µs. The obvious design solution in a newly designed RT is to make it respond in 7.0 µs or less. This is not easy, however, because most of the available VLSI ICS for RTs do not respond this quickly. To meet this requirement, parts have to be selected carefully or the response time shortened by some means. Some chip sets allow shorter response times by eliminating the check they would normally do for another (extra) word following the transmission from the BC. It is also possible that the design of the 1553A BC will

allow 12.O-µs response times, as there is no requirement in 1553A (or 1553B either, for that matter) that a BC invalidate the response at any particular time. Alternately, it could be possible to modify the 1553A BC to allow this longer response time. In this case, there will be no operational problems.

There are differences in terminal analog characteristics between 1553A and 1553B requirements. A 1553A terminal for transformer-coupled stubs is designed for transformers with a turns ratio of 1:1, not 1.4:1 as in 1553B. It must be connected to the 1553 bus with a transformer of the proper turns ratio. If this is done, most of the differences in its analog characteristics will not disturb the system. These differences are:

a. The output voltage of a 1553A terminal can be as high as 20 V_{p-p} as measured on the bus, as opposed to 1553B which allows a maximum of 9 V_{p-p} Most 1553A terminals don't have such a high output, and most 1553B terminals can withstand this voltage on their inputs. This issue needs to be evaluated for the actual voltages produced by the particular 1553A terminals involved.

b. 1553A terminals for transformer-coupled stubs do not accept input voltages quite as low as those for a 1553B terminal (1.0 V_{p-p} versus 0.86 V_{p-p}). Because voltages this low seldom occur in an actual system, this is usually not a problem. For direct-coupled stubs, the 1553B limit of 1.2 V_{p-p} is higher and thus no problem.

c. The input impedance of a 1553A terminal for transformer-coupled stubs is higher than a 1553B terminal (2000 ohms versus 1000 ohms). This should cause no problems.

Acroynms and Abbreviations

BC	bus controller
BIT	built-in-test
DMA	direct memory Access
FIFO	first in first out (type of memory)
GFE	government furnished equipment
IC	integrated circuit
I/0	input/output
IRIG	inter-range intrumentation group
j	square root of -1; indicates imaginary part of number
LRU	line replaceable unit (i.e., a box of electronics)
LSB	least significant bit (or byte)
MS	milliseconds
MSB	most significant bit (or byte)
NS	nanoseconds
PROM	programmable read only memory
RAM	random access memory
RT	remote terminal
SA	subaddress (field in 1553B command word)
T/R	transmit/receive (bit in the 1553B command word)
US	microseconds
VLSI	very large scale integrated (applies to ICs)
WC	word count (field in 1553B command word)

SECTION 50 INDEX

SECTION 60

SYSTEM DESIGN

CONTENTS

FIGURES

TABLES

60. MULTIPLEX SYSTEM DESIGN

The emphasis in this section is on the system thinking and perspective required to design a complete multiplex system. Refer to MI MIL-STD-499, 'Engineering Management," and other textbooks for details on system engineering practice. The topics covered in this section are directly related to MIL-STD-1553B (referred to as 1553B) multiplexing. Some of the topics cover nonmultiplexed areas of the system where they relate to the integration of the multiplex system into the overall system. Many topics of multiplex system engineering are not in this section (e.g., multiplex subsystem hardware selection and mission performance analyses relating to accuracy and capability). Therefore, some general prerequisite knowledge is needed to put each of the topics in a multiplex system engineering perspective. Generally, this prerequisite knowledge falls into the areas of:

a. General knowledge of military electronic subsystems (sensors, displays, computers).

b. General knowledge of system engineering and system integration activities as practiced by the Air Force, Navy, Army, and integration contractors.

Particular detailed knowledge of electronic subsystem characteristics (e.g., range, accuracy, and use) is not a prerequisite for this section.

Multiplex system design is the process of designing and implementing a multiplex system architecture. The term "system architecture" as used here includes the externally visible parts of a multiplex system, the internal partitioning of multiplex interfacing elements, and the hardware and software used for data transport and transport control.

Multiplex system architecture consists of two major parts: system topology and system control. System topology is the physical arrangement of data buses and units attached to the data buses. System control implements the protocol required for data transfers; the rules used in achieving media control; and the procedures for initialization or startup, normal data bus operations (e.g., time synchronization, data security, and data integrity), abnormal bus operations (e.g., fault handling and recovery, error handling and recovery, and redundancy management), and system shutdown.

This section begins with discussions of the three topics most directly concerned with multiplex system design:

a. Multiplex system topology (60.1)—Multiplex system physical arrangement design considerations.

b. Multiplex system engineering (60.2)—System design process and integration considerations, providing a basis for the discussion of multiplex system control.

c. Multiplex system control (60.3)-System control design considerations.

These three topics are followed by discussions of:

a. System growth provisions (60.4).

b. System validation tests and test equipment (60.5).

c. Integration incompatibilities among subsystems (60.6).

d. Summary of integration activities related to the normal defense system acquisition process (60.7).

60.1 MULTIPLEX SYSTEM TOPOLOGY. Multiplex system topology is the network of data bus terminals, the components that comprise the data bus, and the physical arrangement of redundant elements (whether terminals and bus controllers; or bus cables, couplers, and terminators). It includes all terminals and data

buses involved in integrating the data buses into the vehicle. Data buses and topologies can be categorized by: (1) their data bus redundancy and stub coupling, (2) the number of data buses-single or multiple, and (3) for those using multiple data buses, by the control and data passing relationships among the data buses.

60.1.1 Data bus redundancy and stub coupling. A MIL-STD-1553 data bus cable is a twisted, shielded wire pair used to transmit and receive a differential signal. Data buses can be categorized by level of cabling redundancy, redundancy implementation technique, and stub-to-bus coupling technique.

60.1.1.1 Cabling redundancy. Data bus cabling can be a single, twisted, shielded pair cable offering no redundancy or it can be multiple cables used redundantly. At this time, we are describing the data path among a group of terminals where all the terminals are connected to each data bus cable. Figure 60-1 is a block diagram that shows how single and multiple cables could be connected in a sample multiplex data bus arrangement.

Data bus implementations using single cables are rare. Typically, where single cables are used, more complex system control is required. System control should detect, isolate, and recover from errors and faults to maintain communication with a maximum number of bus terminals during a mission.

60.1.1.2 Data bus redundance implementation. Data bus redundancy implementation techniques in common use are: standby redundancy (required when two cables are used in a dual-redundant bus configuration) and active redundancy (three or more cables used in a multiple active configuration). Standby redundancy is a technique where one cable is used for transmitting and receiving and one or more other cables are ready to become the active cable. Note that which cable is active can change each transmission. Several pairs of cables maybe used as multiple standby-redundant data buses. In a multiple active configuration, transmission of data can occur simultaneously over all cables.

Dual-standby redundancy is the most widely used and recommended redundancy technique for multiplex systems. MIL-STD-1553B, paragraph 4.6.3, requires that, if a dual-redundant data bus is used, then it shall be a dual standby-redundant data bus. This redundancy level and implementation technique provide adequate redundancy for dispatch-essential (mission-essential) multiplex systems at reasonable interfacing cost. Systems such as flight controls, which require higher levels of redundancy for flight-

critical reliability or mission success or which require that multiple copies of data be sent in parallel and compared or voted on, typically use multiple-active bus configurations. MIL-STD-1553 protocol will support multiple-active configurations. Hardware is available to build such a configuration.

Systems using higher than dual-redundant 1553 interfaces, and systems using 1553 for flight-critical applications, are early in their development stages. Information is not available to describe these systems or to provide any useful guidance because of the infancy of these applications and the closed nature of the programs.

60.1.1.3 Stub coupling. The standard defines two techniques for coupling stubs to the data bus: direct coupling and transformer coupling. Transformer coupling is the most widely used stub coupling method. For pros and cons of these stubbing methods, refer to section 40 of this handbook and to 10.5 of 1553B. Direct coupling is only suitable for very short stubs, generally less than 1 ft long. Transformer-coupled stubs are generally acceptable up to 20 ft long. Air Force and Army applications of 1553B Notice 2 require transformer coupling. Navy applications allow either direct or transformer coupling. Electronics can be built that support both coupling methods. This achieves the widest possible use. Be warned that all buses and stubs are transmission lines. Section 40 discusses the potential problems of reflection and distortion on the buses and stubs. A bus network mockup should be built and bus performance verified.

60.1.2 Topology categories. Generally, topologies can be categorized as a “single-bus topology” or a “multiple-bus topology”

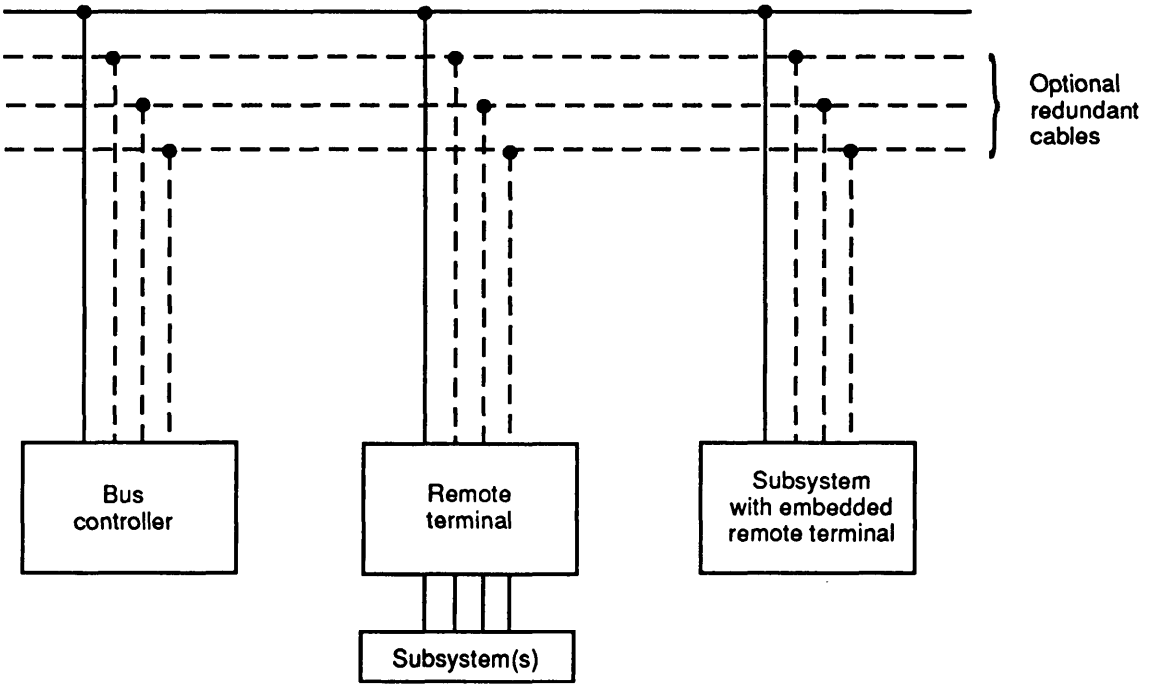


Figure 60-1. Sample Multiplex Data Bus Architecture

60.1.2.1 Single-bus topologies. A single-bus topology is the simplest. An example is the AH-64A multiplex system topology (figure 60-2). The redundancy requirements of a particular application may require a "single-bus topology" to be implemented using redundant bus cables.

The following are characteristics of the AH-64A multiplex topology:

a. Single-bus topology.

b. Dual data bus cables.

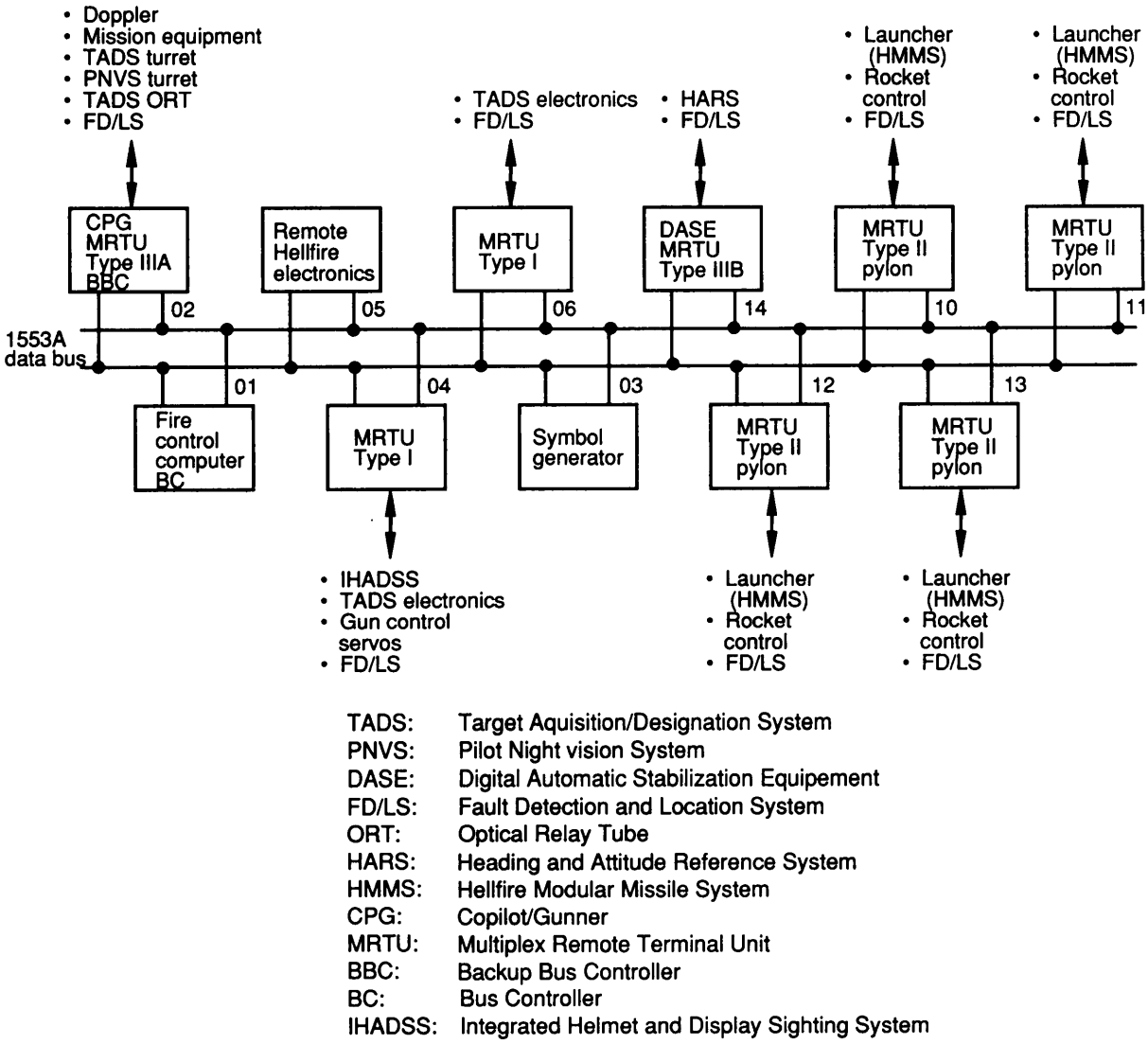
c. Standby cable for redundancy.

d. Transformer-coupled stubs (per MIL-STD-1553A).

Bus control and redundancy management mechanization affect topology in the areas of: redundant terminal location, redundant bus controller (BC) location, and redundant bus cable and stub routing. The BC is conventional and is located in the fire control computer. The backup BC, however, is unusual. It is located in a unit with the copilot or gunner remote terminal (RT). The backup BC and the RT are functionally isolated but share the same analog front end. The backup BC monitors bus activity and uses the lack of activity as one criterion indicating it must assume bus control. The backup BC provides reduced system capabilities when compared to the fire control computer.

60.1.2.2 Multiple-bus topologies. The multiple-bus topology is an expansion of the single-bus topology and has two basic forms:

a. Parallel bus topologies consisting of multiple buses with equivalent levels of control.



TADS:	Target Aquisition/Designation System
PNVS:	Pilot Night vision System
DASE:	Digital Automatic Stabilization Equipement
FD/LS:	Fault Detection and Location System
ORT:	Optical Relay Tube
HARS:	Heading and Attitude Reference System
HMMS:	Hellfire Modular Missile System
CPG:	Copilot/Gunner
MRTU:	Multiplex Remote Terminal Unit
BBC:	Backup Bus Controller
BC:	Bus Controller
IHADSS:	Integrated Helmet and Display Sighting System

Figure 60-2. AH-64A Multiplex System Block Diagram

b. Hierarchical bus topologies consisting of multiple buses with hierarchical levels of control. Most hierarchical topologies are hybrids consisting of parallel buses with the same level of control and hierarchical buses above or below the parallel buses.

Parallel-bus topologies. The multiple-bus topology with equivalent (parallel) levels of control is exemplified by a weapon system that uses multiple single-bus topologies for different functions. The B-1B offensive avionics system central computing complex is an example of parallel topology (see figure 60-3). There are four buses in the central computing complex, each a dual standby-redundant bus. They are: the guidance and navigation bus (A-bus), the weapon delivery bus (B-bus), the control and display bus (C-bus), and the critical resources bus (D-bus). The buses operate independently. Each data bus has its own BC. The guidance and navigation avionics control unit (GNACU), the weapon delivery ACU (WDACU), the control and display ACU (CDACU), and the critical resources ACU (CRACU) are BCs on the A, B, C, and D buses, respectively.

A unique feature is the backup BC. The CRACU is a spare processor that is also the backup BC for all three of the other BCs. It can functionally replace anyone of the other three processors when loaded with the correct

software. It is therefore a "pooled" spare processor. The CRACU receives state data (checkpoint data) over the bus on a continuous basis.

The trend toward multiple bus topologies within a vehicle or in a large subsystem integration is a natural evolution of the single-bus topology.

Hierarchical-bus topologies. A second form of multiple-bus topology occurs when one or more single-bus topologies are integrated with another single-bus topology where the buses have a control relationship. The bus relationship may be expressed as follows:

a. Local buses—subordinate (under submission to global).

b. Global bus—superior (control over local buses).

The primary distinction in control is based on functional use and not on the interconnection of the terminals. Therefore, data bus topologies can be identified or defined on the basis of interconnection requirements of the user terminals. These requirements also establish the interconnection of a sensor to a local or a global bus.

The path for growth in multiplex systems leads a system to evolve from a single-bus system to either a parallel- or a hierarchical-bus system.

Hierarchical topologies can be designed with each function (e.g., weapons delivery) having its own data bus and all the functions exchanging data over one or many global buses. This type of architecture provides isolation between functions. An approximately equal level of redundancy can be designed for the data buses, the functions, and the subsystems to meet mission and performance requirements. This fits the way large systems are functionally organized. The data bus topology can be organized to match the redundancy level of subsystems and functions. Data buses can be dedicated to individual functions for isolation and redundancy. A hypothetical example of such a hierarchical topology is presented in Figure 60-4. Each functional processing unit provides a "gateway" function between the global bus and the local bus. A gateway passes data between two data buses of similar bus type. Each gateway, except the vehicle management gate, is a RT on the global bus and a BC (or RT/backup BC) on the local bus.

The weapon delivery (WD) function in this example implements two data buses below the global bus. The WD bus connects WD processing to weapon interface units (WIU). The WIUs are gateways between the WD bus and local stores buses. The WIUs are RTs on the WD bus and they are BCs on stores buses that connect individual weapons to the WIUs. The stores buses are part of a MIL-STD-1760 aircraft and store electrical interconnection system network.

The vehicle management interface on the local bus is a gateway with RTs on both the global and vehicle management system (VMS) buses. The VMS is not hierarchical to (not controlled by) the overall mission system in this example but is parallel to, and functionally isolated from, the mission system. The RT-to-RT gate between the global bus and vehicle management bus performs a data-passing function but not a control-passing function.

60.2 MULTIPLEX SYSTEM ENGINEERING. The electronic system of a military vehicle, which performs functions such as navigation, flight control, and weapon delivery, must be viewed as an integrated system rather than a conglomerate of functional subsystem sensors, controls, and displays. The data bus integration method forces the system engineer to perform system-level analyses because defining information flow is a key element of an orderly integration process. When using the data bus integration method, software controls the real-time information flow to achieve integration.

The system-level analyses include analyzing vehicle electronic system requirements, system partitioning, and integration. Partitioning and integration are classical processes of system analysis and system synthesis.

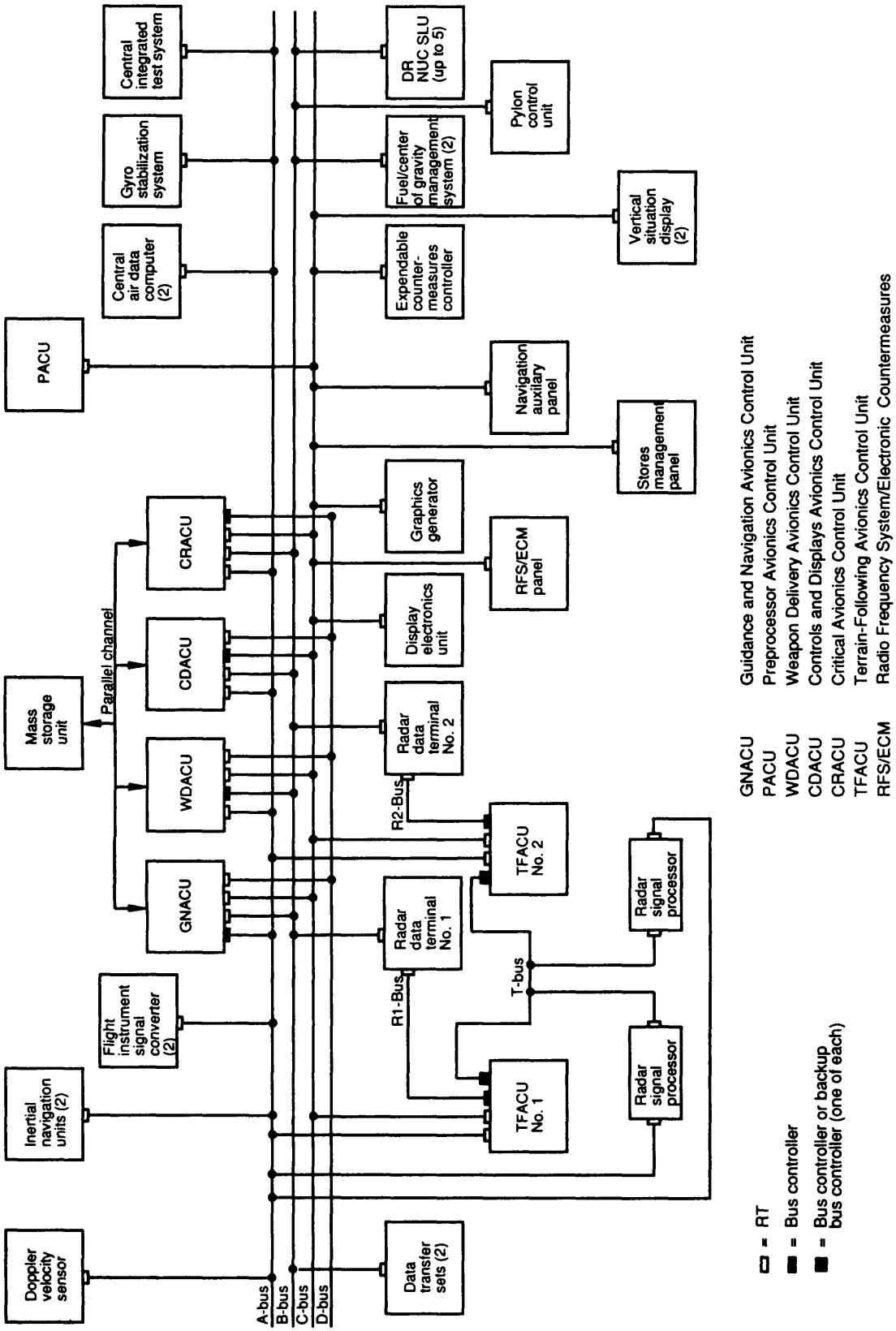


Figure 60-3. B1-B Offensive Avionics System Topology

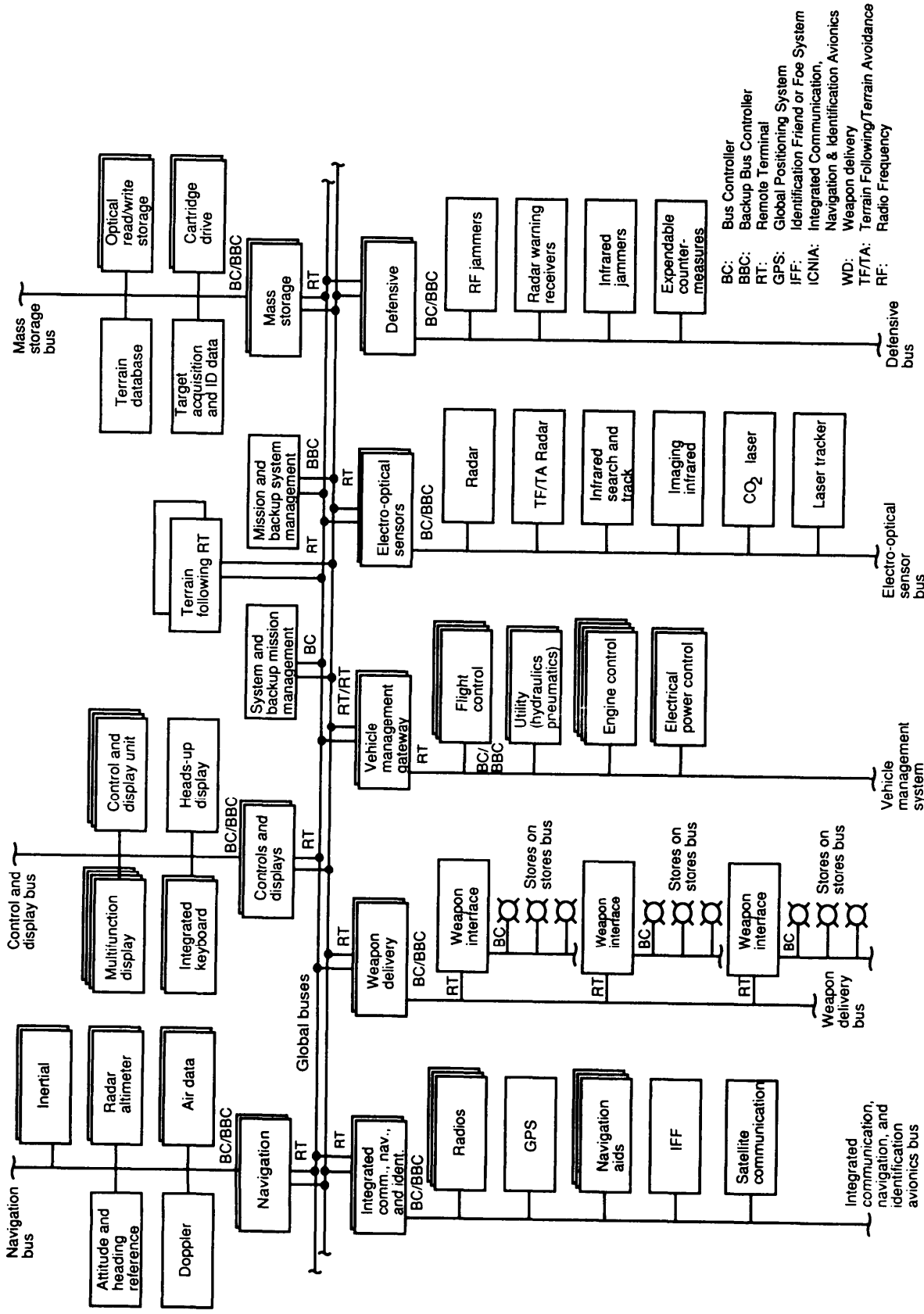


Figure 60-4. Hierarchical Topology Example

The requirements are usually documented in system or segment specifications and become contractual performance requirements.

60.2.1 Multiplex system requirements. Electronic system-level requirements are established from mission scenarios, operational requirements, and program constraints. Typical inputs and constraints for aircraft systems are: mission analyses, flight profiles, aircraft limitations, mission success probabilities, reliability, maintainability, availability, survivability, vulnerability, manning, and physical environment constraints. Program constraints consist of: life-cycle cost, schedule, manpower, interservice use, and required use of existing equipment. These requirements feed into the system partitioning process for validation.

The following basic requirements related to a data bus system should be derived through the system partitioning process, described in 60.2.2, and included in the vehicle segment specification defined by the integration contractor:

a. A requirement stating that MIL-STD-1553B (referred to as 1553B) data buses will be used in the systems integration of vehicle electronic subsystems.

b. System-level redundancy and functional isolation requirements.

c. List of subsystems that will be connected, or interfaced, to the data buses (i.e., inertial navigation systems, fire control systems, crew displays, computers, and communication and identification subsystems).

d. A description of the baseline multiplex topology, including block diagrams of the system arrangement and connecting network.

e. A description of the overall electronic system and data bus system control approach. This includes a description of the RT capabilities required to support the system control concept.

f. Multiplex growth provisions (e.g., number of spare addresses and percent spare bus loading).

60.2.2 Multiplex system partitioning. Multiplex system design begins with a statement of the requirements for electronic system functions that will use 1553B. The overall specification of hardware and software requirements for a multiplex system, including the description of functions, computations, modes, data flows, subsystems, topologies, and system controls, will be derived from examination of functions and data requirements in the areas described in 60.2.2.1 through 60.2.2.7. The steps in the multiplex partitioning flow are summarized in figure 60-5.

60.2.2.1 Analyze mission and performance requirements. The first step in multiplex partitioning flow is to analyze mission and performance requirements and determine the integration method (figure 60-5, item a). Use of multiplexed data buses can potentially reduce the size, weight, and power requirements of electronic systems, as compared to nonintegrated or discrete-wire integrated systems. Multiplexed systems also allow greater sharing of system data resources and ease the addition of new equipment and the control of redundancy. The feasibility of the integration method may be assessed by questions such as:

a. Do preliminary timing and sizing of data transfer requirements indicate that MIL-STD-1553B data buses will perform the required data transfer with adequate growth reserves, typically 30% to 50% of capacity?

b. Are there unique requirements that drive the integration to a fiber optic bus or to a high-speed data bus?

c. Are the integrating subsystems designed with an adequate number of 1553B interface terminals?

60.2.2.2 Derive functional requirements. The second step in multiplex partitioning flow is to derive functional requirements for mission modes (figure 60-5, item b), based on the customer-provided mission and system performance requirements. Then electronic system functional requirements can be defined that meet

each of the mission mode requirements. Functions outside of the electronic system to which it must interface must be defined to understand the meaning of all data.

Before defining how missions can be supported by functions of the electronic system and what particular functions are to be performed during each phase of each mission, it is necessary to determine the complete repertoire of missions. Then, when the missions are known, phases are determined and arranged in groups called mission modes. (Note that these are system or sensor modes and are not related to MIL-STD-1553B mode codes.) For example, the weapon delivery mode of a mission is usually distinguished from the waypoint navigation mode, even though navigation sensors may be used in each, In addition to these normal operational modes, other mission modes that should be considered include system startup and shutdown, error recovery, and degraded system operation.

In defining the electronic system functions for each mission mode, the following should be considered:

a. Data transfers that are unique to a mission mode or common to more than one mission mode.

b. Any unique setup (initialization) conditions.

c. Requirements for time-critical actions or responses.

Thus, a derivation of the functional requirements for each mission mode must include definitions of all of the functions of the electronic system and any external functional dependencies. The result will be functional flow

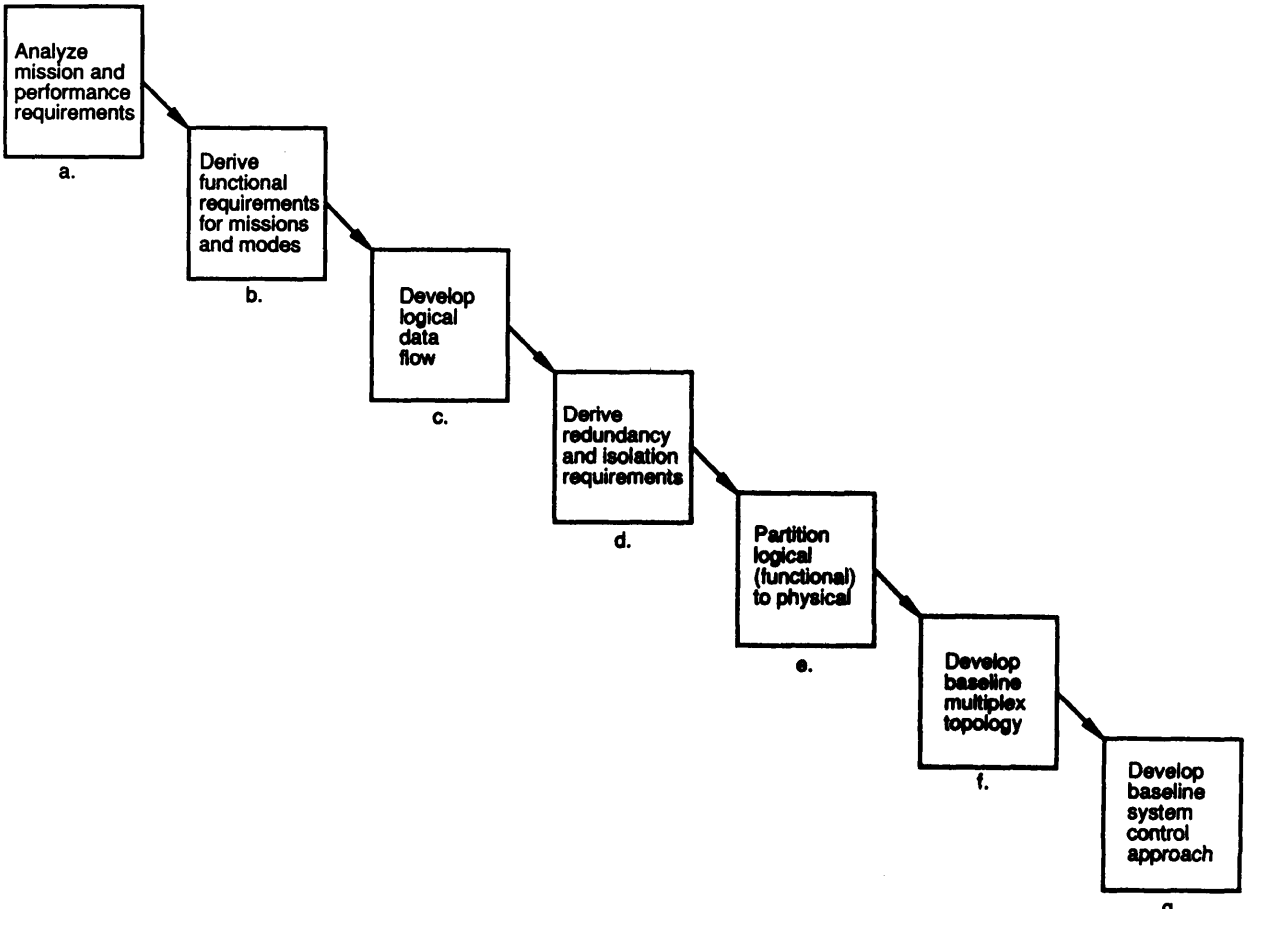


Figure 60-5. Multiplex System Partitioning Process

diagrams that establish the operations to be performed, by mode, and multiplex data traffic requirements (e.g., periodicity and time-critical data and actions).

60.2.2.3 Develop logical data flow. The third step in multiplex partitioning flow is to develop a logical data flow (figure 60-5, item c), including defining its input, processing, and output. This logical data flow must be defined within each function and between the functions involved in each mission mode as defined in 60.2.2.2. A functional schematic and flow diagrams should result from this effort. This effort also defines areas such as multiplex message flows and rates, initial timelines, and initial data packing in messages.

60.2.2.4 **Derive redundancy and functional isolation requirements.** The fourth step in multiplex partitioning flow is to derive redundancy and functional isolation requirements and allocate them to the multiplex system (figure 60-5, item d). The level of redundancy to be required in the system design must be determined. Redundancy is defined as having backup capability to perform an action or function when the primary capability is not operational. The level of redundancy is the number of independent mechanisms with the potential of accomplishing a given action or function. Isolation is the separation of an object from others. Functional isolation is the separation of a function from other functions or the isolation of redundant means of performing functions from each other. This effort segregates messages by buses and may redefine some of the logical data flow (defined in 60.2.2.3) to achieve redundancy.

The redundancy and isolation requirements for the overall electronic system and its individual functions, and for the multiplex system, are based on such factors as:

a. Criticality of the function or system: whether safety (flight) critical, dispatch (mission) critical, or not critical.

b. Mission success probability or flight safety requirements placed on the system.

c. System reliability requirements and later the derived subsystem reliability requirements.

d. A stated fault tolerance level (e.g., a requirement for no single-point failure or for fail operational/fail operational/fail passive).

e. Availability requirements (e.g., the vehicle must remain operational for a stated period, such as 14 days, without requiring maintenance).

Common levels of redundancy are single (no redundancy), dual, triple, and quadruple. Multiplex systems can be devised to implement all of these. Noncritical functions are often implemented with no redundancy; however, recent availability and reliability requirements are mandating redundancy for some of these functions. Mission-critical functions implemented without redundancy or with dual redundancy, usually provide sufficiently high mission success probability to meet requirements. Future systems may need redundancy or increased fault tolerance to meet availability requirements. Flight-critical systems typically use triple or quadruple redundancy.

Isolation can be electrical, physical, or logical. Electrical isolation can be achieved by placing functions or subsystems on different data buses. Physical isolation can be achieved by locating functions or redundant elements in separate boxes or separate locations in a vehicle. Multiplex systems can implement this requirement. Note that the multiplex buses must still be routed among the separate elements. Logical isolation can be achieved through dissimilar redundancy (i.e., two mechanisms of different design, capable of performing the same logical process), multiple copies of a process, multiple actions required to cause a reaction, or an external input.

60.2.2.5 Partition logical (functional-to-physical). The fifth step in multiplex partitioning flow is to perform preliminary functional-to-physical logical partitioning (Figure 60-5, item e). Subsystems required to perform system functions (e.g., navigation and weapon delivery) must be selected on the basis of their ability to meet

redundancy and isolation requirements. Preliminary physical data flow paths and their interfaces among subsystems, as well as between the electronic system and other parts of the vehicle, must be developed. Timing and sizing for both data transfer and processing should be estimated. Allowable data staleness (also called data senescence) must be considered. The overall use of data in the system must be described to apply the advantages of multiplexing as widely as possible.

a. **Functions of each sensor— Descriptions are needed for the inputs that** each sensor requires (including sensor control information), the processing (computation) of sensor data required for all system functions, and the data the sensor provides to other systems. The sensor redundancy concepts and how data from redundant sensors will be used need to be described, as well as sensor modes versus vehicle (avionic, weapon, flight control) modes. Descriptions of the interrelationships of sensors are required (e.g., inertial navigation update using another position-fixing sensor).

b. **Functions of control and display— Descriptions are required for the overall interface of the controls and displays to the rest of the electronic system, as well as which control and display functions depend on multiplexed data. Frequency of control inputs and response times** needed must be determined for controls, as well as preliminary update rates and formats for displays.

c. **Other electronic systems functions-** The advantages of multiplexing are not only applicable to the integration of sensors, processors, and controls and displays, but also to simpler devices like switch position sensors, actuator position sensors, and power sensing and control devices. Use of multiplexing to integrate this type of component must be investigated at the time requirements and concepts are developed to ensure its application. This is usually small-quantity data, a few bits per signal. These data can impact multiplex system integration and should be identified.

d. **External interfaces- Interfaces and data-passing relationships of the electronic system with other** vehicle functions, subsystems, and buses (including power, flight control, fuel, test, video and sensor signal distribution, mass data transfer, and hardwired signals) must be described. Some dedicated discretes will be used in an integrated system for certain critical functions (e.g., stores management arm enable, release enable, and jettison). They may be entered through general-purpose control panels on the 1553 buses. If so, special message handling maybe required (see 60.2.3.5 concerning message integrity).

60.2.2.6 Develop baseline multiplex topology. The sixth step in multiplex partitioning flow is to develop preliminary baseline multiplex topology (Figure 60-5, item f). Determine what subsystems must be connected to the multiplex network and whether they will connect directly, through a RT, or through a subsystem controller.

The preliminary multiplex topology must be defined based on the following:

a. Terminals to be connected to each bus and the projected length of main buses and stubs.

b. Preliminary physical data flows and data bus load estimates.

c. Requirements for redundancy, fault tolerance, and isolation of subsystems and functions.

d. Requirements for using Government-furnished equipment (GFE), and their protocol requirements and capabilities.

e. Requirements for using existing equipment versus designing new equipment and whether to make or buy.

f. Growth requirements including addressing; bus length; bus loading; minimizing stub lengths; and ease of modification to add subsystems, functions, or more buses.

BUS

g. Requirements for time synchronization and data latency control.

h. Requirements for data security, if applicable.

Preliminary topology block diagrams can then be prepared. A system requirements specification should also be prepared describing the topology, the media (specifically including 1553B electrical requirements), and the terminal hardware and firmware characteristics required to support the topology approach. The specification will be amplified during system control development to include 1553B protocol requirements and terminal hardware and firmware requirements to support the system control approach. The block diagrams and specifications should incorporate the required functions, subsystems, redundancy requirements, recommended partitioning method (functional grouping versus functional isolation), number of buses, dependencies of buses, control locations, interfaces between buses, unit separation, and physical sparing concepts. The topology must demonstrate growth reserve for buses (network structure), bus and stub length, bus separation, and ease of adding terminals and functions.

60.2.2.7 Develop baseline system control approach. The seventh step in multiplex partitioning flow is to develop a baseline system control approach (figure 60-5, item g). In the system control approach, the dynamics of the system are implemented so that the electronic system components and the physical network (the topology) meet mission and performance requirements by meeting the requirements derived as outlined in this subsection. Two documents are key to describing the system control approach:

a. **System control procedures-** The system control procedures document contains procedures for initialization; normal system operations; abnormal system operations; and system reconfiguration, recovery, and shutdown. Fault tolerance, system-level fault collection, and hierarchical control considerations (e.g., data passing and data routing) are system issues that must be defined. This system-level document will form the basis for developing software implementation requirements.

b. **Requirements specification-** The requirements specification will be developed using system control specifications and requirements. It will include 15536 protocol requirements and terminal hardware and firmware requirements to support the system control approach and will form the basis for subsystem specifications.

   The first section to be added to the requirements specification defines precise requirements for use of MIL-STD-1553B and its options. This section, referred to as the protocol document, eventually becomes part of the Multiplex Interface Control Document (MICD). It defines the use of options in 15536 and the notices that are mandatory for the system being developed. It also identifies required word formats and word format rules (e.g., transmit floating point based on format used in system computers).

The second section to be added to the requirements specification defines unique requirements for BCs and RTs. Key requirements are in the areas of error- and fault-handling capabilities, and terminal autonomy with respect to the host subsystem or processor.

The RT specification will form the basis for hardware requirements. The BC specification must include extensive hardware and control requirements. The application of consistent software, hardware, and firmware requirements to all contractors and subcontractors will help ensure consistent use of the standard, will ease integration, and will simplify multiplex system control.

Key considerations for system control development are:

a. Multiplex control strategy considering stationary BCs or dynamic bus control (rarely used).

b. Bus control-passing strategy, whether backup bus control switchover for stationary BCs or round-robin or polling contention for dynamic BCs. This includes the handshaking method used for bus control switchover, and the strategy for keeping the backup bus controller (BBC) updated if it is a “hot backup”.

c. Processing partitioning scheme: distributed versus centralized or federated versus independent tasking relationship.

d. Processing and subsystem sparing concept: hot versus warm versus cold versus pooled versus dedicated.

e. Periodic versus aperiodic data transfer requirements, repetition rates, and data latency and jitter requirements.

f. System time base implementation requirements and multiplex time synchronization strategy.

g. Required intelligence and autonomy of multiplex BCs and RTs (whether embedded in a subsystem or standalone) for system to meet error and fault-handling requirements.

h. Relationship among multiple multiplex data buses (if applicable) and between the electronic system multiplex buses and external functions and buses. This includes their required control and data dependencies.

60.2.3 Multiplex system integration considerations. Multiplex system integration, which follows system partitioning, consists of performing system trade studies and developing alternative system designs. System trade studies concentrate on achieving overall system operational capability. This is done by developing a system model that integrates all of the inputs, processing, outputs, and system modes or states in a real-time operational environment. Multiplex design trade studies should cover considerations such as: system architecture; functional partitioning; hardware and software partitioning; redundancy and fault tolerance; system reconfiguration or degradation modes; packaging approaches; level of repair; built-in test (BIT) philosophy and fault coverage; data bus protocol options; reliability allocations; weight, volume, and power allocations; system processing requirements; man-machine partitioning (level of automation); subsystem interfaces; and standardization.

Alternative concept designs are then developed and analyzed to determine the best solutions to mission and performance requirements. Management cost and schedule considerations can then be applied to determine how well concepts meet overall requirements, what areas of technology risk exist, and what development areas will require more management visibility and attention. One of the design alternatives or a combination of several can then be selected as the baseline system design for the next development phase.

The following paragraphs (60.2.3.1 through 60.2.3.6) cover some key considerations of multiplex integration that do not usually drive the topology and system control design but can cause system design revisions later if inadequately analyzed and implemented during the design process. The considerations are data bus loading, time synchronization, data latency, redundancy and isolation, integrity of data bus and data transfer, and data bus security requirements.

60.2.3.1 Data bus loading. Data bus loading is the percent utilization of the total information transfer capacity of a multiplexed data bus. Determination of data bus loading during the development of a system is a key measurement of progress, efficiency, and design adequacy. A means of calculating the bus loading for a system and additional considerations required to refine the bus loading calculation are discussed.

The total information transfer capability (throughput) of a MIL-STD-1553B data bus is potentially 1 M bits per second, based on the 1-MHz frequency of the bus. The theoretical maximum is 50,000 20-bit words per second continuous transmission, with no gaps between words. (Each command, status, or data word uses 20-bit times on the bus.) The practical maximum bus loading is about 80% of the theoretical maximum, or 40,000 words per second taking into account typical bus control protocol. The practical maximum bus loading calculation is based on 10 data words per message (an average derived in the Data Word Formats study performed in development of Section 80), BC to RT or RT to BC message formats, and typical 50 us intermessage gap and 10 us response time (discussed in paragraph 60.2.3.1.1). The calculation yields a

typical message transfer time of 300 us, with 60 us (20%) dead bus time and 240 us (80%) to transfer a command word, a status word and ten data words. Note that the words per second rate would be increased by longer messages, other message formats, and shorter intermessage gap and RT response times; but would be decreased by bus loading considerations to be discussed in paragraph 60.2.3.1.2.

The 80% bus loading level is one above which bus timing and data transfer integrity must be controlled with increasing strictness. Otherwise, abnormal conditions, such as error and fault handling or dynamic transmissions such as variable-length interprocessor traffic and aperiodic message handling, can destroy periodic traffic timing and disrupt process tasking. Symptoms of overloading include increases in data latency, frame overflows, message retries and error handling, priority contention, delayed or suspended processes, number of interrupts, and interrupt response time.

Atypical military requirement is 50% to 70% maximum bus loading, allowing 30% to 50% spare bus throughput for growth. This is usually understood by the system integrators as percent of total bus throughput. Considering a practical maximum throughput of 80%, the true spare throughput is only 10% to 30% without resorting to special measures, including addition of buses. Therefore, military bus loading requirements should be based on the maximum practical bus loading. Contractors should design the system with generous spare bus capacity. Note that available spare bus capacity for growth would be much higher for a bus with a few RTs (e.g., 3 RTs), compared to a bus with many RTs (e.g., 30 RTs).

Bus loadlng calculation. The control bits, words, and messages associated with information transfer system management are overhead and reduce the data transfer capability. Because the data bus transmission rate is 1 M bits per second, and the word length is 20 bits per word, the word transfer rate is theoretically 50,000 words per second. The data transfer rate is reduced by the following overhead and variable functions:

a. Variable message lengths.

b. Message transfer formats.

c. Command and status word overhead.

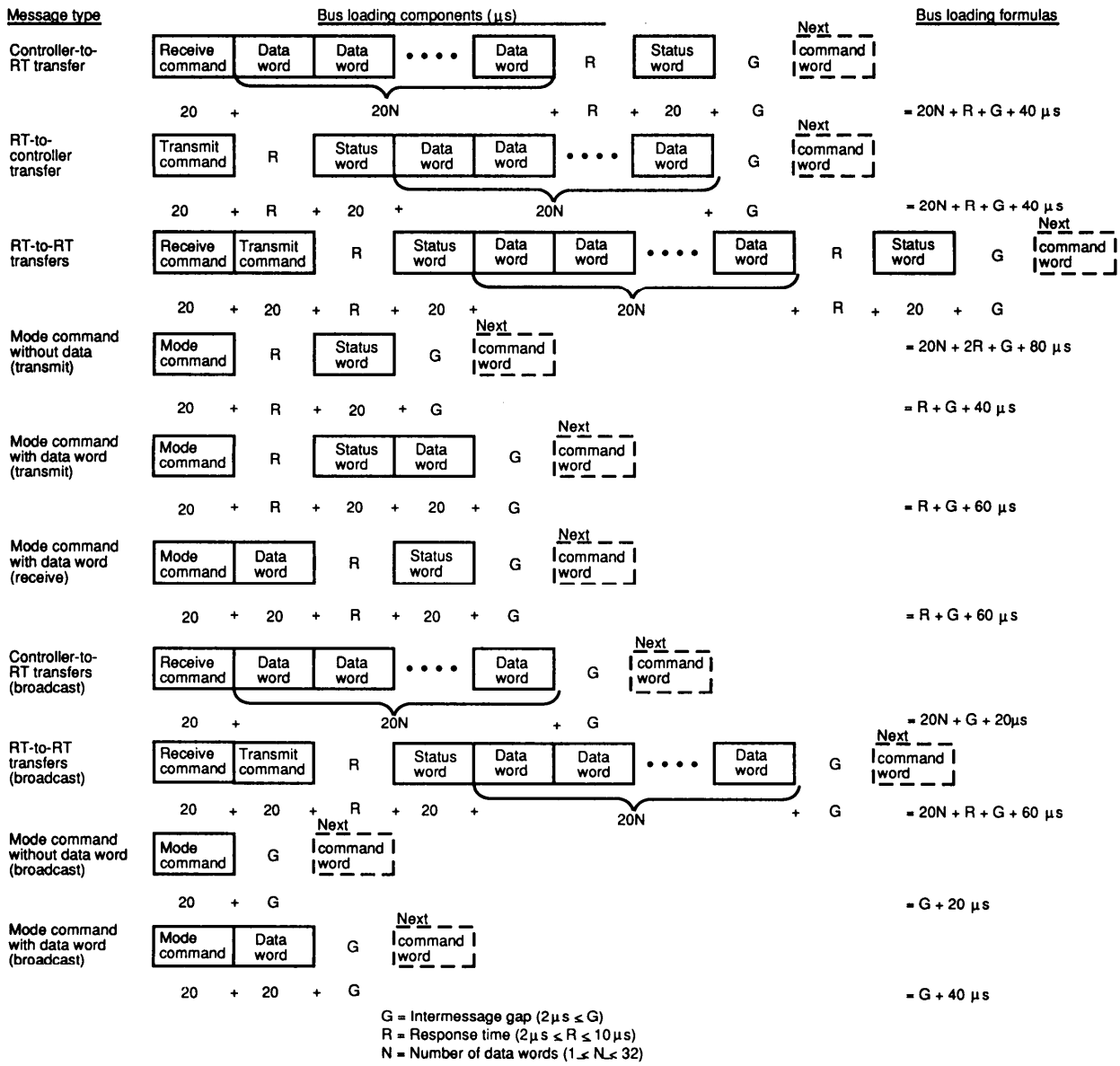
d. BC intermessage gap.

e. Response time gap.

f. Additional considerations required to refine the bus loading calculation (see following discussion).

First-cut bus loading and bus efficiency calculations can be performed as follows. There are five variables involved: (1) number of messages per second, (2) message length, (3) message type, (4) intermessage gap introduced by the BC, and (5) RT response time. If we pick or determine values for intermessage gap and response time, only the first three variables remain. Bus loading formulas by message type are presented in figure 60-6. The formulas consider overhead and variable functions (items a through e above). The formulas cover the ten message types (i.e., information transfer formats) allowed in MIL-STD-1553B. The formulas incorporate a variable, N, for the number of data words in a message, where applicable. The value of N can vary from 1 to 32.

Of the above five variables, message lengths and intermessage gaps usually have the most influence on the efficient use of bus throughput. Shorter message lengths have a higher percentage of overhead than longer messages. Therefore, longer data messages improve bus efficiency. The intermessage gap is a function of BC design and is the time it takes the BC to prepare for the next message after completion of a message. The intermessage gap is unrecoverable bus throughput time used along with each message and can be a very significant part of bus loading. The minimum intermessage gap specified in 1553B is 4 us, measured from the mid-bit zero crossing of the last bit of the preceding message to the mid-bit zero crossing of the next command word sync. This represents an actual delay of 2 us. An efficient BC should have an intermessage



Bus loading formulas (μs)

Message type	General formula	With minimum R&G*	With typical R&G**
• Controller-to-RT	20N + R + G + 40	20N + 44	20N + 100
• RT-to-controller	20N + R + G + 40	20N + 44	20N + 100
• RT-to-RT	20N + 2R + G + 80	20N + 86	20N + 150
• Mode command without data (transmit)	R + G + 40	44	100
• Mode command with data word (transmit)	R + G + 60	64	120
• Mode command with data word (receive)	R + G + 60	64	120
• Controller-to-RT (broadcast)	20N + G + 20	20N + 22	20N + 70
• RT-to-RT(s) (broadcast)	20N + R + G + 60	20N + 64	20N + 120
• Mode command without data word (broadcast)	G + 20	22	70
• Mode command with data word (broadcast)	G + 40	42	90

* Minimum: G = 2 μs R = 2 μs

** Typical: G = 50 μs R = 10 μs (maximum but typical value)

Figure 60-6. Bus Formulas by Message Type

gap of *30* us or less. Atypical BC intermessage gap is 50 us. This value will vary for BC-based factors, such as interrupts required, type of message, and BC processing required to handle the current message data or setup for the next message. A worst case combination of message length and intermessage gap effects will occur when the message lengths are short and the intermessage gap is long. This combination has more frequent, long intermessage gaps and high overhead-to-data ratio messages, yielding very low efficiency data bus utilization.

Note that message type selection may have more influence on bus loading than intermessage gap and message length, depending on system data passing requirements. For example, if the BC and an RT need data from another RT, a single RT to RT transfer can replace an RT to BC transfer, followed by a BC to RT transfer. The BC monitoring and storing the data from the RT to RT transfer saves 20N+50 us, typically.

To calculate a first-cut bus loading, determine the number of messages of each type to be transmitted per second and the number of data words in each message. Decide whether to use the general formulas or the formulas with minimum or typical intermessage gap and response times of Figure 60-6. Then use the formulas to determine the number of microseconds each message will use on the bus. Sum these message times. The total is the number of microseconds per second of bus loading. Dividing the total microseconds by 1×10^6 us and multiplying by 100 yields the first-cut percent bus loading.

Percent bus efficiency is the ratio of the number of data bits transmitted per unit time (e.g., 1 see) to the total microseconds of bus use per unit time multiplied by 100. It can be calculated as follows: Sum the number of data words, N, in all of the data messages transmitted per second. Do not include data words associated with mode commands, because they are overhead (control) words. Then multiply the total data words per second by 16 (i.e., 16 data bits per data word) to determine total data bits transmitted per second. Then divide the total data bits per second by the total microseconds of bus load per second (calculated in the previous paragraph) and multiply by 100 to yield the first-cut percent bus efficiency.

Rough quantitative measures of nominal, low and high percent bus efficiency can be calculated, given the following assumptions. Assume: BC to RT and RT to BC message types only, 50 us intermessage gap (G), 10 us response time (R), 10 data words per message for nominal efficiency, 1 data word per message for low efficiency, and 32 data words per message for high efficiency. The formula in Figure 60-6 for BC to RT or RT to BC messages with typical R and G, is 20N+100 us. The percent bus efficiency is the microseconds of system data per message (16-bit data words) vs. the total message time, or 16N divided by 20N+100 and then multiplied by 100. The nominal bus efficiency measure is therefore 160 divided by 300 and multiplied by 100, or 53.3%. The low bus efficiency measure is 16 divided by 120 and multiplied by 100, or 13.3%. The high bus efficiency measure is 512 divided by 740 and multiplied by 100, or 69.2%.

Additional bus loading considerations. The initial and projected growth of bus loading for the vehicle lifetime should be estimated during multiplex system design. This will ensure adequate spare bus loading or show the need for additional buses in the topology, either initially or for future system enhancement. Key considerations are:

a. **Periodic bus loading-** The periodic traffic and periodic overhead on the bus includes the data traffic and mode command traffic calculated in previous paragraph and the bus loading due to considerations in items b. through g. below (if not already included).

b. **Frame synchronization overhead-** The amount of time required to initiate each major and minor frame, if any, must be estimated. Any provision for flexible (overflow, often referred to as ‘rubber”) frame length and frame overruns should be included. The time required by the BC to set up for frame synchronization, during which it cannot send messages, should also be included.

c. Polling overhead- If the system polls each RT, or selected RTs, on a periodic basis, an estimate of this bus loading should be included in the overall calculations. Polling can be done to prove communication with the RT, retrieve service requests, and verify RT or subsystem health.

d. **Interprocessor communication-** This is a significant part of bus loading in modern systems. Updates should be designed for a periodic rate and with a fixed size, if possible. Communications required for periodic sharing of system state data (called "checkPointing") and access or update of global memory should be part of this calculation, if used. The checkpointing also could be to a backup BC (BBC) to keep it apprised of current system-critical data and system state. These messages are sometimes called BBC state variable transfer messages and help the BC-to-BBC switchover to occur with minimal system interruption.

e. **Instrumentation messages-** During system design, messages for bus monitoring and telemetry may be included in the design. If these messages are to be left in the system after system deployment, whether for maintenance testing or for prevention of change to bus timing and dynamics, they should be included in the bus loading analysis.

f. **Test messages-** A test message, such as a wraparound message, is typically transmitted, from BC memory, over the bus and stored in RT memory. The RT may then process the data (e.g., performing a twos complement calculation), and, as commanded by the BC, retransmit the processed data to the BC, where a data comparison is performed. This technique has been found effective for periodic testing of subsystem and RT communication capabilities. It can replace other usual error- and fault-handling mechanisms, including polling for RT status response and most uses of the terminal flag and subsystem flag status bits. Its use does add some bus loading that must be included in the analysis.

g. **Subsystem status messages-** RTs on the bus may be polled periodically for subsystem health messages. This can replace or supplement some other error and fault handling. Although typically performed at a low rate, the bus loading caused by these messages must be added to the analysis.

h. **Aperiodic message traffic-** It is important to estimate, as accurately as possible, the average and peak occurrences of aperiodic messages per time period, usually per major frame. An important subset consists of a periodically requested messages. In addition to aperiodic data messages, aperiodic bus loading must include the considerations in items i and j, below. Use these estimates, along with periodic data and periodic overhead estimates to arrive at average and peak bus loading.

i. Message retries and error or fault handling— These are considered abnormal operations and traditionally have not been added to the data bus loading. Under normal conditions, when the system is working, the contribution of this traffic is minimal. For example, there should only be about 13 retries per hour on a data bus, which meets the 1553B bit error rate requirement, running at 70% bus loading. However, when bus loading gets high or there are failures in the system that require retries, error handling involving mode commands, redundancy management, or reconfiguration, the bus loading increase can be significant. The effects on peak bus loading should be calculated.

j. **Data routing overhead in hierarchical systems-** Data transfer from one bus to another in hierarchical topologies often requires specific additional messages or data words in messages to control routing of data from upper to lower buses and routing of data and bus status from lower to upper buses. The additional data bus loading due to these messages must also be considered in the loading analysis. Note that these messages may be either periodic or aperiodic.

60.2.3.2 Time synchronization. System time synchronization is a critical aspect of achieving real-time mission performance requirements in a system design because (1) the periodic nature of communications requires a common time reference and (2) time tagging of data to correct for latencies also requires a common time reference. A time-synchronization scheme must be selected early and incorporated in specifications for all the contractors and subcontractors to ensure its consistent application. If this is not done, two main problems occur. First, the selected scheme may not be accurate or expandable enough to meet requirements of system enhancement contracts. Second, if a consistent and expandable scheme is not implemented, the system will end up (or even start out) as an assortment of different time-synchronization schemes. The result is more processing and more algorithms than a system using a single consistent scheme.

Time synchronization is particularly important to the multiplex system for consistency in the initiation of periodic major and minor frames (see 60.3.3.1); for initiating critically timed messages; or for time tagging messages to indicate their time of creation, transmission, or receipt.

Two common methods of implementing a system time base are:(1) hardwired discretes that distribute master clock pulses among subsystems and (2) messages over the data bus that periodically synchronize independent timers in subsystems. Three methods of synchronizing over the data bus are:(1) the synchronize without data word mode command, (2) the synchronize with data word mode command, and (3) a data message containing time or reset data. The usual method of initiating the next minor frame in a multiplex system is a real-time clock interrupt. The real-time clock is adjusted using system synchronization data provided by the selected synchronization method.

60.2.3.3 Data latency analysis. Data latency (aka, data staleness) is a measure of the time delays experienced in data transfer and processing from sensor or data source to the using algorithm or data sink. The multiplex contribution to latency is in the data transfer and buffering process. Considerations in analyzing and controlling latency in the system include:

a. There are several multiplex transport delay factors to be considered. The bus media delay time is negligible, approximately 1 ns/ft. Most modern BCs operate asynchronously with respect to their host processor, therefore, delays between processor creation of data and BC transmission of data, and between BC receipt of data and application use of data, must be analyzed. The data transport delays may also be influenced by the time required for the BCs host processor to notice and act on flags (also called, semaphores) set by the BC, or to respond to processor interrupts set by the BC. Data bus protocol overhead times, including command word, status word, intermessage gap, and response time, must be considered. Bus frame synchronization times, polling, and other fixed-rate components of bus loading (see 60.2.3.1) can add to the transport delay. For data transfers between data buses, data buffering and retransmission add delays. Dynamic components of bus loading, such as data frame extension and error and fault handling, complicate latency analysis by adding uncertainty (also known as jitter) to the calculated latency.

b. Processing time is also a contributor to data latency. Processing delays can be small or very large. Kalman filter processing of navigation data, for example, can add several seconds of latency. Most applications will add an average of one minor cycle of delay (i.e., 15.625 ms at 64 Hz minor cycle rate) on incoming data and one minor cycle of delay on outgoing, considering that they input data one minor cycle, process it the next, and transmit it the third minor cycle.

c. Time tagging and extrapolation of data is a common technique used to compensate for time delays. A time tag (e.g., a data word that contains the time of data sampling with respect to synchronized system time) may be required if latency is unacceptable.

d. Critically timed messages with guaranteed transmission in specific minor frames may reduce latency to a tolerable amount.

e. Uncertainty (jitter) in time of arrival and use, because of response time of host or because of frame length variation or clock uncertainty and granularity, must be included in the analysis.

f. Performance requirements usually impose a limit on the staleness of data. This is referred to as the maximum latency of the data. To determine if a system meets the latency requirements, all the worst case delays in generating and transporting the data are summed and the sum compared to the maximum allowable latency for the data. Minimum latencies are usually of academic interest only.

Figure 60-7 shows an example latency analysis. In this example, an inertial navigation system (INS) is the sensor, and position update of a missile during a launch process must be achieved with acceptable latency. A navigation processor acquires data from the INS, processes it, transmits it to a weapons processor that

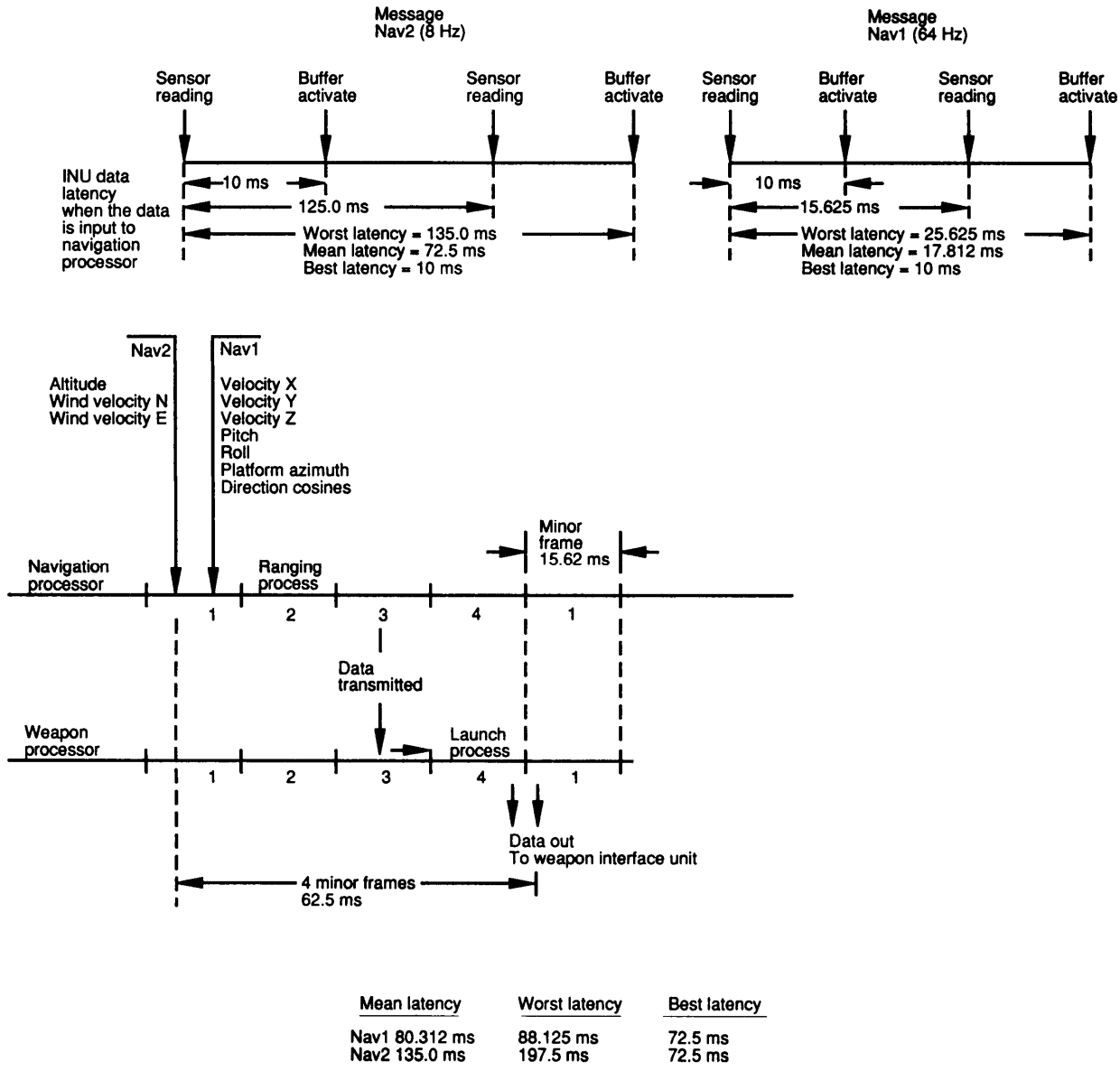


Figure 60-7. Latency Analysis of Carrier Inertial Data Transfer to Missile

transmits it to the weapon interface unit. The bus delays are negligible and are ignored. The largest component of latency is due to an 8-Hz sampling rate of data from the INS.

60.2.3.4 Redundancy and isolation. The system design must be examined to verify redundancy and isolation requirements. Usually redundancy requirements that are derived from availability requirements alone will be shown to be satisfied when the probability of common-mode failure of redundant elements is at a satisfactory level. The common terminal portion of dual-redundant buses (e.g., the subsystem interface) has been shown to satisfy mission availability requirements. However, if isolation is also a requirement, the degree of isolation achieved must be examined carefully. Two key issues are: (1) the redundancy of data paths and how far into the input and output devices and processors the redundancy is carried and (2) bus control redundancy and isolation requirements and how bus control switchover is to be implemented.

RT implementations are built with differing levels of internal redundancy. Section 50 discusses commonly used levels of internal RT redundancy. The system engineer must determine the required redundancy level

for the system and then levy appropriate requirements on the hardware and software. For the vehicle to meet performance and availability requirements, the internal redundancy of RT components and associated subsystem interface and processing components must meet the derived requirements (e.g., redundancy, isolation, reliability, and common-mode failure).

Redundant BCs may have a common-mode failure in the switchover mechanization. Vulnerability to common-mode failure may be reduced by making the switchover itself redundant or by employing multiple methods of implementing switchover. For example, either a discrete or lack of bus traffic could initiate a switchover. Special bus "claim" messages by the current controller can be effective in preventing contention for bus control

60.2.3.5 Integrity of data bus and data transfer. The 1553B data bus has proved to have an acceptable error rate for military aircraft avionics, including weapon delivery. However, 1553 buses are not error free, so system designers must supplement the data bus error detection capability with additional error detection if the rate of error detection inherent in a 1553 bus implementation is inadequate. Note that contaminated data may be used by application software unless a data validation technique is implemented and its indications of invalid data are heeded by the application. Following is a review of 1553B error detection capabilities and a discussion of data transfer integrity.

Unenhanced 1553B integrity. Based on the noise test conditions and maximum word error rate of one part in 10E7 (1553B, paragraph 4.5.2.1.2.4), 13 message retries per hour can be expected at 70% bus loading. Experience has shown that bus systems typically have either a much better or a much worse retry rate than this. Most problems that cause retries will be discovered and corrected during system development testing. If broadcast is not used, all message completion failures are detected. For broadcast messages with critical data, completion can be verified by either asking for playback of the data, or using transmit status or transmit last command mode commands.

Implementation of the 1553B Notice 2 requirement that no single-point failure shall cause a terminal to validate a false address should reduce the incidence of problems caused by incorrect address decoding. Without a mechanism such as address line parity, it is possible that connector failures can be undetected and change the physical address of a terminal. Address errors may also occur because of misinterpretation of a command word caused by a loss or shift of bus signal time reference. In production multiplex systems, these anomalies are readily diagnosed.

Data transfer Integrity. Some applications may require data integrity higher than that provided by the unenhanced 1553B error rate. Additional error detection may be achieved by adding system-level error detection or by adding data protection to specific messages. The multiplex system may be viewed as a means of transferring data from one memory to another, for example, the data buffer of a subsystem to the memory of a BC processor. A system-level test using periodic wraparound messages with known characteristics has proved to be an effective means of verifying the physical data transfer path integrity on a periodic basis and has low system impact. The periodicity of data wraps must match the data transfer integrity need. A low periodicity (e.g., 2 Hz) of data wrap introduces the need to analyze the latency of a detected fault. One-half second may be sufficient. Higher periodicity of data wrap may be required for statistical confidence. However, if statistical confidence is not enough for some special data, additional data validation tests can be performed. The data integrity (message validation) features inherent in a 1553B system and specific techniques for adding data validation tests at the application software level to enhance data integrity are discussed in paragraph 60.3.3.3.

Some considerations used to determine that the required level of data transfer integrity has been achieved in a system are:

a. **Analysis of consequences of using incorrect data.** The periodicity of vehicle control commands is usually established so that a single incorrect command is of no effect. Special attention should be given to accumulators, however. For example, a single bit error in the most significant bit could alter velocity, distance, or time significantly.

b. **Tradeoff of isolated redundant voting approaches versus self-test.** Modern digital systems can be designed for very good self-diagnosis or self-fault detection. Therefore, self-test maybe economical compared to additional hardware, including redundant multiplexed data paths.

c. Use of the subsystem flag bit in the status word. Watchdog timers are frequently used to detect software out of control, that is, failure by the software to keep a timer reset. An effective system indication of such an event is to set the subsystem flag bit in the status word. Even though the data may appear reasonable, at least initially, the subsystem flag conclusively indicates that the watchdog timer detected a failure.

d. **Use of the terminal flag bit in the status word.** Self-test of the terminal mayor may not be initiated independently by the system, but this bit should always be used by the BC to detect a terminal failure.

60.2.3.6 **Data bus security reauirements.** The application of multiplex data bus networks to military aircraft has provided a significant level of subsystem and data integration, expanding the capabilities of avionics systems. This integration may include transfer of classified data via data bus.

System security policy. The system security policy is established by the Government program manager. The details of this policy that impact system designers are provided in the program security classification guide and its references. Some major areas that may impact the design are:

a. The maximum classification of the data processed by each of the systems using the bus.

b. The maximum classification and separation of the data transferred via the bus.

c. The maximum authorized classification and separation of the systems connected to the bus.

d. The access authorization of the various crew and maintenance personnel.

Red/black architecture requirements. If any of the subsystems with terminals process red information, then the data bus network design must address three complementary security areas: (1) compromising emanations (i.e.: TEMPEST), (2) encryption, and (3) trusted message routing and control.

System security architectures, each with different advantages and disadvantages, are:

a. **All-black bus-No** red data or red data processor is directly connected to the bus.

b. **All-red bus-All** systems connected to the bus are authorized access to the highest data classification and all compartments using the bus.

c. Red/black gateway—Separate ail-red and all-black buses (as defined above) are used with a gateway to allow necessary data to pass between them securely.

d. **Red/black composite—On a time-share basis, the bus** processes red and black data between red and black subsystems securely.

Tempest requirements. Tempest requirements must be fulfilled by the bus interface circuitry and the transmission media (bus network) for data bus systems processing red information. The data bus network shall fulfill the Tempest provisions of the following documents:

a. NACSIM-5100 andNACSIM-5112 for U.S. military systems.

b. BID/01/202 (4) and BID/01/200 (series) for United Kingdom military systems.

c. AMSG-719 and AMSG-720 for NATO military systems.

d. Equivalent national requirements for other national military systems.

In complying with Tempest, the following comments clarify the requirement:

a. **All-black systems-** There is no Tempest requirement unless encryption is used; then Tempest design must be included to prevent compromising emanations from bypassing the encryption.

b. **All-red system-** The transmission media must fulfill the Tempest requirements. For data bus systems, the cable must be thoroughly shielded and grounded, usually to and through the connectors. For fiber-optic systems, the electrical-to-optical converters must fulfill the Tempest requirements and the optical signals must be designed to prevent compromising emanations between signals within the cable.

c. Red/black gateway systems-The gateway must fulfill Tempest requirements in isolating the red bus from the black bus. The red and black buses must fulfill the requirements shown in items a and b above.

d. **Red/black composite systems-The transmission media must fulfill the Tempest requirements as** shown in item b above. In addition, Tempest requirements must be fulfilled in both directions across the bus interfaces (e.g., isolating black data processing equipment from the red data messages on the bus and isolating the red data processing equipment from the black data messages and bus cabling).

Encryption designs. Encryption techniques are used by the data bus network and its associated terminals and processors to convert red data into black data and to isolate multiple classification levels and compartments of red data. The specific encryption technique and system design must be approved by the Government agency responsible for encryption certification.

Encryption requirements can be applied to the system architecture as follows:

a. **All-black systems-** Encryption is required to convert any red data to black data to preserve the all-black bus architecture.

b. **All-red systems-** Encryption may be required to isolate different classification or compartment levels.

c. Red/black gateway systems- Encryption may be required on the individual red or black buses for the reasons listed in items a and b above.

d. **Red/black composite systems-** Encryption may be required on individual data messages for the reasons listed in items a and b above.

Trusted message routing and control design. The data bus network design must fulfill the requirements of DOD 5200.28-STD, “Department of Defense Trusted Computer System Evaluation Criteria,” or national equivalent, with less than one undetected control error per 10,000 hrs of operation at the maximum bus message transfer rate. Corrective control action to maintain and restore system trust must be incorporated for detected system security failures.

The data bus network can be designed to meet these requirements by using the following:

a. Low bit error rate circuitry and cabling techniques.

b. Parity coding of control words involved in message routing.

c. BC monitor to detect and correct message routing errors.

Application to the systems architectures is as follows:

a. **All-black systems-** There are no trusted-message routing and control requirements unless encryption is used in the system. If encryption is used, trusted-data routing and control requirements must be incorporated to ensure that the approved encryption processes are not circumvented by failure or manipulation.

b. **All-red systems—** There is no trusted-message routing and control requirement unless multilevel security system design is imposed by different classification or compartment levels.

c. **Red/black gateway systems-** The gateway must fulfill all of the requirements for trusted-message routing and control. It maybe necessary to fulfill these requirements for data transfers in both directions across the gateway because of systems integration requirements. In addition, the separate red and black buses may have to fulfill the requirements shown in items a and b above.

d. **Red/blackcomposite systems-** These systems must fulfill all of the requirements for trusted-message routing and control at each RT and BC.

60.3 MULTIPLEX SYSTEM CONTROL. The basic philosophy of the information transfer system is that it must operate as a transparent communications link. Its management must introduce overhead into the transmission of data. The command word(s), status word(s), status word response time, and intermessage gap provide the framework for data transfer management. The status word provides link integrity information. The status word and mode commands are multiplex system management tools provided in the standard.

Every data transfer via the 1553B bus contains multiplex system control information in accordance with 1553 protocol. For the system designer to increase the multiplex system control capability, if necessary to meet system requirements, two options exist: (1) additional data transfers dedicated to multiplex system management (such as, data wraparound and periodic hardware health messages), and (2) use of the optional multiplex management capability provided in the standard.

The bus controller (BC) is responsible for initiating all information transfers on the data bus. Control defined for the multiplex system must allow the data to arrive at a terminal, be processed, and depart in a timely and synchronized manner.

60.3.1 Multiplex protocol. Protocol is defined as a code prescribing strict adherence to correct etiquette and precedence. In 1553B, the data bus protocol determines how the terminals will know when to transmit or receive. Because the standard covers a wide variety of designs, flexibility has been achieved without the loss of interface compatibility by allowing options to be selected by the user. Protocol options are available in the following areas: information transfer formats, status word bits, and mode commands. Paragraphs 6.3.1.1 through 6.3.1.3 provide guidelines for selecting and using the protocol options.

The system designer must select options that allow the necessary flexibility in the multiplex system design. The design should provide the control mechanism, architectural redundancy, degradation and reconfiguration concept, and traffic patterns required by the system. For systems designed to Notice 2, several of the formerly optional protocol features are now required and, in a few cases, restricted from being used for Air Force internal avionics applications.

60.3.1.1 Information transfer formats. There are ten message formats defined in paragraph 4.3.3.6 of MIL-STD-1553B. These message formats have been subdivided into two groups: six normal (non-broadcast) information transfer formats, as shown in figure 6 of the standard; and four broadcast information transfer formats, as shown in figure 7 of the standard.

Of the six information transfer formats, four are required to be implemented in RTsper MIL-STD-1553B, Notice 2. They are the controller to RT transfer, the RT to controller transfer, the RT to RT transfer and the mode

command without data word transfer. Implementation of the mode command with data word (transmit) and mode command with data word (receive) formats is optional; however, per Notice 2, bus controllers must have the capability to issue all of the information transfer formats defined in the standard. This means that while bus controllers must be capable of exercising the optional message formats, the system multiplex protocol has the option of not implementing those formats.

There are four broadcast information transfer formats. All four of these formats are optional in 1553B. They are the BC to RT transfers, the RT to RT transfers, the mode command without data word, and the mode command with data word. These formats would only be implemented if broadcast of messages or mode commands are implemented in the system. Per 1553B Notice 1, the broadcast command may not be transmitted on the data busby the BC in Air Force avionic applications. Therefore, use of these broadcast formats are prohibited in Notice 1 systems. Per 1553B Notice 2, the only broadcast commands allowed to be transmitted on the data busby the BC are the broadcast mode commands identified in table I of the standard. Therefore, the BC to RT transfer and the RT to RT transfer broadcast formats are prohibited, and the mode command without data word and the mode command with data word broadcast formats are allowed options in 1553B Notice 2 systems. Refer to paragraph 60.6.1 .4.2 for a discussion of considerations and limitations of implementing broadcast messages in a system.

60.3.1.2 Status bit options. There are eleven status word bits defined in paragraph 4.3.3.5.3 of MIL-STD-1553B. Three of these bits are resewed for future use. Of the eight bits available for use, implementation of the message error bit is required, and implementation of the other seven bits is optional or conditionally optional as described below. System application of the status word bits is discussed in paragraph 60.3.4.4.

a. Message error bit—The message error bit is required to be implemented in RTs. The system designer may choose to implement the transmit status word or the transmit last command mode command to examine the message error bit associated with the previous transmission. This examination would be useful in cases where a non-automatic retry is required. For example, block transfers over the bus, sent in several messages, may require that retry of an individual message only occur after verification that the message was not received and stored by the receiving RT. This cautious approach could be necessary to preserve the order of data in a stack or to prevent the Ioss of or duplication of a message length segment of data. The transmit last command mode code would retrieve the last valid command processed by the receiving RT, and the ME bit in the last status word would indicate if the data associated with the last command was valid and stored or invalid and discarded.

b. Instrumentation bit—The instrumentation bit is always set to a logic zero. In order for the instrumentation bit feature to function, the corresponding bit in all command words within the system must be set to a logic one. A terminal (usually a bus monitor) can then determine whether the word received is a status word or a command word. The system designer must decide whether to implement an instrumentation bit in all command words, that is, to always have a logic one in the equivalent bit position in the command words. Because the corresponding bit position in the command word is also the most significant bit of the subaddress field, the effect of implementing instrumentation bits is that it limits the number of usable subaddresses to 15 receive and 15 transmit.

c. Service request bit—The service request bit is optional. The system should implement the capability to recognize the service request bit set in the status word if there are any terminals that require asynchronous data or have data to transmit asynchronously. The status bit maybe recognized either in the BC hardware or in bus control software. The transmit vector word mode code is usually implemented along with the service request bit to handle RTs with multiple asynchronous messages.

d. Broadcast command received bit—The broadcast command received bit is optional in 1553B and 1553B Notice 1. This bit is conditionally optional in 1553B Notice 2, which states that if the RT implements the broadcast option, then this bit is required. If any broadcast messages are used in a system, the system designer should implement recognition of this status bit in the BC. Also, the transmit status word or the transmit last command mode command should be implemented to examine the broadcast command

received bit associated with the previous transmission. This examination provides message completion verification that is not provided by the broadcast message transfer formats, and is the only way to ensure that every terminal that was supposed to receive the broadcasted message did receive it.

e. Busy bit—The busy bit is optional in 1553B and 1553B Notice 1. This bit is conditionally optional for RTs in 1553B Notice 2 (paragraph 30.5.3). Notice 2 additionally provides specific conditions under which the busy bit may beset and requires that those conditions be predeterminable by the system designer. If the system contains any terminals that implement the busy bit, the system designer should implement recognition and some level of handling for the busy condition. The system response can vary from simple to complex. A simple response could be either to continue with normal message traffic or to do an immediate retry. A complex response could be for the BC to set a timer based on individual RT busy conditions and try communicating with the terminal after the timer expires.

f. Subsystem flag bit—The subsystem flag bit is optional in 1553B and 1553B Notice 1. This bit is conditionally optional for RTs in 1553B Notice 2, which states that if an associated subsystem has the capability for self-test, then this bit is required in the RT. The system designer should implement the capability to recognize and act on the subsystem flag bit if it is implemented in system RTs. If the system designer chooses to act on a subsystem flag bit, there are no mode commands available to retrieve the information from an RT. Typically, a subsystem status or BIT request message will be used to extract that information.

g. Dynamic bus control acceptance bit—Thedynamic bus control acceptance bit is optional in 1553B and 1553B Notice 1. This bit is conditionally optional for RTs in 1553B Notice 2, which states that if the RT implements the dynamic bus control function, then this bit is required. The system designer should implement recognition of this bit only if dynamic bus control is used in the system. The bit will typically be set as a result of the transmission of a dynamic bus control mode command by the BC. Note that dynamic bus control is not allowed in Air Force internal avionic systems.

h. Terminal flag bit—The terminal flag bit is optional in 1553B and 1553B Notice 1. This bit is conditionally optional for RTs in 1553B Notice 2, which states that if an RT has the capability for self-test, then this bit is required. The system designer should implement the capability to recognize and act on the terminal flag bit if it is implemented in system RTs.

60.3.1.3 Mode command options. The requirements for use of mode commands have evolved as the standard has evolved. In 1553B, the mode commands are all optional for both RT and BC. Systems built to the basic 1553B standard could implement any combination of mode commands or none. Notice 1 states that the mode codes for dynamic bus control, inhibit terminal flag bit, override inhibit terminal flag bit, selected transmitter shutdown, and override selected transmitter shutdown may not be transmitted on the data busby BCs in Air Force avionic applications. The mode code capability can exist in RTs and BCs as long as Air Force avionic systems do not implement the transmission of these five mode commands. Notice 2 states that the BC will have the capability to implement all of the mode codes, as defined in 4.3.5.1.7 of the standard, and that the dynamic bus control mode command shall never be issued by the BC for Air Force applications. Therefore, Notice 2 systems can implement any combination of mode commands supported by the RTs, with the exception that the dynamic bus control mode command shall not be implemented in the system for Air Force systems.

A set of optional mode commands for multiplex system management are defined in 1553B. Implementation experience has shown that typical uses have developed for particular mode commands and groups of mode commands. Table 604 lists the mode commands and their characteristics, identifies the mode commands required for RTs by Notice 2, and presents a matrix of mode commands and typical uses for each. The following paragraphs discuss the typical uses.

a. Periodic polling and frame start-Periodic polling and frame start are typical uses of the synchronize without data word, transmit status word, transmit vector word, and synchronize with data word mode

commands. Use of these mode commands either put the RTs into a known state, or retrieve data from the RTs so that the BC can determine the RT state. Status or vector word information retrieval and clock synchronization are examples of functions that can be performed by the polling or frame start communications. The capability to communicate with each RT can also be verified on a periodic basis.

b. **Time or event synchronization and subaddress extension-** Time or event synchronization and subaddress extension are typical uses of the synchronize without data word, and synchronize with data word mode commands. The synchronize without data word mode command can be used to notify an RT of an implicit action or time event. Reset clock, start a process, increment minor cycle number, and switch subaddress tables are examples of possible implicit meanings for receipt of this mode command by an RT. The synchronize with data word mode command is used to transfer an explicit value or action to an RT. Set clock to xxx, switch to subaddress table y, new minor frame is 24, and start process “INS align” are examples of explicit data that can be conveyed with the synchronize with data word mode command.

c. **Message error conditions-** Message error condition handling is a typical use of transmit status word and transmit last command mode commands. Invalid data reception by an RT causes it to set the message error bit in the status word and suppress the status word transmission. If the BC wants to determine message completion, it can retrieve the last status using transmit status word and see if the message error bit is set. If the BC wants to determine whether there was an invalid command or an invalid data reception, it can use the transmit last command mode command to retrieve the last status word and last command word to determine what happened. Note that some current systems do not use these mode commands for real-time message error handling. Lack of status word response is a good indicator of message completion failure, usually prompting the BC to retry a message or to proceed with other communications.

d. **Abnormal event handling-** Abnormal event handling is atypical use of transmit status word, initiate self-test, inhibit terminal flag bit, override inhibit terminal flag bit, reset RT, transmit last command word, and transmit BIT word. Some current systems do not perform real-time abnormal event handling using these mode commands. If retries on all possible cables do not solve communications problems with an RT, it may be taken out of the normal communications list. Then some systems simply try to talk to it periodically, while others may try to reset it or initiate its self-test and examine its BIT word.

e. Transmitter control-Transmitter control is the typical use of the transmitter shutdown, override transmitter shutdown, selected transmitter shutdown, and override selected transmitter shutdown mode commands. Some current systems do not implement these mode commands. Selected transmitter shutdown and its override are more useful for RTs with redundancies higher than dual, which are rare. Transmitter shutdown and its override have not proved very necessary in systems, because of the reliability of RT transmitters and their associated transmission watchdog timers.

f. Bus control switching-Bus control switching is the typical use of the dynamic bus control mode command. Dynamic bus control is very rare. The Air Force will not allow the use of dynamic bus control in their avionic systems. The Army and Navy allow the use of dynamic bus control but rarely implement it. Some Navy systems have proposed using dynamic bus control for maintenance purposes, on the ground, to transfer bus control to an external test set. The test set would then be able to directly exercise the system and gather test and maintenance data.

g. Broadcast message received verification-Broadcast message received verification is a typical use of the transmit status word and transmit last command mode commands. These mode commands would be very valuable in a system that uses broadcast messages to verify message completion after critical transmissions or perhaps after every broadcast transmission. Per 1553B Notice 1, the broadcast command may not be transmitted on the data busby the BC in Air Force avionic applications. Therefore, use of broadcast is prohibited in Notice 1 systems. Per 1553B Notice 2, the only broadcast commands allowed to be transmitted on the data busby the BC are the broadcast mode commands identified in table I of the standard. Therefore, the broadcast mode commands are the only broadcast messages allowed in 1553B Notice 2 systems. Extreme care is advised in implementing broadcast mode commands. Some

Table 60-I. Mode Commands Characteristics and Typical Uses

Transmit-receive bit	Mode code	Function	Associated data word	Broadcast command allowed	Required for RTs by Notice 2	Periodic polling and frame start	Time/event sync. and subaddress ext.	Message error conditions	Abnormal/event handling	Transmitter control	Bus control switching	Broadcast message rec'd verification	Aperiodic message handling
1	00000	Dynamic bus control	No	No		X	X				X		X
1	00001	Synchronize	No	Yes		X							
1	00010	Transmit status word	No	No	X			X	X			X	
1	00011	Initiate self-test	No	Yes									
1	00100	Transmitter shutdown	No	Yes	X	X				X			
1	00101	Override transmitter shutdown	No	Yes	X	X				X			
1	00111	Inhibit terminal flag bit	No	Yes					X				
1	00110	Override inhibit terminal flag bit	No	Yes					X				
1	01000	Reset remote terminal	No	Yes	X				X				
1	01001	Reserved	No	TBD									
		↓	↓	↓									
1	01111	Reserved	No	TBD									
1	10000	Transmit vector word	Yes	No		X							X
0	10001	Synchronize	Yes	Yes			X						
1	10010	Transmit last command	Yes	No		X		X	X			X	
1	10011	Transmit BIT word	Yes	No		X			X				
0	10100	Selected transmitter shutdown	Yes	Yes						X			
0	10101	Override selected transmitter shutdown	Yes	Yes						X			
1 or 0	10110	Reserved	Yes	TBD									
		↓	↓	↓									
1 or 0	11111	Reserved	Yes	TBD									

broadcast mode commands could be very valuable (e.g., the two synchronize mode commands for simultaneous time or event synchronization of all RTs on a bus). Any of the broadcast mode commands could be dangerous if accidentally transmitted by the BC or accidentally received by the RTs. Some, such as broadcast reset RT or broadcast initiate self-test, could be disastrous if sent or incorrectly received at a critical time during the vehicle mission.

h. **A periodic message handling-** A periodic message handling is a typical use of the synchronize without data word, transmit status, and transmit vector word mode commands. Transmit status is sometimes used to poll terminals for service request bit set. The transmit vector word mode command is used to retrieve data that direct the BC to the particular aperiodic service needed by an RT. Synchronize without data word is sometimes used as a handshake signal associated with an asynchronous transfer. Receipt of this mode command could be defined as completion of the asynchronous transfer, causing the RT to increment a message service request queue pointer. Alternatively, receipt of this mode command could be defined as failure of the asynchronous transfer, causing the RT to decrement a message service request queue pointer.

60.3.2 Multiplex system control procedures. Once the multiplex protocol has been determined, the system designer should use the protocol to develop the multiplex system control procedures. Control procedures include how the multiplex system will be started and initialized, normal operations, abnormal operations, and shutdown.

60.3.2.1 Multiplex startup and initialization. Multiplex system startup and initialization begins during system startup and continues from there. During system startup, power is applied to the subsystems. If there is a backup BC, procedures must be developed for applying power to the primary and backup BCs. The primary BC must be given an opportunity to take control of the bus. Once the power has been turned on to the BCs and they have been initialized, the primary BC can begin to initialize the other subsystems on the bus. It is recommended that the terminals and associated subsystems have power applied to them while they are in a known state so that multiplex communications with them can begin. Notice 2 requires that the status word transmitted by an RT following power up contain valid information. Once communications have been established with the terminals, program loads have to be transferred to those terminals that require it. The last step that may be required before the BC begins periodic message transfers is system synchronization using a mode code or data messages.

60.3.2.2 Normal operations. The most important functions of the bus controller and the bus control executive are to manage the normal transfer of data, initiate retry of transmissions, and call error and fault recovery procedures when normal transfers fail. The BC can use the synchronization mode codes (with or without a data word) or a data message to maintain system time synchronization and initiate periodic data transfer cycles.

Bus controllers should be designed to make an effort to complete every message transfer. This effort should include retries and bus switching as part of normal procedures. If a status word is not received by the BC in response to a normal (nonbroadcast) message, the controller should know if the particular message should be retransmitted and how many retries to attempt. Error or fault handling procedures (abnormal operations) may then be invoked that use mode commands, such as transmit status word or transmit last command, to determine if the message was received by the terminal.

If the controller is not successful in communicating with the terminal on the primary bus, transmission should be tried on the standby-redundant bus. If this is successful, then communications with that terminal normally should continue on the redundant bus, which now becomes the primary bus for that terminal. Communications to other terminals should continue on the primary bus, if possible. This requires that the BC have the capability to distinguish, on a message basis, which bus to use, and requires more complex BC software to accomplish. A simpler alternative is to switch all message traffic to the alternate bus after failure to communicate with an RT on the primary bus. If communications cannot be established with a terminal on either bus over a period

of time, the system must decide how to proceed. The system could continue trying normal message traffic to the RT, stop normal message traffic to the RT but periodically poll it attempting to re-establish communications, or declare the RT failed and stop all communications with it. The threshold of communication failures before the multiplex control function declares an RT to be nonoperational must be set by the system engineer. Some systems continue polling all RTs in case they lose power and then have power reapplied or recover from an error or fault condition.

60.3.2.3 Abnormal operations. Error and fault management are functions that handle abnormal events. The 1553B protocol options selected for the system (see paragraph 60.3.1) can dictate the type of error and fault handling that is designed into the BC and bus control executive which, together, accomplish the multiplex control function. Each system has different requirements for the detection, handling, and recovery from errors and faults. Errors are one-time or transient events that temporarily degrade bus timing or performance and can be corrected or tolerated. Faults are intermittent or permanent and require changes to system structure or operation to continue. It is the responsibility of the multiplex control function to manage errors and faults on the bus. The complexity of error management depends on the system requirements and design. The status word is frequently used as a way of detecting problems. The absence of a status word signals to the controller that there is a problem. The status word received during a normal transmission or by the use of a mode command may be analyzed bit by bit by the controller. It is possible that the format of the status words may be different if a non-1553B terminal is on the bus. The controller should be able to interpret different status word formats if there are RTs with different status word formats in the system. Note that some systems use the status word only as a means of verifying message completion and do not check any of the status word bits. Those systems generally implement message retries and means of verifying terminal health and status, such as periodic wraparound messages and subsystem status messages.

The complexity of the error management used can vary from simple to complex. A simple scheme is to ignore the error and continue. This places the responsibility on the application software and the specific task that needs the data to deal with missing or corrupted data. The controller may detect the error or fault, continue normal message traffic, and investigate the problem at the end of a cycle; or the controller may respond to the problem immediately. Depending on the severity of the problem, an error or fault recovery sequence could be executed. Failures or errors detected could be counted to assess repeated occurrences and recorded for evaluation after the mission is completed. (See 60.3.4 for further discussion on error and fault management.)

60.3.2.4 Multiplex system shutdown. There should be a specific routine that the controller must perform at normal shutdown. Note that the system should also be designed to function, in a degraded state if necessary, and recover from disorderly or random power-up or power-down of subsystems. Abnormal subsystem shutdown may occur, for example, due to power failure, battle damage or equipment failure. Normal system shutdown activities depend on the system requirements but can include the following:

a. **Classified data erase-** If there are classified data in the system and they are to be saved, they must be stored on a storage device that can be removed from the vehicle. Next, the classified data in the subsystems, BC, and mission processor must be erased by an acceptable means.

b. **Unclassified data save-** The system designer must determine ahead of time what data are to be saved before shutdown.

c. **Weapons status-** If the vehicle is carrying weapons, the status of each weapon must be known and safing activities must be performed.

d. **Power shutdown sequence-** No matter what device controls the power, it should be designed such that normal power shutdown to the subsystems is done in a known sequence. It is desirable for the BC to be the last subsystem to be taken off-line.

60.3.3 Data transfer control.

60.3.3.1 Data framing and phasing. Most multiplexed electronic systems operate on a fixed schedule of data transfers (i.e., periodic data scheduling). The scheduling requirements come from the examination of the largest and smallest process and data transfer iteration rates and allowable latencies.

The slowest iteration rate, which is usually the least common multiple of the faster iteration rates, is normally defined as the major cycle (see figure 60-8). Over the course of a major cycle, all periodic transmissions and computations occur at least once. Some exceptions do exist where the iteration frequency is low (such as Kalman filtering once per 6 sec or periodic built-in test functions once every 5 see). Typical major frames are 1/8 sec to 1/3 sec in length.

The minor cycle is normally the frequency of the most rapidly transmitted periodic data. Minor frame lengths can be binary (2N/see) or decimal (1 ON/see) with common values being 1 /64, 1/32, or 1 /50 sec. All timing on the bus is relative to the beginning of a minor frame, which may or may not be synchronized to a clock. Also, due to intermessage gaps, RT response times, unscheduled retries on the bus and BC internal timing, the relative time at which each message (periodic or aperiodic) is transmitted over the bus will vary within each minor frame. Figure 60-8 presents atypical minor cycle. (Note that the periodic messages item is the only portion of the minor frame shown that is found in all systems where framing is used.) Some or all of the following activities may occur during a minor cycle:

a. **Minor cycle synchronization-** By using one of the two synchronization mode codes or a data message, the BC can inform the subsystems of minor cycle start and minor cycle number. This may not be required in a system design.

b. **Periodic messages-** Periodic messages are scheduled messages (time critical) that have a specific update rate achieved by scheduling messages in specific minor cycles.

c. **A periodic messages-** Aperiodic messages are based on conditional events and are used to initiate other conditional events. Many systems do not have aperiodic messages.

d. **Error correcting, polling for status, and/or BC to BBC communications-** During this time, the BC can handle error-conditions that developed during the minor cycle. The BC can also poll those terminals

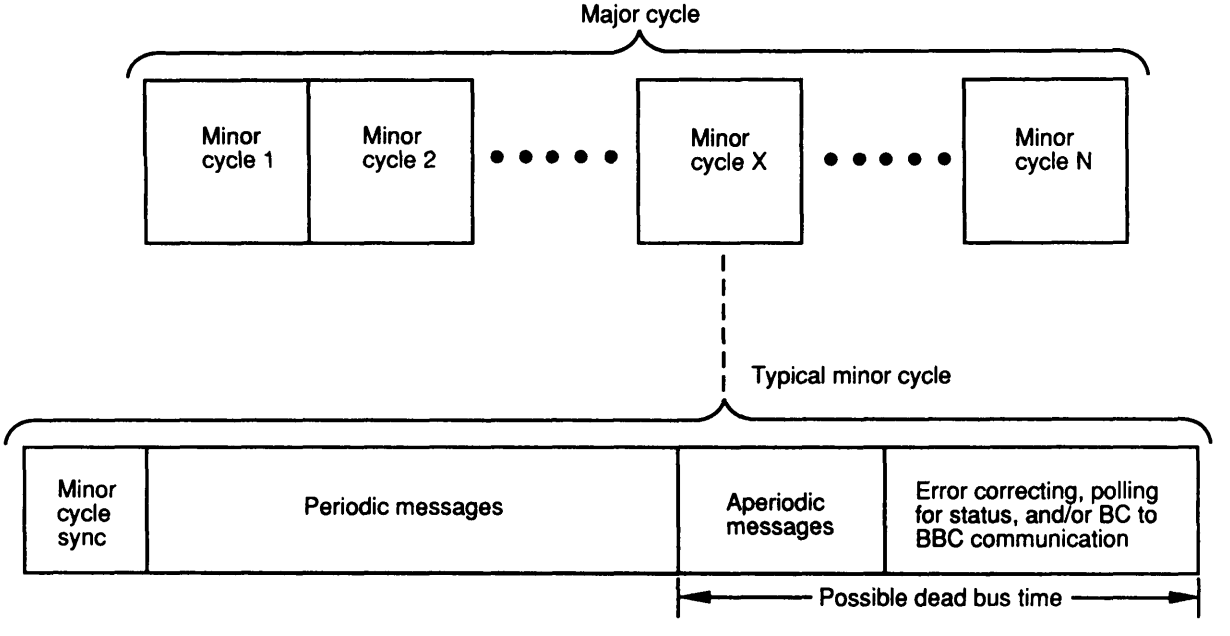


Figure 60-8. Major and Minor Cycles

that have not been communicated with to see if they require servicing. This period may also be used for BC to BBC communications. These functions could be handled as a part of scheduled periodic message traffic or, as shown here, as a low-priority (background) function.

Bus loading should be distributed as evenly as practical overtime. Bus load distribution is aided by the proper phasing or spreading out of data transfers overall available minor cycles. Even bus loading will allow time for error handling without minor cycle overflow and will allow room for addition of messages as system growth occurs.

60.3.3.2 Addressing and subaddressing. The BC uses the 1553 command word to identify which RT is to respond, if the RT is to transmit or receive data, what data are to be transmitted or received, and how many data words are to be transferred. Each terminal within a system must be assigned a unique address. Notice 2 requires that an RT be capable of being assigned a unique address, established through an external connector. Per the standard, if the broadcast option is used, then the terminal shall also recognize the address 31 (11111) as the broadcast address and terminal address 31 (111 11) shall not be used as a unique address.

The five-bit subaddress/mode field either specifies what data are to be transmitted or received by the terminal, or specifies that the five bits in the word count/mode code field area mode code. The subaddress/mode field should not to be used as an operation code to specify an action by the associated subsystem; that is, the command word should not convey data to the subsystem (only data words should). The codes 00000 and 11111 are used as mode command indicators. There are, therefore, 30 subaddresses left for use. Typically, the transmit/receive (T/R) bit is used in conjunction with the subaddress bits, establishing a six bit field which is used to identify 30 receive and 30 transmit subaddresses. If the instrumentation bit is used in the system to distinguish between a command word and a status word, then the possible subaddresses for each RT are reduced to 15 receive and 15 transmit (see instrumentation bit discussion in paragraph 60.3.1.2 for further explanation). Notice 2 requires that terminals implement a data wraparound capability. The notice states that data wraparound receive subaddress of 30 (11110) and transmit subaddress of 30 (11110) are desired.

The number of subaddresses is limited, so how they are used is an important issue. For some applications, the number of subaddresses is not sufficient. For example, a standalone RT that services a number of subsystems may require more than 30 subaddresses, and therefore need to extend the MIL-STD-1553B subaddressing scheme.

Two basic methods which have been used to extend subaddressing, without violating MIL-STD-1553B protocol requirements, are fixed subaddress maps and dynamic subaddress maps. The system designer defines the meaning of fixed subaddress maps. The processing during operational use defines the meaning of dynamic subaddress maps.

A single fixed subaddress map is a commonly used, non-extended subaddress mapping technique. In a common implementation of this technique, the subaddress and T/R bit of a command word are added to a base memory address to forma pointer into a table of memory addresses, the subaddress map. Each entry in the table is the memory address of the data buffer for that subaddress. The single fixed subaddress map can be easily extended to implement multiple fixed subaddress maps:

a. **Multiple subaddress maps, switched on a major frame, minor frame, or vehicle mode basis-** Typically, this works in a manner similar to the single subaddress map case, but a different base address is loaded into the terminal for use during a new frame or mode. The new base address points to a different subaddress map.

b. **Multiple subaddress maps, switched on demand-** A message, such as the synchronize with data word mode command, is typically sent to an RT causing it to switch to another subaddress map specified by the message. For a BC, the executive software will affect the subaddress map switch.

Three ways in which dynamic subaddress maps have been used in systems are:

a. A technique where the first one or two data words in the message are used as an index into memory or provide the memory address for the remaining data words.

b. A technique where a particular subaddress points to part of the subaddress table itself. The contents of a message to the particular subaddress overwrite a portion of the subaddress table, thereby changing the memory locations to which other subaddresses point. In the B1-B bomber, for example, there are four subaddresses dedicated to remapping portions of the subaddress table. A 16-word message sent to one of these subaddresses will remap eight other subaddresses, setting a new memory address pointer for each. The four dedicated subaddresses allow a total of 16 receive and 16 transmit subaddresses to be remapped. Refer to the B-1B example in Section 70 for more information.

c. A technique whereby a mission computer, acting as bus controller or a monitor, is not limited by the subaddress field of the bus command word in the receipt of or transmission of messages. This technique relies on the protocol of RT to RT transfers and is implemented in the C-17 transport aircraft, which uses approximately 70% RT to RT transfers. The technique relies on the mission computer (whether acting as BC, BBC or secondary BBC), selectively using the terminal address, T/R bit, and subaddress field of either of the two bus commands in an RT to RT transfer. Whether the receive command or the transmit command of the RT to RT message protocol is used for data mapping, and whether the associated message data is to be received, transmitted, monitored and stored, monitored for errors but not stored, or ignored is designated by two bits in each mission computers command block data for an RT to RT transfer. Refer to the C-17 example in Section 70 for more information.

60.3.3.3 Data validity. It is required that each data word conform to the following minimum validation criteria (1553B paragraph 4.4.1.1):

a. The word begins with a valid sync field.

b. The bits are in a valid Manchester II code.

c. The information field has 16 bits plus parity.

d. The word parity is odd.

Additional data validity tests are permitted by the standard as long as data and message format requirements are met. Because most methods require additional bits or data words, the bus overhead increases so the amount of data that can be transferred is reduced.

These validity tests provide very good data protection. (See 60.2.3.5 which discusses the numerical level.) However, if the level of protection it provides is not good enough, the following techniques have been used successfully to increase it:

a. **Transmission of muitiple copies-** More than one copy of the data is transmitted and then compared by the application software before use.

b. **Echo data-** Data are transmitted back to the transmitting terminal and compared with the data originally transmitted.

c. **Checksums-** This method is described in section 80 of this handbook. The checksum word consists of the arithmetic sum, without regard to overflows, of a selected group of data words. If required, more than one checksum may be used.

d. **Cycle redundancy check—** A cycle redundancy check (CRC) is an error-detecting code. It is also known as the polynomial code. A CRC does not correct an error but can cause the terminal to request a retransmission of the data.

e. **BCH(Base-Chandhuri-Hocquenghem) error detecting and correcting code (BCH(31,16,3)-** This method, described in section 80 (table 80-XIX) of this handbook, requires that the error protection word immediately follow the data word to be protected, so it increases bus loading significantly.

60.3.3.4 Data buffering validation. It is required by 1553B paragraph 4.4.1.1 that the terminal validate each word to a set of criteria. A terminal must have the capability to validate the data sent to it prior to the next command. (The standard defines the minimum time the BC must wait before it may send the next message in paragraph 4.3.3.7, but it does not impose this minimum time for a terminal. If a terminal cannot accept a command, it may set the busy bit. However, the use of the busy bit is discouraged by Notice 2.) All this requires that the terminal receive the message, validate it, and either transfer it to the subsystem or switch to another data buffer in time to receive the next command word transmitted to the terminal. The data maybe buffered in the terminal or in the subsystem memory. The following are example methods for meeting this requirement.

a. One method is to have a buffer such as a first-in/first-out (FIFO) in the terminal. As data are received, they are validated and then stored in the FIFO. If the data are all valid, they are transferred into the subsystem memory. If the data are not valid, they are not transferred to the subsystem and the next message is written on top of the last. In this scheme, timing of data transfer to the subsystem is critical due to the possibility of a subsequent message overwriting a valid message in the FIFO, awaiting transfer to the subsystem.

b. Another method is to have the terminal validate the data and then transfer it to the subsystem memory buffer using direct memory access (DMA). The transfer to subsystem memory maybe accomplished one word at a time or as a complete message after validation. Two buffers are usually established for each subaddress used by the terminal. In some designs, a tag word associated with each received message is generated by the terminal and stored in subsystem memory. A tag word can contain time of arrival, validity of complete message (per 1553 paragraph 4.4.1.1 criteria), and control flags for buffer access. For receive messages, the terminal toggles data buffers and buffer access flags. For transmit messages, the subsystem associated with the terminal performs these duties. A problem arises when the subsystem has not read the data in the buffers and new data are received. If nothing is done, the new data will overwrite the old data. In some cases, this is permissible, however, it should be evaluated on a message-by-message basis.

Another level of data validation maybe performed within the subsystem. Examples of these validation tests are data staleness tests, limit checks and data reasonableness tests.

60.3.3.5 Bulk data transfer. The 1553 data bus is not adequate for many repeated bulk data transfers, e.g., the transfer of several megabytes of data from one mass memory device to another. Therefore, the system designer should minimize such data transfers, especially if they must occur during real-time operations. Nevertheless, bulk data transfers via the 1553 bus may be cost-effective, considering the cost of other communication links. Up to 32 words per message are allowed to be transmitted by 1553B. Many systems today have requirements to transfer large amounts of data from one location to another. These transfers are usually between processors, processors and mass memory, processors and sensors, or processors and stores. Because only 32 words can be sent in one message, multiple messages have to be used. In systems with hierarchical buses, the amount of data that can be sent in one message may be further limited. For example, MIL-STD-1760 limits MIL-STD-1553 messages to 30 data words plus one or two words for control of data routing on lower buses.

The system designer must decide how to transfer a block of data using multiple messages. If the transfer is during real-time normal operations, then major and minor cycle timing could be used, and a message containing a part of the data could be sent every minor cycle. If timing permits, the messages could be transmitted back to back using command words with different subaddresses. The impact of the selected method on data consistency should bean important consideration.

Regardless of the method selected for transfer of bulk data, the system designer should consider using data checks, either CRC or checksums, to ensure that all data has been transferred correctly.

No matter what method is used to transmit the block, the system designer must be concerned about how to handle transmission errors. One method used when transmission errors are detected is to retransmit the message. Care must be taken that the correct message is sent on the retry. There is a possibility of a redundant or a missed message. Different methods have been implemented to prevent this from happening. One method is to use a message header word that describes that message and makes it unique. Another method is to send a handshake message to the transmitting terminal stating(1) correct message received so prepare to send the next message or (2) message received had an error so prepare to retransmit the same message.

60.3.4 Multiplex system error and fault management. Error and fault management should be designed into the bus control mechanization. Provisions should be made during system design to handle errors in data transmissions and to handle errors and faults caused by power transients and hardware failures. This includes how the terminal responds to an error and how the BC handles the error condition. The BC and its associated executive software are responsible for the management of errors on the bus.

The 1553 data bus, with its prescribed protocol and hardware characteristics, provides extensive transmission error detection capability, but the standard leaves the selection of the remedial action, upon error detection, to the system designer. The 1553B requirements applicable to this discussion are:

1553B requirement	Topic
Para. 4.4.1.1	Terminal word validation
Para. 4.4.1.2	Terminal transmission continuity
Para. 4.4.3.1	RT operation: acceptance of commands
Para. 4.4.3.3	RT operation: rejection of commands
Para. 4.4.3.4	RT operation: rejection of commands
Para. 4.4.3.6	RT operation: suppression of status word after invalid data reception

Determining the requirement for response to a detected error is difficult, and there are no generally accepted guidelines for performing error analysis and handling. In this area, 1553 offers no guidance. Errors and failures can be grouped into reasonably exclusive classifications. These classifications are discussed in 60.3.4.1 through 60.3.4.4, following, which provide guidance on the implications of responses to detected failures.

60.3.4.1 BC receives no status response. There are several error conditions under which an RT will not transmit a status word in response to a command from the BC: invalid commands, invalid data reception and, a subtler one, invalid message formats. The BC also may not recognize a status word which was correctly transmitted by an RT, and then distorted by the transmission media or incorrectly interpreted by the BC interface. A retry or bus switch will generally correct this situation. There is also no status response to a broadcast command, but that is not an error condition.

a. **Invalid commands-** Paragraph 4.4.3.3 of 1553B states that a command is invalid when it fails to meet the criteria specified by paragraph 4.4.3.1 of the standard. Because the command word is the key to the operation of the command-response data bus, the entire command word must be validated by a terminal before it takes any action. If the terminal determines that the command is invalid, it will reset its command decode circuitry and wait for the next command addressed to it. The status response will not be sent, and no error indications will be set in the terminal. The BC will detect a no status word response condition. The system designer may require that the bus controller retry the message on the same or on the alternate data bus.

b. **Invalid data reception-** Paragraph 4.4.3.6 of 1553B states that "any data words associated with a valid receive command that does not meet the criteria specified in 4.4.1.1 and 4.4.1.2 or an error in the data word count will cause the remote terminal to set the message error bit in the status word to a logic one and suppress the transmission of the status word." Because this could be a transient condition the system designer may require that the BC retry the message on the same or on the alternate data bus.

c. **Invalid message formats-** Paragraph 4.3.3.6 of the 1553B defines the valid message formats, and any other format received by an RT is considered to be invalid and results in a no response. Examples are: (1) a data word contiguous with a transmit command, and (2) during an RT to Retransfer, if the receiving RT detects that the transmitting RTs status word has a data sync.

If the BC cannot establish communications with the terminal, it could remove the terminal from the message stack or list or could continue trying periodic communications with the terminal. The BC could assume that the terminal is either powered off and might be powered on, or that a malfunctioning terminal might recover communications capability.

60.3.4.2 Illegal coremands. Paragraph 4.4.3.4 of 1553B states that 'an illegal command is a valid command as specified in paragraph 4.4.3.1 ." However, the command word indicates a mode command, subaddress or word count that is not implemented in the terminal. RT designers have the option of adding or not adding to their terminal illegal command recognition capability, called illegal command monitoring in the standard. Most RTs do not implement illegal command monitoring due to the complexity of the circuitry required.

A RT designed to detect illegal commands will respond as follows. When the RT detects an illegal command with the correct number of valid data words following it, the RT is required to set the message error bit in its status word, transmit the status word only, and not use the data received. In a mature system, the safest thing for the BC to do is increment an error counter and continue normal communications. if the error condition continues for a single terminal, the problem is likely the terminal. If the error condition occurs on both buses and with several terminals, the problem may be with the BC, and switchover to the backup bus controller may be required. Other mechanisms such as minor frame overflow or lack of required messages between the BC and backup BC will usually cause a switchover to the backup BC.

A RT not designed to detect illegal commands is required to "respond in form". In other words, the terminal responds to the command, and receives or transmits data just as if the command was implemented in the terminal. A prudent design should direct data received with nonimplemented subaddresses to unused receive data buffers so as not to corrupt other data buffers. Also, such a design should transmit data asked for in nonimplemented subaddresses from unused transmit data buffers.

60.3.4.3 Nonimplemented mode codes. Paragraph 4.3.3 .5.1.7 and table I of 1553B define the mode codes. Table I also identifies the reserved mode codes. The resewed mode codes and any mode codes not implemented in a RT are nonimplemented mode codes (mode commands). The receipt of a valid, nonimplemented mode command by a RT must be treated as an illegal command reception, and processed as described in paragraph 60.3.4.2, above.

60.3.4.4 Status word bits set. Paragraph 4.3.3.5.3 of 1553B defines a status word, a word that plays an important part in the command-response protocol. When the BC receives a status word from the RT, the BC knows that the previous transmission was received. Suppression of the status word indicates non-receipt of the command by the RT or receipt of an invalid command, invalid data, or a broadcast message. Typical actions taken if particular status bits are set in the status word received by the BC include:

a. Message error bit-Note that this bit will only be seen if an illegal command was detected by a RT that implements illegal command monitoring, or a suppressed status word was retrieved by use of a mode command. Refer to 60.3.4.2 for the suggested response to a message error bit set by an illegal command. For the case where the status word retrieved by use of a mode command indicates a message error on the previous message, the system designer must specify the appropriate follow-up response. Generally,

automatic retry of messages will have corrected the problem before mode commands were used. In cases where automatic retry is not allowed or prudent, the message error bit will indicate that the data were not properly received, so they can be retransmitted.

b. **Service request bit—** The service request bit set in a status word does not indicate an error condition. The BC must know or must determine the service that the terminal needs. If there is only one message for that terminal associated with the service request bit, then the controller will know what action is required. If there are multiple messages or actions that a terminal can request, the controller could use the transmit vector word mode command. The contents of the vector word usually define the action requested by the terminal.

c. Busy bit- Notice 2 of 15536 discourages the existence of busy conditions in RTs or the associated subsystem(s) interface. Predefine conditions could exist during which a RT goes busy for a determinate length of time. If the BC detects the busy bit set in a status word, it generally responds in one of three ways: (1) it can retry the message right away, (2) it can wait a period of time based on knowledge of the particular RTs busy conditions and then retry, or (3) it can continue with its other communications and try the RT later. In a mature system, the conditions under which each RT goes busy and for how long it remains busy are determined during system integration and testing. Therefore, if a terminal goes busy for an unusual length of time or under unusual conditions, it indicates a possible fault in the RT or associated subsystem.

d. **Subsystem flag-** Presence of this bit in the status word indicates a fault within the subsystem associated with the RT. Because mode commands cannot be used to obtain information from the subsystem, data messages would have to be used to obtain subsystem status and health via built in test (BIT), if possible. The BC host processor could then use an application software task to determine the problem and possible corrective action. Subsystem self-test, reset, or reload are possible actions. If the subsystem cannot be recovered, a redundant subsystem could be used if available.

e. **Terminal flag-** If the terminal flag is set in a status word, then a fault exists in the RT. The BC can determine the ability of the RT to communicate either through normal message traffic, by using wraparound messages, or by using mode commands to reset the RT or command self-test of the RT and examine the RT BIT word. The BC host processor could then determine the problem and possible corrective action. If the RT cannot be recovered, then a redundant RT and subsystem could be used if available.

A partial failure of the RT could also set the terminal flag. All dual-redundant 15536 terminals must have some level of redundant circuitry (at least from the bus cable through the address decode circuitry to meet the superseding command on the alternate bus requirement), so the terminal flag could indicate a problem in this redundant circuitry that affects only one path. If the status word is received and the bit is set, then the fault could be in the other path. If the error occurs on only one bus cable, then the BC might attempt to communicate with the RT over the good path. The controller could use the inhibit terminal flag mode command to turn off the terminal fail (TF) bit in the RT, or the BC could mask out the TF bit in its status word register. Another option is that the RT not set the TF bit for single bus faults, but only set the TF bit for failures that affect total RT operation.

60.3.5 Bus control mechanization. The topics concerning bus control mechanization to be discussed below are bus control terminal capability, bus control schemes, backup bus control, and bus control software.

60.3.5.1 Bus control terminal capability. BCs can be defined by the function of the control or protocol logic they are designed to implement. Bus control protocols can be divided into three categories: word processors, single-message processors, and multiple-message processors. Each is summarized as follows:

Word **processors.** Word processors are the simplest form of BCs, in that each word of the message to be transmitted or received is under control of the subsystem processor. Predominant in the earlier days of 1553, this type of BC was designed as an I/O channel to the host computer. Each word to be transmitted had to be

placed into an output buffer by the processor and every data and status word received had to be read from an input buffer by the processor. Each status word then had to be analyzed in software. Typically, after message initialization, the processing of the data and status words was handled via an interrupt service routine. Depending on the amount of data bus traffic, the subsystem processor could experience as much as a 20% reduction in throughput due to the heavy time demands of the 1553 I/O channel.

Single-message controllers. Using a command word set, single-message controllers process each message, one at a time, interrupting the subsystem processor at the completion of the message or on detection of an error (typically no response or message error). Initiation of the message requires the subsystem processor to setup pointers in memory or registers within the controller that point to the location of the command to be output and to control such information as which bus to issue the command on. All words transmitted, including the command word, must be formatted by the subsystem processor. The BC will then output the command and associated data (receive command) and receive the status word and associated data (transmit command) via DMA transfers to shared memory. On completion of the message or detection of an error, the subsystem processor is interrupted. The subsystem processor must then interpret the contents of the received status word and set up the associated pointers so the protocol logic can issue the next command.

Multiple-message controllers. Multiple-message controllers attempt to "off-load" the subsystem processor to the greatest extent possible. These controllers are capable of chaining messages to form minor or even major frame message lists. Some multiple message controllers are also intelligent enough to interpret status word contents, perform exception chaining, and provide automatic retry transmission on detection of an error. Initialization of this type of controller typically consists of setting address pointers to the starting address of the message list and defining interrupt conditions (what the subsystem processor must be interrupted for).

60.3.5.2 Bus control schemes. The bus control function encompasses the terminal hardware and software required to provide for the integration of the information flow over a MIL-STD-1553B multiplex data bus. This makes the capability and flexibility of the BC critical to the design, development, and future growth of the system. BCs almost always have the capability to be an RT, and sometimes they may also have monitor capability. A unit may be the BC for one bus and be an RT on one or more other buses.

It is most common for buses to have a BC and a backup BC (BBC). However, the standard does not mandate this. An alternative provided in the standard is dynamic bus control, that is, where the BC function moves among a designated group of units. The two control approaches, fixed bus control and dynamic bus control are discussed in the following paragraphs.

Fixed bus control. The fixed bus control concept is used when a single BC orchestrates the bus communication for all devices on that data path. Only in the event of a failure of the BC hardware or software will another BC (BBC) operate the data bus. As discussed in 60.1, multiple stationary master BCs can exist within a system, each controlling its own data bus.

Dynamic bus control. The dynamic bus control concept is used when multiple (more than one) BCs orchestrate the bus communication for devices on a single data path. MIL-STD-1553B provides a method of transferring control from an active BC to a potential BC (dynamic bus control mode code). This mode code provides a protocol for issuing the BC offer with the responding status word providing an acceptance or rejection of the offer. Because the standard prevents the operation of multiple BCs simultaneously, a method must be established to determine when the above mode code is to be issued and to whom it should be offered. The development of the timing (when) and the ordering (how the selection is achieved) are not specified by the standard and must be established by the system design. The following are methods that have been used.

Round robin. The round robin concept uses a fixed listing of BC operational order and usually a fixed maximum operating time for each BC. If this maximum operating time is maintained by each BC, a degree of system synchronization is maintained. Using this approach, each potential BC will control the bus during a minor cycle

(maximum update rate). Equal time for each potential BC is not a requirement.

Depending on the application and the minor cycle message traffic, a potential BC may require varying bus capacity each time it is in control within a major cycle (minimum update rate). The system engineer should exercise care in this area if user subsystems require synchronous operation. Subsystem synchronization can be maintained under this approach by broadcasting a master clock signal to all users from a single source at a periodic rate. If fixed minimum times are established for each potential BC and some potential BCs have no traffic during some minor cycles, bus bandwidth will be allocated but unused. This will lower data bus efficiency.

Analysis of round robin bus control has shown that subsystem data latency is impacted significantly as the number of potential BCs increase. Therefore, the advantages inherent in the relative simplicity of round robin bus control must be contrasted with potential system performance penalties (e.g., efficiency and data latency) for applications using many bus controllers.

Polling. This is the method of polling potential controllers to establish which controller has the greatest need to control the data bus (i.e., a priority message to transmit). This process is more complex than the round robin bus control transfer, and the performance impacts (e.g., efficiency) can be more significant. Because selection of priority is achieved, data latency can be improved and, if several terminals collect data asynchronously, data transfer requirements could diminish. As in the round robin scheme, once the new controller establishes control, performance is identical to the stationary master bus control approach.

60.3.5.3 Backup bus control. Failure of a RT will likely cause degraded operation, but failure of a BC will cause loss of the entire bus. Therefore, almost all systems have a backup unit to act as the BC if the designated BC fails. It is called the backup BC (BBC). The system issues of backup bus control require the following considerations:

a. Is full operational capability required after failure of the BC or is degraded system operation acceptable?

b. How is the BBC notified that it is to become the BC?

c. How is the designated BBC kept up to date so that it can function as the BC?

d. Does the BBC need to be kept current (because it is a hot backup), or can it start from scratch upon takeover of bus control?

e. Is more than one BBC required?

Backup bus control redundancy. If the BBC is an identical unit to the BC, if there is one identical redundant BBC unit for each BC, and if the BBC program load and data are identical to those in the BC, then use of the BBC depends only on the switchover. (Bus control switchover is discussed next.) Such massive redundancy will be unlikely in systems having multiple buses simply because the production hardware cost, including penalties for space, power, fuel, etc., point to other solutions. In place of massive redundancy, the designer should consider: (1) a multipurpose BBC that can act as BC on more than one bus, (2) system partitioning that tolerates the loss of one bus in a multiple bus system, or (3) the use of existing ‘intelligent” RTs as BBCs, possibly operating the system in degraded mode. Discussion of each of these alternatives follows.

If massive redundancy of the BC is not used, the system will likely be more complex. Even this case maybe simplified if the hardware unit of the multipurpose BBC and the BCs for which it is a backup are identical. Still, it remains a system problem of how to load the correct program and data in a timely manner. Approaches that may be considered are (1) continue operation of the system in a temporarily degraded mode until program and data are loaded or (2) maintain all the programs and data in the BBC. Typically, the system consequence of multipurpose BBCs is temporarily degraded operation.

If systems are partitioned functionally, the loss of a bus may mean the loss (or partial loss) of a function. If

the function is vehicle management, the backup maybe mechanical. If the function is maintenance recording, operation without a backup is likely to be tolerated. If the function is a dedicated MIL-STD-1760 stores bus, normal use of stores on that bus maybe lost.

The likely consequence of using an intelligent RT/BC as the BBC is increased complexity in software. To reduce the complexity, simplification should be considered, especially taking into account that a degraded mode may have been selected. If the intelligent RT/BC, operating as BBC, only provides a degraded system mode, then a simple, unvarying message transfer sequence and simplified error handling maybe designed for it.

Bus control switchover. The key to successful backup BC design and implementation is the ability to meet the following criteria:

a. Primary BC recognizes internal failures and ceases operation.

b. Backup BC recognizes the failure of primary controller and initiates action to take over control.

The procedures by which the backup BC takes over the bus need to be defined. The simplest approach is to use dedicated discretes with a watchdog timer between the two controllers. The primary BC must signal the backup BC periodically, indicating that is is still in control of the bus and is in good health. This requires the primary BC to perform internal self-tests. Another method is for the backup BC to monitor the data bus for dead time or the lack of a specific "keep alive" message. If the data bus is dead for a given period of time or number of minor cycles, then the backup controller takes over.

60.3.5.4 Bus control software. The system designer must be aware of the capabilities of the BC hardware. The software will be written to use these capabilities. Specifically, the designer should catalog the capabilities of several candidate hardware designs. Key issues are what features are user programmable (e.g., retry, which bus pair, status bit masking, message linking, exception handling, and error monitoring and logging), and at what level are they programmable (i.e., system, terminal, or individual message).

The bus control terminal is usually a programmable device, with the contents of registers as the medium by which control and status are passed between the BC terminal and its host processor. Therefore, the software must be written to use these programmable features. More importantly, the multiplex system design must be consistent with the programmability of the terminal. For example, a programmable BC terminal could interpret status words by their RT address, allowing otherwise incompatible terminals to be used on the same bus. Also, programmable terminals usually require a portion of shared main memory.

Usually the BC passes bus message data to and from the shared memory using direct memory access (DMA) hardware. The BC should have higher DMA priority than the central processing unit to maintain continuity of data bus message traffic. Bus control software is what implements system use of the autonomous and semiautonomous features of BC hardware. The BC design example in 50.8.6 should be read for additional guidance on the requirements of bus control software.

60.4 SYSTEM GROWTH PROVISIONS. During the life of a system, modifications will be made to it. Subsystems will be added, old subsystems will be replaced with new technology or more capable subsystems, and the overall multiplex system will grow and change. Consideration must be given during the design of the system to allow for this growth. Key areas for consideration are multiplex system topology, data bus loading, and BC growth capability.

60.4.1 Multiplex system topology. Data bus topology is the map of physical connections of the data bus terminals to the data bus. It includes all terminals and data buses involved in the data bus integration of the system. Items that affect the system topology growth capability include the length of the bus cable, number of terminals, and length of stubs. A maximum main bus length is not specified in 1553B because the cable length, number of terminals, and lengths of stubs must be considered in the design for reliable system

operation.

60.4.1.1 Bus lenght. A maximum cable length of 300 ft, including stub lengths, was specified by 1553A. However, 1553B does not specify a bus length and allows the system designer to optimize the bus network design by using all network parameters. The system designers should determine by analysis and simulation if the bus, stub, and terminal configuration is approaching a point at which unacceptable waveform distortion will occur. If so, then a second bus should be considered to allow for growth. See section 40 for guidance in this area.

60.4.l.2 Number of terminals. Thirty-one unique terminal addresses are allowed by 1553B, with the limiting factors being the five-bit address field and the reserved address for broadcast. The actual number of terminals on the bus maybe greater than 31 because the BC and any BBCs may not be assigned a terminal address, and an unspecified number of monitors maybe present.

The actual number of terminals allowed in a given system depends on the bus, stub, and terminal configuration and is limited by the electrical parameters required by 1553B. Some system designers prefer not to number the terminals consecutively. This particularly applies to terminals that have stores attached. This practice reduces the number of available addresses even further.

The designer should evaluate the possible growth of the system. System growth and upgrade plans may already include subsystems to be added in the future. If planned growth would nearly fill the bus, then another bus should be added. Some techniques that allow for system growth are (1) limit the number of terminals per bus in a new design, (2) provide bus control units with the capability to handle additional buses in the future, and (3) install spare bus cables in the vehicle when it is built because retrofit installation of bus cables is costly and difficult.

60.4.1.3 Length of stubs. Direct-coupled stubs (less than 1 ft) and transformer-coupled stubs (1 to 20 ft) are allowed by 1553B. Without stubs, the bus looks like an infinite transmission line with no reflections to distort the signal. As stubs are added, the bus is loaded and an impedance mismatch occurs, with consequent waveform distortion. The number of stubs, their lengths, and their placement are very important. Analysis and simulation should be conducted to determine the optimum bus/tub geometry to accommodate additional stubs resulting from future system growth. See section 40 for additional discussion.

60.4.2 Bus loading. Bus loading is the percent utilization of the total information transfer capacity of a multiplexed data bus. The maximum information transfer capacity of a 1553 data bus, stated in words per second, is 50,000 20-bit words per second. However, a practical upper limit is about 40,000 words per second or 80% maximum bus loading (see paragraph 60.2.3.1 for calculation). Above this limit bus control timing becomes increasingly critical. Therefore, if a data bus analysis shows that the bus is 60% to 70% loaded, consideration should be given to adding a second data bus.

60.4.3 BC growth capability. Two important areas of BC growth capability are spare processing and multiprotocol handling capability.

The unit that contains the processor and BC hardware, and provides the multiplex system control for a bus, could include the capability for adding additional BCs. This would support growth of the system. The effect of bus control demands on the processor throughput, and the effect of any growth BCs, should be included when sizing the processor.

Bus control hardware and multiplex control software should be designed to accommodate the different protocol options within the version of the standard to which the system is designed. The basic 1553 protocol options are message transfer formats, status bits, and mode commands. The protocol options are discussed in 60.3.1. A desirable characteristic of the bus control function is that it be able to handle differences in protocol option implementation on a terminal-by-terminal basis. This characteristic becomes increasingly important if the system includes a mixture of terminals built to different versions of, or notices to, the standard. A

multiprotocol BC could recognize terminals with different capabilities, or terminals designed to different versions or notices of the standard, and handle each correctly.

60.5 SYSTEM VALIDATION System validation includes hardware and software qualification, system integration testing in laboratories, on-vehicle testing, and initial operational test and evaluation (IOT&E). There are some avionic integration design activities that are also supported by laboratory tests (e.g., bus network modeling). Tests of the 1553 vehicle data bus system will take place(1) at the facilities of suppliers of units with 1553 interfaces, (2) at a system integration laboratory, and (3) during ground and operational test of the vehicle. Note that new contracts for 1553 system development may require that the system pass the SAE developed System Test Plan (SAE AS4115). Refer to Section 110 for a listing of the SAE test plans and their availability. The purpose of this section is to briefly describe hardware, test procedures, and test philosophy of the various levels of testing required to validate the multiplex part of vehicle systems.

60.5.1 Scope Of tests. A vehicle multiplex system is validated when all of the following test activities have been successful:

a. RT and BC validation.

b. Development tests of the integration of RT and BC in subsystems.

c. Unit and subsystem qualification.

d. System integration tests.

e. Initial operational test and evaluation (IOT&E) and operational test and evaluation (OT&E).

60.5.1.1 RT and BC validation. The final criterion of RT and BC validation is successful completion of the tests defined in the RT and BC validation test plans. In all new systems and significant updating of existing systems, it is expected that completion of tests defined in the RT and BC validation test plans will be a contract requirement. Therefore, program and test managers should make provision for these tests early in the full scale engineering development (FSED) phase. Refer to the RT validation test plan in section 100 and the listing of other test plans, including the BC validation test plan, in section 110.

60.5.1.2 Subsystem interface tests. Although these tests may be conducted in the same facility and concurrently with RT and BC validation, many vehicle integration requirements must be validated early in FSED. It is necessary to prove by tests that the subsystem interface meets system performance requirements. Examples of multiplex-related problems found in this phase of testing include: (1) wrong data in response from a particular subaddress, (2) inability of the RT and subsystem to respond in a timely manner to BC requests for data resulting in either the busy bit set in the status word or stale data sent, and (3) inability of a BC to transmit the next message in a chain within specification time.

60.5.1.3 Unit and subsystem qualification. It is often true that parts, materials, and processes that are required for production equipment will alter unit or subsystem responses established by development tests because of changes made during the qualification process. Therefore, these qualification tests must be audited to track the impact of design changes during qualification on system multiplexing performance. Problems encountered are more likely to be related to electrical performance than to software performance.

60.5.1.4 System integration tests. Thes tests are frequently done initially with production prototype hardware, both in system integration laboratories and in vehicle-on-ground and flight tests. These tests are also initially done with immature simulators and incomplete operational software. As tests progress and initial hardware and software are replaced with fully qualified units, simulated operational tests may expose additional multiplex-related problems. Examples of these include: (1) minor frame overrun, (2) unanticipated data latency, (3) incomplete error handling, and (4) improper system synchronization. Program and test

managers should make provision for instrumentation, data recording, and analysis to support anomaly resolution.

60.5.1.5 initial operational test and evaluation (IOT&E) and operational test and evaluation (OT&E). These tests are aimed at proving weapon system capability in an operational environment as much as practicable. Examples of multiplex-related problems found in this phase include: (1) improper operation caused by hardware-related quality such as intermittent connections and (2) operator-reported anomalies, including such things as a complete system shutdown. These problems are usually accompanied by very minimal descriptions. Managers must realize that instrumentation used in system integration will be required to isolate such problems.

60.5.2 Bus development support, and test equipment. This paragraph provides an introduction to the capabilities of various types of 1553 support equipment, their uses, as well as other techniques used in system integration and testing.

Multiplex support equipment has come a long way since the introduction of the SEAFAC Bus Tester Four in 1980. The proliferation and variety of support equipment is a contributing factor in the continued success of 1553 based avionics. The use of 1553 test equipment is indispensable in any and all 1553 development programs. The overall success or failure of a given 1553 development program can often be traced to inadequate or poorly applied development tools. Even with the proliferation of ready made 1553 components and interfaces, there is no substitute for a good high quality bus analyzer/tester.

MIL-STD-1553 support equipment falls into four main categories: 1553 terminal design support, 1553 terminal validation test systems, production test systems, and avionics integration support systems.

MiL-STD-1553 terminal design support. This category of equipment makes up the majority of 1553 test equipment on the market today. They range from simple hand held or “card in computer” based stimulators and testers to fairly sophisticated 1553 logic analyzers. The price range of this type of support equipment is as varied as the capabilities of the equipment. Cost effectiveness is generally the key factor in choosing a particular analyzer/tester for design support. A lower cost tester will have fewer features, which often translates into longer development time. A low cost tester maybe adequate for basic terminal design, but inadequate for integrating software with the terminal hardware.

As a minimum, terminal design support equipment should have the ability to monitor and store bus traffic on a dual redundant bus. The monitor should provide visual indication of command data and status words captured, and some indication of gap and status response timing. The monitor would have the ability to indicate basic bit and protocol errors. The detail of the error analysis and reporting capabilities of an analyzer become a major consideration if the analyzer is also to be used in a terminal validation system.

Simulation of remote terminal, and bus controller functions with a static data set is another important feature. Single remote terminal simulation is adequate, but multiple remote terminal simulation provides a more realistic RT development environment, and is mandatory for BC development. Programmable intermessage gap time, transmission rates, response times, and bit and protocol error injection capabilities are necessary to determine worst-case performance of a terminal, and are a must if the analyzer/tester is to be used for terminal validation.

The “buy the lowest cost tester” attitude can lead to spending more to use the poorly designed terminals which may result. Ease of use (user friendliness) tends to be the first ‘luxury” item to be sacrificed when the cost of an analyzer/tester becomes the driving issue. Then error injection and terminal simulation capability would go. Tester documentation and support would also be sacrificed. Terminal designs tend to be very late when the designer is spending time deciphering documentation, developing software to drive the tester, or the tester is down for repair.

MIL-STD-1553 validation test systems. Validation test systems are typically enhancements made to the

mid-to-high performance development analyzers/testers. Frequently the only enhancements necessary to perform terminal protocol validation using many of the analyzers/testers on the market, are specialized software programs which can be purchased as part of the basic system or as upgrades. Electrical terminal validation systems typically require additional hardware to implement the electrical validation requirements. At this writing there are several companies offering packages which are suppossed to satisfy both the protocol and electrical RT validation requirements being specified in current Air Force procurement contracts. The key to compliance for a contract using any validation system will be acceptance and approval by the individual Air Force program office. Section 100 of this handbook (RT Validation Test Plan) covers the requirements for validating a 1553 RT.

Production test systems. Terminal production testing is not concerned with design verification and validation, but with assuring that 'all the components in a given terminal are operating as specified". The key to a terminal production test system is the capability to functionally test a terminal, ensuring all components are tested for proper operation within the limits of their design specifications, in the shortest possible time. Test systems designed for this purpose typically give go or no/go indications only, are host computer controlled, often PC based, and maybe configured to test a single terminal or multiple terminals at the same time. The practical level of production testing lies somewhere between a full electrical and protocol validation test and a basic functional test of the terminal. The ideal system would perform full electrical and protocol validation testing on each terminal; which is probably not practical from a production line standpoint. The production testing must ensure that all of the components of the terminal are operating within the design parameters validated by the terminal validation testing. The overall terminal design and associated software controls do not change from terminal to terminal (if properly validated), and the requirement for complete validation testing is not needed. If the terminal or software design is changed, then full validation re-testing is required.

Avionics integration support systems. These can take on many different forms depending on the integration task. Complex integration tasks using multiple 1553 buses are rarely satisfied with a single piece of test equipment, and have for the most part been accomplished using a variety of in house designed "special test equipment". The systems integrator is more concerned with actual information or data exchange over the buses, leaving actual bus testing to the terminal designer.

The test equipment requirements for 1553 systems integration become very different from the requirements for the terminal designer, although a good 1553 test system is still a must. The systems integrator's support requirements have been driven by a number of factors not easily served by 'off the shelf" test equipment. Test systems with the capability to stimulate the system with actual or simulated data in real time or near realtime and high speed monitor systems have become the integrators "tools". The ability to provide realistic simulation and analysis of functions in a system or subsystem requires very fast and complex support devices. Typically, integration support systems have been designed around, and at the same time as the actual operational hardware; with the ability to replace simulated functions with operational hardware as available. Flexibility in many cases has had to take, a back seat to the specific test requirements. Thus an integration system has tended to be an assortment of specialized testers and test software.

As 1553 avionics has matured, so has the support equipment. There are "off the shelf" systems that will allow a building block approach to system integration support equipment. These systems now address system timing requirements, multiple buses, and real time bus data storage. They are flexible enough to be used in various integration scenarios, with elements that are easily transportable for use in production test and flight test environments. What type a system is best depends on the complexity of the integration task. For small integration tasks the current crop of tester/analyzers may be adequate but difficult to use. Most data bus oriented testers present data in a rather rudimentary manner; much like using a memory dump to debug a Fortran program. Integration oriented analyzers perform engineering unit conversion and analyses, and their displays and graphics to present **a** more meaningful picture of data bus activity. Static, or low rate of change, data simulation may be adequate for small integration tasks, but real time data simulation is needed for complex systems integration. Multiple bus integration efforts require some form of time reference, both for simulation and analysis. Flight test monitoring systems use a global time reference or range time Interrange Instrumentation Group (IRIG) to synchronize multiple flight data inputs that must be recorded and analyzed.

This global timing technique is very useful for multiple 1553 bus data acquisition and analysis, and is provided by some of the higher performance analyzers.

60.5.3 System test techniques.

60.5.3.1 Avionic hot bench. A 'hot bench" is a commonly used term to describe a system development laboratory (SDL) or system integration laboratory (SIL). Such SILs or SDLs provide simulation and data recording capabilities that are used in developing vehicle hardware and software. To allow for incremental testing of avionic interfaces, simulators are used for such subsystems as the radar or stores.

The simulators provide realistic inputs and responses so that dynamic conditions maybe evaluated in the laboratory. This is in contrast to the capability of bench or suitcase testers, which usually can simulate only a limited set of commands and responses. The simulators in hot benches area substitute for unavailable hardware, and an intermixing of prototype or production airplane hardware with simulators is usually possible. By this means, vehicle hardware can be added incrementally to an avionic system. Whenever the interface is the 1553 data bus, rapid substitution of the simulator for the airplane hardware permits the isolation of problems or anomalies.

Several benefits of integration with 1553 data buses become apparent during system test. The data bus approach requires integrating only one electrical interface per subsystem versus multiple interfaces in the point-to-point method. The single interface also allows more of the integration activity to be done at the subsystem level using one special test fixture, which might be too costly with many unique point-to-point interfaces. The data bus interface of subsystems can easily be simulated using a computer with a data bus interface as the simulator. The equivalent simulation in a point-to-point architecture may require several special-purpose interfaces to be developed. The data bus will also accommodate unexpected integration problems such as added data words, changes in update rates, and rerouting of data parameters.

60.5.3.2 Bus monitor and airborne instrumentation. System designers should make provision for the connection of a bus monitor (BM) and avionic instrumentation capability. Provision will usually be a stub or connection, properly terminated when not in use, on prototype and test airplanes. With this connection available, a BM may be used during flight testing to acquire selected bus messages. Recall that 1553B, paragraph 4.4.4, specifies BM operation as follows:

> **4.4.4 Bus monitor operation. A terminal operating as a bus monitor shall receive bus traffic and extract selected information. While operating as a bus monitor, the terminal shall not respond to any message except one containing Its own unique address if one is assigned. All information obtained while acting as a bus monitor shall be strictly used for off-llne applications (e.g., flight test recording, maintenance recording or mission analysis) or to provide the back-up bus controller sufficient information to takeover as the bus controller.**

BMs are usually implemented using a digital computer, appropriate memory for buffering, and bulk memory media for storage. Several suppliers manufacture BMs and airborne instrumentation that are qualified for flight test.

Merely recording bus traffic has been inadequate in system integration. Many intermediate values of data needed for performance evaluation and analysis are never transmitted on the data bus. A valuable technique to overcome this has been termed the data 'pump," which consists of messages transmitted on the bus for recording by the BM. Such messages are created by the applications software and the software executive. (These messages remain in the operationally deployed weapon system because system and performance validation occurred with them present).

60.6 INTEGRATION INCOMPATIBILITIES AMONG SUBSYSTEMS. New multiplexed electronic systems are rarely designed with all-new subsystem units built to a single multiplex specification. Multiplex system design must accommodate a combination of subsystems with new 1553 interfaces specified by the system

designer, Government-furnished equipment (GFE), and off-the-shelf equipment from vendors. The integration of units with diverse 1553 characteristics and capabilities, perhaps built to different versions and notices of the standard, involves analyzing the compatibilities and incompatibilities among the selected and required subsystem units. In the following paragraphs, 1553 protocol and other multiplex interface design factors that can cause incompatibilities in a system are discussed. For 1553 electrical incompatibility handling, refer to sections 40 and 50.

60.6.1 Protocol. The specification of protocol options for new units in a system and the reconciling of differences between new units and existing units can lead to two different design philosophies. The capabilities of all the units can be compared and the lowest common denominator of capability accepted as the multiplex system control level implemented. Alternately, the multiplex system control can be designed to use the maximum capability of each unit. The first approach is possibly lower in cost but is lower incapability. It wastes many features already built into some units and paid for. The second approach maybe higher in nonrecurring engineering costs but may be lower on a per-unit cost basis. It does take advantage of the features in each unit and potentially offers higher system availability.

The main areas of protocol incompatibility are in command word interpretation, status word implementation, mode code implementation, information transfer format implementations, and subsystem data requirements and rates.

60.6.1.1 Command word interpretation. Command word interpretation in the areas of addresses, subaddresses, and mode indicator can cause incompatibilities.

Addresses. The system designer may be faced with restriction in address selection due to reserved addresses, restricted use of addresses, or units with internally hardwired or hard coded addresses. The standard allows 32 possible addresses. One address, decimal 31 (111 11), is reserved for broadcast. The remaining addresses could be digitally spaced to increase Hamming distance, especially between redundant resources. Addresses may be reserved for growth. Units built to versions of 1553 prior to 1553B Notice 2 may come with addresses internally set, either with jumpers or in firmware. The designer must resolve potential address assignment conflicts while providing adequate growth and, if possible, adequate address spacing.

Subaddresses. There area growing number of ways to implement subaddresses in a RT. There are also new uses for multiplexing that restrict subaddressing. Information about unique requirements for subaddressing use in terminals will be invaluable to the system engineer in defining the commands to be sent, any special synchronization or subaddress map loading or switching required, limited subaddress RTs, bulk data transfer requirements, and restricted use of subaddresses (e.g., MIL-STD-1760 requirements for reserved, dedicated, and nuclear subaddresses).

able to issue mode commands to equipment designed to 1553A requirements.

60.6.1.2 Status word implementation. The terminals selected for a system will often have different status word bit setting capabilities and will set and reset the status bits under different conditions. Eight functional status bits are defined in 1553B (see figure 60-9). Of the eight status bits, only the message error bit is required; the other seven are optional. Three of the remaining seven status bits are rarely implemented: instrumentation bit (always logic zero), broadcast command received bit, and dynamic bus control acceptance bit. The service request bit, busy bit, subsystem flag bit, and terminal flag bit are the remaining four status bits. Though optional, these bits are often implemented.

The BC and the multiplex system control software must implement status bit exception handling if any is required in the system. Status bit exception handling can either be done immediately upon occurrence (i.e., handle as many as possible of the exceptions in BC hardware and interrupt the processor to handle others), or on a deferred basis (i.e., queued).

The capability for handling status bit exceptions varies widely. The lowest level of capability is to handle no status bit exceptions and, optionally, to store the status word directly in host processor memory. An intermediate level capability is to handle only exceptions for those status bits implemented by all terminals in the system, that is, the lowest common denominator of terminal status reporting capability. A high level of status bit exception handling would handle both full and limited status reporting as well as status from terminals built to earlier versions of 1553. Note that a BC which communicates with both 1553B and 1553A RTs must either ignore status word exception bits or it must interpret 1553B status words and 1553A status words differently, with the exception of the TF bit which is in the same bit position and is set similarly in status words of both versions. The BC must also recognize that 1553A RTs implement the message error bit differently, although they are in the same bit position for both versions status word. The 1553A RT will transmit a status word with the message error bit set, in response to a message error, instead of setting the message error bit and suppressing the status word like a 1553B terminal will. The remaining 1553B status bits, and the 9 bit status code field in 1553A status words (which were a system designer option to define and are defined uniquely in every 1553A system where implemented) must be handled uniquely, if at all.

Status bit exception handling is used primarily for real-time error and fault identification. The primary tool for multiplex error identification is the suppression of status word transmission by a terminal. The basic error-correction technique consists of message retries by the BC. The primary tools for fault detection at the multiplex level are: (1) continuing lack of status response from a terminal, (2) failure of communication to several or all terminals on a single bus cable, (3) detection of subsystem flag or terminal flag bit set in a status word, (4) broadcast command received bit not set in a status word, and (5) the message error bit in a 1553A status word.

The system designer must determine the status word capability of each terminal and design BC and multiplex system control to implement a level of status word handling consistent with the cost and performance requirements of the system.

60.6.1.3 Mode command implementation. Before 1553B Notice 2, there were no required mode commands. Therefore, existing terminals may implement some, all, or no mode command handling capability. Notice 2 requires RTs to implement a minimum set of four mode commands (transmit status word, transmitter shutdown, override transmitter shutdown, and reset RT), and BCs to have the capability to implement all the mode commands. The system may be designed to use a common set of mode commands or to have knowledge of the capabilities of each terminal and handle each uniquely. The system may also be required to handle unique definitions of the data words associated with mode commands.

The usefulness of mode commands has been controversial. Generally, few mode commands have been implemented in 1553 systems. There has been reluctance for systems to determine errors and faults in real time using mode commands because it might jeopardize the periodicity of the system.

Existing systems have used mode commands to implement normal communications functions. Some

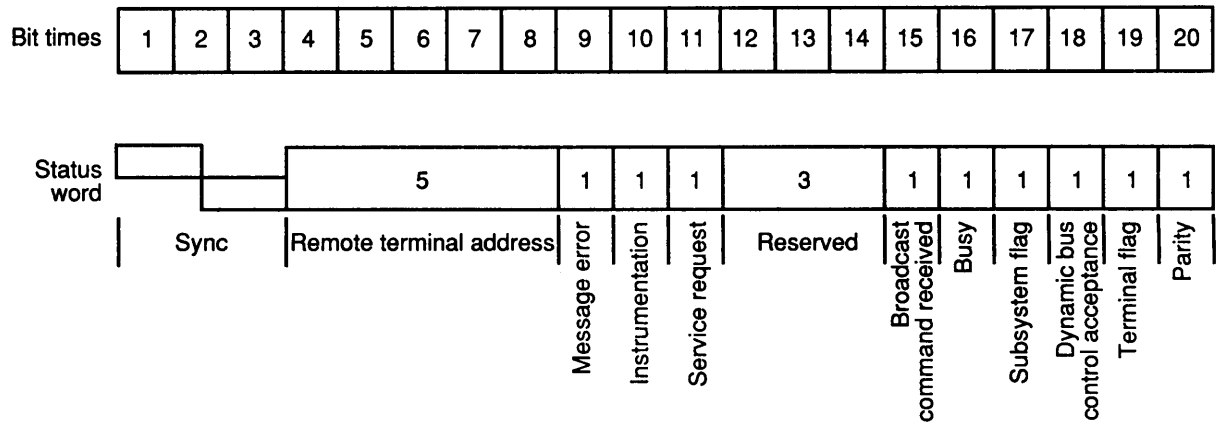


Figure 60-9. Status Word

systems periodically poll RTs to determine if they can still communicate or to look for service requests. The transmit status word mode command is typically used for these functions. Some systems use the transmit vector word mode command to retrieve data pertaining to a service request by an RT. Synchronize without data word and synchronize with data word are often used for minor and major cycle synchronization, clock synchronization, or subaddress map switching. The reset RT mode command was used by one system for periodic synchronization of its RTs.

The system designer must be aware of the way in which the data words associated with mode commands are implemented for existing terminals. The designer must also apply consistent requirements when designing new subsystems that use mode commands with the data word. Transmit vector word, synchronize with data word, and transmit BIT word mode commands are the most commonly used.

60.6.1.4 Information transfer format implementations. Two 1553B information transfer format implementation areas that differ among terminals are RT-to-RT message transfer capability and broadcast message handling.

RT-to-RTmessage transfer capability. The following are some characteristics of RT-to-RT implementation to be aware of when integrating existing terminals:

a. Some terminal designs do not implement RT to RT transfer capability.

b. Some systems have encountered problems implementing RT-to-RT messages as a result of having a mix of 1553A and 1553B units. The shorter 1553A response times have prevented RT-to-RT messages from being completed successfully from a 1553B unit to a 1553A unit, because the 1553A unit timed out before the 1553B unit responded.

c. Other terminals have been built with no time-out on RT-to-RT message reception, and may accept data from a following message. Notice 2, paragraph 30.9, established an RT-to-RTvalidation requirement with a time-out window to prevent reception of incorrect data.

Note that Notice 2, paragraph 30.9 recommends that the receiving RT validate the proper occurrence of the transmitting RT's command and status word. As a minimum, the RT must validate the proper message format; i.e., that the word following the receive command is a valid command word, and the word following the response gap is a valid word with a command sync (status word). The Notice 2 recommendation is that the receiving RT also compare the terminal address in the transmitter's command and status words. It maybe desirable for the RT or subsystem to look at the TF and SF bits in the transmitting RT's status word before the data is considered valid.

Broadcast message handling. There are differing broadcast implementation requirements inversions and notices of the standard. The broadcast information transfer formats option is defined in 15536 paragraph 4.3.3.6.7, but its use is discouraged in paragraph 10.6. Earlier versions of the standard did not define broadcast. For Air Force avionic applications, 15536 Notice 1 prohibited the broadcast of messages by the BC but allowed the incorporation of broadcast handling capability in RTs. Notice 2, paragraph 30.6, states that "The only broadcast commands allowed to be transmitted on the data bus by the BC shall be the broadcast mode commands identified in Table 1. The broadcast option may be implemented in RTs. However, if implemented, the RT shall be capable of distinguishing between a broadcast and a non-broadcast message to the same address for non-mode command messages." Also, paragraph 30.8 requires BCs to have the capability to issue all of the broadcast information transfer formats.

The system designer may anticipate finding different levels of broadcast handling capability in existing terminals and RT interface components. RTs built to 15536 or 15536 Notice 1 should either have full broadcast handling capability or none. Careful testing must be done with RTs that are supposed to have broadcast capability but have never been used in a system with broadcast. One RT design was found to recognize the broadcast address of 11111 and, instead of suppressing its status word, would respond with a status word containing its unique address. That design could not be used in a system using broadcast.

The Air Force is opposed to implementing broadcast in any of their internal avionics multiplex systems. There are many negatives to implementing broadcast in a system, but the most cited one is the lack of status word response after a broadcast command. This is a departure from the fundamental command-response nature of 1553. Other limitations of broadcast include: (1) a maximum of 30 broadcast subaddresses per system, (2) little portability of terminals with broadcast message receipt capability from one system to another due to potentially different interpretations that might exist for the same subaddress, and (3) the possibility of terminals accepting broadcast messages as nonbroadcast messages to the same subaddress.

The military and industry did agree in 15536 Notice 2 to allow use of broadcast mode commands in a system. Extreme care should be taken in implementing them, however. Some broadcast mode commands could be quite useful (i.e., broadcast synchronize with or without data word) to simultaneously synchronize a system's terminals. (Note that all terminals receiving a broadcast mode command must know how to properly use it internally or how to ignore it.) Other broadcast mode commands have the potential for great harm. An example is broadcast reset RT mode command. Different RT designs respond differently to the same mode command. Some terminals only perform harmless functions, like clearing registers or resetting timers, upon receipt of reset RT mode command; other terminals clear all RT programming and interrupt their host to be reinitialized. The purposeful or accidental transmission of the broadcast reset RT mode command in a system having any RTs that go to the state where they must be reinitialized by their subsystem can potentially cause havoc with the periodicity and state of a system. Periodic time synchronization, historical data, and subaddress maps are examples of data that could be cleared accidentally.

60.6.1.5 Subsystem data requirements and rates. The periodic and aperiodic data requirements and data handling capabilities of subsystems and their associated terminals must be analyzed to ensure meeting system performance requirements. Consistent specification of data requirements and data handling capabilities across all terminals and subsystems is desirable. If that is not possible, a system-level ability to handle diverse terminal and subsystem data requirements and data handling capabilities can be used to integrate a multiplex system.

Periodic data. Subsystems may require periodic data at different rates for different messages or at different rates from other subsystems. For example, one subsystem may expect to receive data at 50 Hz or submultiple and another subsystem at 64 Hz or submultiple. They may also require varying length data messages. Periodic time synchronization of terminal or subsystem, or time tagging of data maybe required. Subsystems have limitations on the rate at which they can prepare and send data, the rate at which they can receive and process data, the data resolution and formats required, and the resolution of computation and transmission formats. Terminal designs may limit the number of message buffers, subaddresses, and the ability to receive successive messages or retries.

Aperiodic data. Subsystems and their terminals may differ widely in their requirements for aperiodic data and their method of handling it. Aperiodic data includes both message transfers requested by a terminal and messages sent to a terminal on an irregular (i.e., event driven) basis. Subsystems may require no aperiodic messages, only one aperiodic message or many.

Methods for a terminal to communicate the request for aperiodic data differ. The terminal may set the service request bit in the status word or indicate in a data message that it needs servicing. The BC may know what service a terminal needs at a particular time, or it may require additional information. The BC may gain additional information by using the transmit vector word mode command, where the vector word retrieved from the terminal identifies the service needed, or the BC may ask for a data message identifying the service needed. Queuing of multiple service requests in a terminal may require the BC to send a handshake message to the terminal after service completion or for a message retry. This handshake could increment or decrement a pointer to the service request queue. Synchronize mode commands have been used to provide this handshake in some designs.

Event-driven data sent to terminals on an aperiodic basis mayor may not be critically timed. To reduce transmission time uncertainty, the aperiodic message could be sent by the BC at a time predetermined by the sending application. Doing this may interrupt or delay ongoing periodic message transfers and is almost impossible to implement at the precise time requested. Alternatively, the aperiodic message could be time stamped, either with the time of creation or the time of transmission, and inserted in the periodic message handling or queued for transmission after periodic message list completion.

60.6.2 Other factors. Other aspects of terminal and subsystem design may impact system integration. Defined conditions under which terminals can go off-line or busy must be taken into account in multiplex system control. For each terminal, any bulk data transfer requirements (see 60.3.3.5) as well as time synchronization requirements (see 60.2.3.2) must be considered.

Initialization, reset, and self-test are three RT conditions that can impact system operation. The multiplex system control must know when these conditions can occur for each terminal and for for how long the terminal can be off-line or busy. Unexpected terminal off-line or busy conditions can cause unnecessary message retries, declaration of terminals as failed and, as a result, system reconfiguration to a potentially degraded state. Too many retries will affect the periodic synchronization of the system. Premature declaration of terminals as failed will waste redundant system resources and degrade system performance.

60.7 SUMMARY OF INTEGRATION ACTIVITIES. This summary relates multiplex system design activities to a normal defense system acquisition and discusses multiplex system design as related to conceptual, validation, and full-scale development phases of a normal system acquisition.

The aircraft avionics of modern military airplanes must be viewed as an integrated system rather than a conglomerate of functional sensors, controls, and displays. The data bus integration method forces the system engineer to perform system-level analysis because defining information flow is the key element in the orderly integration process. When using the data bus concept, it is important to realize that software does most of the integrating. Therefore, the final and most critical integration step is performed by effective application of operational software (e.g., the software controls the real-time information flow). Therefore, to avoid schedule delays and cost overruns that may be associated with insufficient planning for software and computer systems, it is important that the critical technical decisions relating to data bus system integration be made in the phase that supports this intelligent planning.

If the military data bus standard (1 553) is to be effective, its definition in the program management directive and the program management plan is essential. The system acquisition life cycle provides a basis for categorizing program management activities. For Air Force systems, it consists of file major phases with major decision points as defined in AFR 800-2. Using this as a basic management approach, the following descriptions briefly explain a normal system acquisition with emphasis on multiplexing and computer resources. This discussion is adapted from AFR 800-14, Management of Computer Resources in Systems.

Conceptual phase. The conceptual phase is the initial planning period when the technical, military, and economic bases are established through comprehensive studies, experimental development, and concept evaluation. The objective of this initial planning may be directed toward refining proposed solutions or developing alternative concepts to satisfy a required operational capability.

During this phase, proposed solutions are refined or alternative concepts are developed using feasibility assessments, estimates (cost and schedule, intelligence, logistics, etc.), trade-offs, studies, and analyses.

The major definitive document resulting from this phase is the initial system specification, which documents total system performance requirements. It will document the requirements for integration (e.g., avionic sensors, crew displays, weapon delivery systems). The initial system specification will be used to establish the general nature of the system that is to be further defined during a contract definition activity. This specification will be the basis for the performance required of prime items and configuration items because overall system performance will be allocated to these items. It is to be expected that the following list of applicable requirements related to a data bus system would be included in the initial system specification:

a. A requirement stating that 1553B data buses will be used in the systems integration of aircraft subsystems.

b. Requirements for subsystems to be connected to the data buses, such as inertial navigation systems, fire control systems, crew displays, computers, and communications systems.

c. System-level redundancy requirements.

d. A description of the multiplex topology, including line drawings.

e. A description of the overall sensor and data bus system control approach.

The system specification may also document the requirements to be met by computer resources as well as relevant design constraints. An adequate definition of essential system interfaces between mission computer equipment functions, and personnel functions should be provided to enable the further definition and management of the computer programs and computer equipment into configuration items. Normally, this information is derived from system engineering studies of the system functions.

Validation phase. The validation phase is the period when major system characteristics are refined through studies, system engineering, preliminary equipment, computer program development, test, and evaluation. The objective is to validate the choice of alternatives and to provide the basis for determining whether or not to proceed into the next phase.

During this period, system performance requirements, including computer resources, are further defined. Also, preferred development methodologies for computer programs, such as organic or contractor (per AFR 26-1 2), are selected. Validation phase activities define the efforts (performance, cost, and schedule) required by system characteristics and provide confidence that risks have been resolved or minimized. Necessary technical reviews are the system requirements reviews and system design review.

For computer resources, there are three major definitive documents resulting from this phase: (1) the authenticated system specification, (2) the preliminary development specifications containing system functional requirements allocated to configuration items of computer programs and equipment, and (3) the initial computer resources integrated support plan (CRISP).

For the data bus system, the major definitive documents resulting from this phase are the same as for computer resources. The system specification should contain additional detail on the following:

a. Whether the data bus interface unit is standalone or part of the sensor unit.

b. Requirements for the growth of the data bus system, including expansion of the multiplex system topology, increases in bus loading, and growth capability in the BC.

c. Overall definition of all normal and error recovery data communications, identifying at least the source, destination, update rate, and nominal length of each message.

d. Definition of the applicable portions of 15536 that are optional.

e. Rationale for deviations from 15536.

f. Requirements for the use of existing subsystems (whether GFE or not).

Full-scale development phase. The full-scale development phase is the period when the system, equipment, computer programs, facilities, personnel subsystems, training, and the principal items necessary for support are designed, fabricated, tested, and evaluated. The intended outputs are a system that closely approximates the production item, the documentation necessary to enter the production phase, and the test results that demonstrate that the system to be produced meets the stated performance requirements.

During this phase, the development specifications are completed and authenticated to establish the allocated baseline. A preliminary design effort is used to lead to an acceptable design approach. A preliminary design review (PDR) is held for each equipment configuration item and computer program configuration item (CPCI) to review the preliminary design against the respective authenticated development specification. Formal engineering change control procedures are implemented to prepare, propose, review, approve, implement, and record engineering changes to the allocated baseline.

For computer programs, the preliminary design includes defining the entire computer program in terms of functions, external and internal interfaces, storage allocation, computer program operating sequences, and data base design. This information should be contained in the development specifications and become the basis for the PDR of the computer program.

For data bus systems, preliminary design includes a complete data transfer description, usually in the form of an interface control document, a definition of the design approach of each RT, and a definition of the bus control software and its functions in relation to the system executive software. Significant to evaluate at PDR are the proposed methods and mechanizations of backup and alternative bus control switchover.

Following an acceptable PDR for a configuration item, detailed design of that item begins. This activity produces engineering documentation such as drawings, product specifications, and test plans. For computer programs, design is accompanied by documentation of logical flows, functional sequences and relations, formats, constraints, and the data base. This documentation should be reviewed by engineering personnel prior to the critical design review (CDR). The CDR should ensure that the recommended design satisfies the requirements for the development specification. The primary product of the CDR for CPCIs is t he identification of specific portions of the product specification that will be released for coding and testing. For data bus systems, the CDR should ensure that each assigned data transfer can be accomplished in the proposed design and that all requirements for message growth and system growth have been consistently applied in the design.

Development, test, and evaluation and initial operational test and evaluation phases. During the development, test, and evaluation (DT&E) and initial operational test and evaluation (IOT&E) phases, tests are conducted of configuration items according to formal test plans initially submitted in preliminary draft form for review at CDR and finalized prior to the start of testing. These activities normally proceed in such a way that testing of selected functions begins early during development and proceeds through successively detailed levels of assembly to the point where the complete system is subjected to formal qualification testing.

A data bus system allows considerable flexibility in system testing, even to the point that the same facility may be used alternately for subsystem qualification, system integration, and software qualification. Configuration management of the test facility and the software is vital to integration testing. Each additional terminal (RT or sensor) requires verification of the simulation, usually simultaneously with initial subsystem test. Additional computer programs and equipment may be required to properly simulate the operational environment or test the computer programs or sensors.

The scope and realism of computer program testing maybe progressively expanded as additional items of the operational computer equipment and subsystems are made available for this purpose. Adequacy of the performance of these systems is checked to the maximum extent possible through prudent use of simulation prior to the installation of the sensor into the integration. The use of artificial data or recorded data from similar equipment should be considered. Nuclear safety cross-check analysis (NSCCA) is also performed on specified computer resource items (AFR 122-1).

Planning for transfer of the system to the supporting command and turnover to the using command begins early in the system development process. Necessary agreements should be prepared, coordinated, and approved prior to the end of the DT&E phase. Satisfactory performance of the system, especially a large operational system, may not be completely demonstrated and assessed until completion of operational test and evaluation (OT&E).

Section 60 Index

SECTION 70

MULTIPLEX SYSTEM EXAMPLES

CONTENTS

TABLES

FIGURES

70. MULTIPLEX SYSTEM EXAMPLES

This section presents six multiplex system examples that reasonably represent the state of the art in aircraft multiplexing. The examples represent all three DOD services. Table 704 shows the service and program name of the examples contained herein.

Table 70-1. System Examples

Service	Name
Air Force	B-1B Strategic Bomber
Navy	SH-60F ASW Helicopter
Army	OV-1D Special Electronics Mission Aircraft
Army	AH-64H Attack Helicopter
Air Force	F-16 C/D Air Combat Fighter
Air Force	C-17A Transport

The systems design variations clearly show that differences in multiplex data bus use arise from designer choices and backgrounds as well as from differences in requirements. 'There is value, then, in reading through these examples to get a more balanced perspective. Obviously, many details are omitted in these descriptions, as are the rationales for the designs in most cases. Readers who need additional information will have to make contact through channels to the procuring activity.

The following comments may help readers to select one or more of the examples for initial reading:

a. The B-1B description is of the offensive avionics and it includes only Boeing responsibility for this large system. There are six bus controllers (BC), seven buses, and hundreds of terminals in this system. The essence of the discussion is on synchronization, subaddress extension, and error handling.

b. The SH-60F has two BCs, less than 20 terminals, and one bus. However, this bus is dynamically reconfigured from red only to red-black by means of an isolator/connector. Message processing is demand driven in this system because the BC polls each remote terminal (RT) first for service requests. This type of message processing is unusual.

c. The OV-1D has two BCs, less than 20 terminals, and one bus. This system is an excellent example of the interoperability that has been achieved with 1553B terminals because most RTs in this system were provided as Government-furnished equipment (GFE) to the integrator. The backup BC must have the same data as the BC, and the 1553B message format used must use RT to backup BC transfer (commanded as RT-to-RT), with BC monitoring. This is efficient.

d. The AH-64A is an old 1553A system, but it has noteworthy features for present-day designers. It has two BCs, less than 20 terminals, and one bus. The backup BC and an RT are collocated in one physical unit.

e. The F-16 C/D has two BCs, less than 30 terminals, and four buses. A significant part of this system was built from the old 1553 (USAF), and the new C/D includes dual capability 1553(USAF)/1553B in some terminals.

f. The C-17 has seven BCs, more than 50 terminals, and five buses. This system architecture is unique by its use of interbus transfer units having RTs on two of the buses. There is less detail in this example because of its early development status. it is an excellent example of isolated redundancy.

In each of the foregoing comments, the number of BCs counted is the number of physical units that contained one or more BCs or backup BCs.

The examples show that the trend for backup BC is to provide an identical unit as the BC. Four of the six examples retain normal operations if the BBC takes over, two of them have degraded operation. By the use of one or more discretes combined with monitoring for bus activity, switchover to the BBC is similar in all of the systems. Manual override or manual selection of the BC is a feature of two of the systems.

Status word use varies significantly. In the B-1, it is used only for message completion detection; in the SH-60F, it is used for service requests to initiate data transfers; in the OV-1D the status words are treated differentially by the RT; in the AH-64A, the 1553A status word bits are unique (to AH-64A) system and hardware data indicators; and in the F-16, it is used for message completion and detection similar to the AH-64A in its use of the 1553 (USAF) status word.

If no status word is received, one or more automatic retries of the message occur before proceeding to the next frame. This is apparently true for all the examples except AH-64 and OV-1D, which merely wait until the next frame to try again. However, the systems vary widely as to whether the failure is logged and whether reconfiguration will ever occur as a result of failure detection.

70.1 B-1B STRATEGIC BOMBER.

70.1.1 Mission requirements. The B-1B is a long-range strategic bomber developed by Rockwell International and three associate contractors. Boeing Military Airplanes, as an associate contractor, developed the avionics system. This bomber is designed to perform high-speed low-altitude penetrations to designated targets and deliver nuclear or conventional weapons.

70.1.2 System architecture

70.1.2.1 System topology. The B-1B avionics system hardware consists of a computer complex and supporting line replaceable units (LRU). The system provides capabilities for guidance and navigation, controls, display functions, weapon delivery, terrain following, radar management, defensive operations, and fault recording and monitoring.

Figure 70-1 shows the block diagram of the system. The B-1B contains seven 1553 dual standby-redundant buses. Four of these buses are used by the central computing complex, which provides communications among four BCs and many RTs. The remaining three buses are within the terrain-following (TF) subsystem. Two buses are used as point-to-point links (i.e., one BC and one RT). The remaining bus provides communications among BCs and the radar. A multiple bus architecture was chosen to provide functional organization of the system and to simplify potential problems of bus contention and error detection as follows:

a. Multiple buses were necessary to accommodate the large number of separately addressable LRUs contained in the avionics system because a single bus will support only 31 separate LRUs. There are more than 100 terminals among all the LRUs.

b. This multiple bus architecture permitted functional partitioning of avionics components and processors.

c. Multiple buses with multiple BCs facilitate rapid data acquisition, distribution, and message error detection. Performance is enhanced by rapid data exchange because of reduction in data latency.

d. The use of multiple buses lowers bus loading and thereby increases the potential for growth.

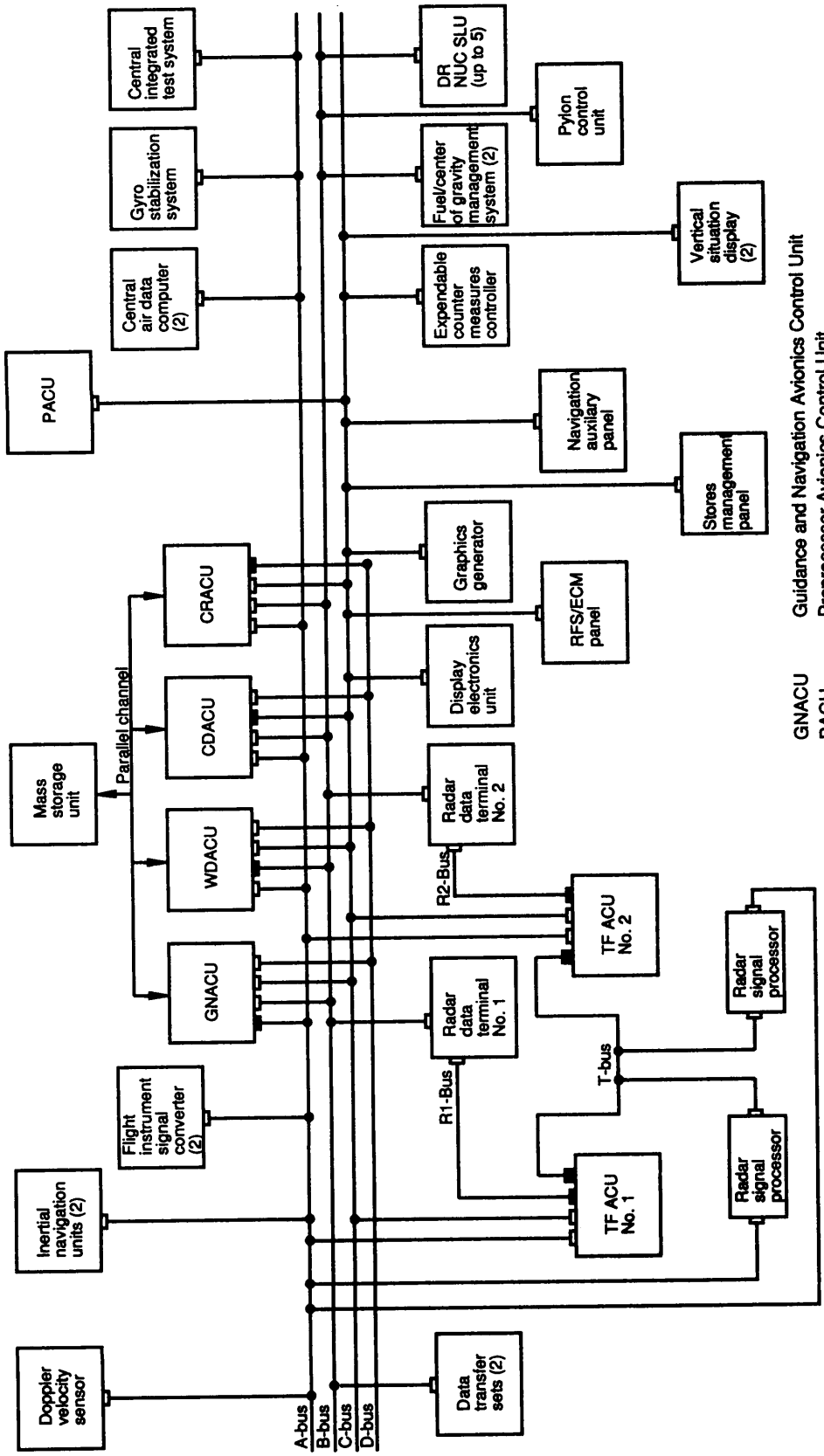


Figure 70-1. B-1B Block Diagram

The B-1B central complex consists of four avionics control unit (ACU) LRUs, each of which contains four dual standby-redundant 1553B interfaces, a computer, discrete 1/0, and power supply. Each ACU 1553 interface may be programmed to be a BC or an RT, so each of these ACUs is a BC on one of the four central buses (A, B, C, and D) and is an RT on the remaining three buses.

Each ACU in the complex (and the bus on which it is a BC) is partitioned functionally. Each bus is assigned the following functions:

a. **A-bus pair—** The A-bus pair controls the guidance and navigation functions of the aircraft. The ACU that is the BC on this bus is designated the guidance and navigation ACU (GNACU).

b. **B-bus pair-** The B-bus pair controls the functions associated with controlling and releasing the weapons. The ACU that is the BC on this bus is designated the weapons delivery ACU (WDACU).

c. **C-bus** pair-The C-bus pair controls the operator interface to the avionics. The ACU that is the BC on this bus is designated the controls and displays ACU (CDACU).

d. **D-bus pair-** The D-bus pair is connected only to the four ACUs. The ACU that is the BC on this bus collects time-critical data from the above three ACUs. If one of the other ACUs fail, this critical ACU (CRACU) reconfigures itself to take over the functions of the failed ACU.

e. **Bus pairs RI and R2—** The BC is the terrain-following ACU (TFACU); TFACU 1 for the R1 -bus and TFACU 2 for the R2-bus. Radar data processing and terrain-following data are handled by this bus.

f. **T-bus pair-** The T-bus pair interconnects the TFACU and the offensive radar systems (ORS). The two TFACUs are the BC and-BBC for this bus. Radar Control and terrain following are controlled from this bus.

In addition to the ACUs in the central complex and TF system, there are two other ACUs on this aircraft. They are assigned the following functions:

a. **Preprocessor ACU-** The preprocessor ACU (PACU) provides the interface and control between the ACU and the defensive system. It is configured as an RT on the C-bus pair.

b. **Central integrated test system ACU-** The central integrated test system (CITS) ACU collects, records, and reports faults in the system. It is configured as an RT on A-bus pair.

The 1553 equipment lists for each bus are as follows (numbers in parenthesis indicate the number of LRUs):

a. **Bus pair A (navigation functions)-**

1. Four central ACUs.

2. Doppler velocity sensor (DVS) (1).

3. Radar signal processors (RSP) (2).

The RSP LRUs are part of the radar set (RS). Airplane state data are provided to the RS via the A-bus.

4. Inertial navigation units (INUs) (1).

There is also provision for one more.

5. Terrain-following ACU (TFACU) (2).

Airplane state data are provided to the TF system via the A-bus.

6. Central integrated test system (CITS) computer (1).

7. Gyro stabilization system (GSS) (1 **)**

8. Central air data computer (CADC) (2).

9. Flight instrument signal converter (FISC) (2).

The FISC provides the interface with the airplane flight control system for roll steering commands.

10. Offensive radar system (ORS) (2)

b. **Bus pair B (weapon delivery)-**

1. Four central ACUs.

2. Data transfer sets (DTS) (2).

The DTS data tapes provide a backup source for the operational software and are the primary source of mission and weapon targeting data.

3. Radar data terminal (RDT) (2).

The RDT LRUs provide an interface with the airplane electrical multiplex (EMUX) and nonmultiplex signals of the TF system.

4. Decoder receiver (DR) (up to *5).* (A total of five NUC SLUs and DRs are available.)

This LRU is part of the stores interface.

5. Pylon control unit (PCU) (1).

The PCU LRU is part of the stores interface.

6. Nuclear station logic unit (NUC SLU) (up to 3) or conventional station logic unit (CON SLU). (A total of five NUC SLUs and DRs are available.)

The NUC SLU and CON SLU LRUs are part of the stores interface.

7. Fuel and center-of-gravity management system (FCGMS) (2).

Stores weight data are transmitted to the FCGMS system.

c. Bus pair C (controls and displays-defensive)-

1. Four central ACUs.

2. Display electronics unit (DEU) (1).

The DEU provides the electronics for the vertical situation display.

3. Graphics generator (GG) (1).

4. Expendable countermeasures (EXCM) controller (1).

5. Terrain-following ACU (TFACU) (2).

The TFACUs provide display, power control, and maintenance information to the central complex.

6. Radio frequency surveillance/electronic countermeasures (RFS/ECM) panel (1).

7. Navigation/auxiliary (NAV/AUX) panel (1).

8. Stores management (SM) panel (1).

9. Vertical situation display (VSD) display (1).

10. Preprocessor avionics control unit (PACU) (1).

The PACU controls the functions of the RFS/ECM.

11. Tail warning receiver (1).

d. **Bus pair D (critical function)-**

1. Four central ACUs.

e. Bus pair T (terrain following)-

1. Terrain-following ACUs (2).

2. Radar signal processor (2).

f. **Bus pairs RI and R2 (radar data)-** There is both an R1 bus and an R2 bus. Each has equivalent sets of equipment (i.e., R1 has TFACU 1 and RDT 1).

1. Terrain-following ACU (1 for each R-bus pair).

2. Radar data terminal (RDT) (1 for each R-bus pair).

70.1.3 System hardware.

70.1.3.1 Media. The seven 1553B buses on the B-1B range in length from 40 to 375 ft, and the number of stubs per bus range from three to twenty. The bus cable is made by Raychem and has a nominal impedance of 77 ohms.

The B-1B uses transformer coupling exclusively. There are two types of bus couplers used (both made by Singer-Kearfott). The type I coupler has a 1:1 turns ratio and is used for five 1553A stubs on the B bus. The type 1 coupler has a 1:1.41 turns ratio and is used for all other stubs.

Each bus has at least one ground support stub that is not connected to a terminal during normal operation. This stub is used to connect diagnostic test equipment to the bus.

Stub lengths are, on the average, 4 to 7 ft. On the B-bus, there is one 18-ft stub, and on the C-bus there is one 25-ft stub. Table 70-11 shows the lengths of each main bus (note that Al and A2, etc., refer to each side of a dual-redundant pair).

Table 70-11. Lengths of Main Bus

Bus	Number of stubs	Main bus length
A1	18	270 ft
A2	18	230 ft
B1	20	330 ft
B2	20	330 ft
C1	17	375 ft
C2	17	375 ft
D1	5	65 ft
D2	5	40 ft
R1-1	3	60 ft
R1-2	3	55 ft
R2-1	3	55 ft
R2-2	3	50 ft
T1	5	100 ft
T2	5	90 ft

The waveform quality on all buses falls within the specifications of 1553B. On the longer buses (B and C), there are certain points where reflections caused a terminal to malfunction. An analysis of the problem indicated that tailoff was being interpreted by a terminal as a valid part of a message; this was fixed by modifying terminal hardware.

70.1.3.2 RT details.

Avionics LRUs. All B-1B avionics LRUs are equipped with embedded dual-redundant 1553B terminals. The LRUs operate as RTs in accordance with 1553B, except as indicated below.

Mode commands. The RTs, except the INU, radar signal processor (RSP), and all ACUs as RTs, do not respond to mode commands.

Broadcast commands. The RTs do not respond to broadcast commands.

Illegal commands. The RTs do not monitor for illegal commands.

Status word bits. New-design RTs set the bits in the 1553 status word as follows (these bits are further defined in the standard):

Bit no.	Label
9	Message error bit
10	Instrumentation bit
11	Service request bit

12-14	Reserved status bits
15	Broadcast command received bit
16	Busy bit
17	Subsystem flag bit
18	Dynamic bus control acceptance bit

The RTs in Government-furnished and modified LRUs set the bits in the status word with their individual specifications. As a result, status word bits are not monitored because the capability to interpret each bit of the RT is not a BC hardware capability. Evaluation of status bits in software is not feasible.

70.1.3.3 BC details. The avionics control unit is a general-purpose computer that may use up to 256K 16-bit words of core memory, four dual standby-redundant 1553 terminals, and a parallel I/O channel.

In the BC mode, the multiplex controller accepts a list of "chain" instructions, where each instruction may request a bus message transmission or jump conditionally to another list of chain instructions. The generation or completion of error interrupts is controlled by parameters in the chain instructions. The controller can accept two chains of instructions: the normal and the priority chains. Initiation of a priority chain pre-empts processing of the normal chain at the end of a current bus message. When the priority chain is exhausted, processing of the normal chain resumes where it left off. This arrangement allows large, efficient blocks of cyclic bus requests to be used without preventing occasional, high-priority requests from being transmitted promptly.

In the RT mode, received messages are transferred directly to memory, according to tables of pointers accessed by the multiplex controller, as a function of the subaddress (S/A) in each multiplex command. Bits in these tables also control whether completion interrupts are to be generated.

The ACU supports interrupts for 1553 data bus completion and detection of errors.

70.1.4 System control.

70.1.4.1 Data transfer formats. The B-1B avionics multiplex system uses BC-to-RT, RT-to-BC, and RT-to-RT transfers. It does not use broadcast.

70.1.4.2 Mode code use. Only the synchronize without data word and the synchronize with data word are used in this system. They are used to synchronize the INU and ORS, respectively.

70.1.4.3 Status word use. The presence or absence of the status word determines successful message completion. No status word bits are interpreted by the processors because error detection is successfully completed by other means discussed in 70.1.4.6.

70.1.4.4 System startup. Each of the four buses is controlled by an ACU assigned a particular function associated with the terminals on that bus. The guidance and navigation ACU (GNACU) controls the A-bus, the weapons delivery ACU (WDACU) controls the B-bus, the controls and displays ACU (CDACU) controls the C-bus, and the critical ACU (CRACU) controls the D-bus. TFACU 1 is the BC for the T-bus and the RI -bus. TFACU 2 is the backup bus controller (BBC) for the T-bus and the BC for the R2-bus. When power is first applied to the computers, the system management function checks the loaded and operational status of the central complex, synchronizes timing in the ACUs, and executes the initialization routines provided by all functions to initialize data bases and begin normal processing.

Message scheduling. All minor frames are executed at 64 Hz. Figure 70-2 illustrates central computing complex I/O by minor frame and bus pair.

Synchronization. The central computing software (CCS) provides for control and maintenance of all avionics system timing relationships.

The GNACU is the prime source for all the time references to which all time-critical elements of the system are synchronized. The ACU that is configured (loaded) as the CRACU assumes the role of the prime time reference source if the GNACU fails.

a. **ACU synchronization-** The GNACU sends a minor frame count and ACU ID (physical address in the central complex) to the other central ACUs via the multiplex bus once each minor frame. The GNACU also outputs hardwired real-time clock (RTC) pulses to each of the central ACUs. Because each of the central ACUs receives clock pulses from all the other central ACUs on their external interrupt ports, they must use the ACU ID signal to determine which of the three external interrupts is that of the GNACU RTC by relating physical address to both physical discrete input and to logical load information. They then choose that as their external clock source. Upon initialization, each central ACU adjusts its minor frame number to match the one that it received from the GNACU. During normal processing, any ACU out of synchronization for five consecutive minor frames will be declared failed and cause reconfiguration.

   Each central ACU adjusts its internal real-time clock to follow the GNACU real-time clock by 350 us. Their internal RTC is not to be used unless a GNACU failure occurs.

b. **Inertial navigation system (INS) synchronization-** The INS runs asynchronous to the GNACU, but it does provide a time tag along with the navigation data it supplies. This time tag represents the value of a free-running counter within the INS that is read at the time the navigational data are measured. To establish a relationship between the INS time tag and the GNACU system time, the GNACU has been given the capability to reset the INS free-running counter.

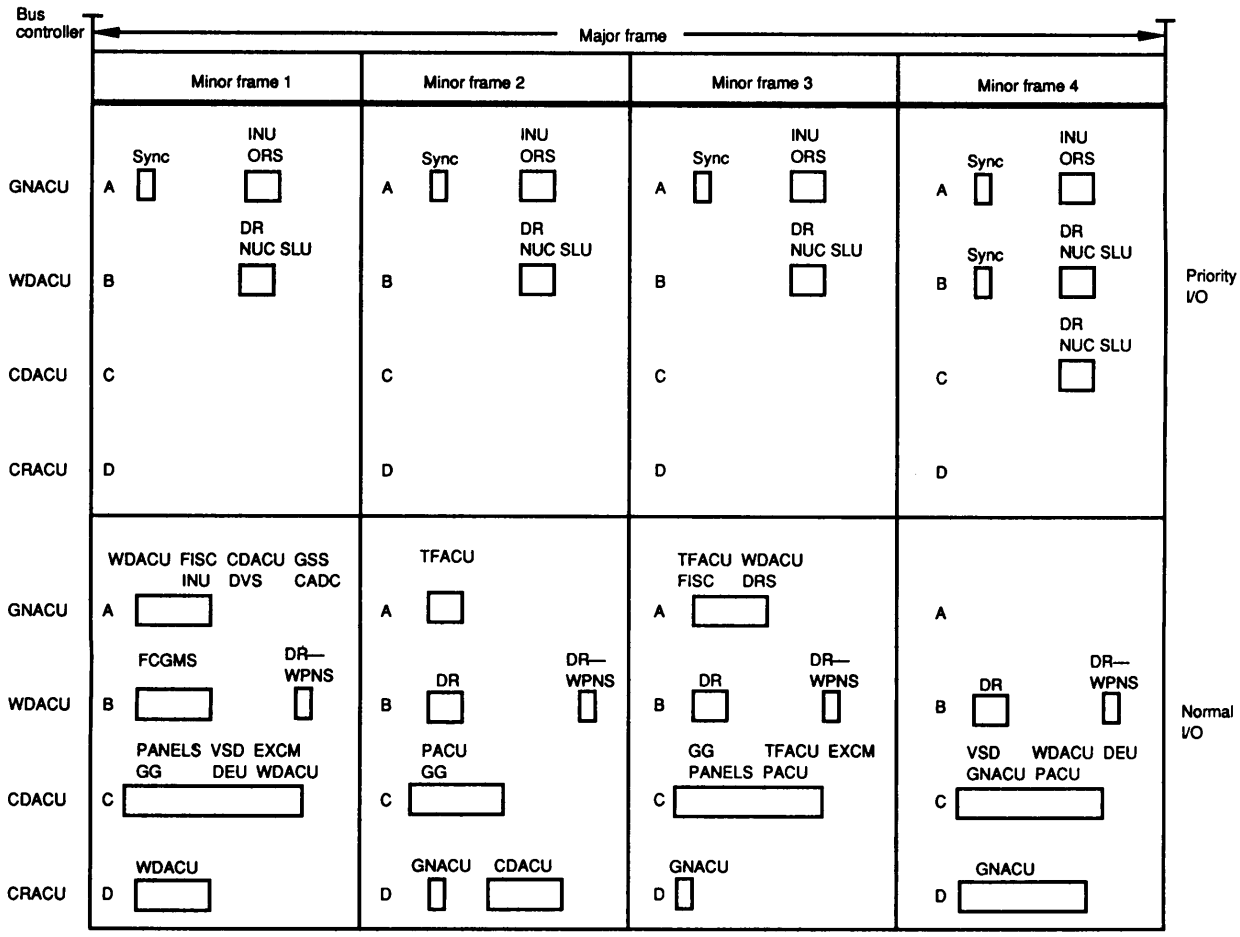
   At a 1 -Hz rate, the GNACU outputs to each INS a synchronize mode code without data word. The INS immediately sets its free-running counter to zero. The INS time tag provided with navigation data then represents the time expired from the last synchronization command received from the GNACU to the time the INS reads the airplane state data.

c. Radar set (RS) synchronization— The RS contains an internal clock that is synchronized to the GNACU to minimize aging effects of the navigation and other data it uses.

   The GNACU sends a synchronization mode command with data word to each RS channel at a 1 -Hz rate. The data word contains the time expired since the beginning of the last GNACU minor frame. The minor frame number related to this command is sent to the RS in a separate message. The RS calculates the time left in the minor frame and increments that time by both the estimated clock drift (constant) and worst case time delays due to transmission retries (constant). The final time calculated is the worst case time delay that high-rate navigation data are received by the RS. The RS then sets and activates a 64-Hz clock to this value. At every clock pulse, the RS assumes new navigation data have been received. Also, the 1-Hz synchronization command presets an interval timer used for reference to calculate the latency of the navigation data.

   The synchronization message sent to the RS and INU are sent in a group in the following order: INU 1, RS 1, RS 2, INU 2. This set pattern minimizes the error in the estimation of the latency of the data the RS receives from the INU.

d. **TFACU synchronization—** The TFACU relies on its internal clock for timing and is synchronized to the GNACU to minimize errors in its computations, which use data passed on from the GNACU and CDACU. A synchronize command (not a mode code) at a 1 Hz rate is used to synchronize the GNACU outputs to each TFACU. This transmission includes the minor frame count and time reference. The time reference is the time that has expired since the beginning of the GNACU minor frame to the start of the current transmission. The TFACU then calculates how much time is left in the GNACU minor frame and sets an



GNACU	Guidance and Navigation Avionics Control Unit
PACU	Preprocessor Avionics Control Unit
WDACU	Weapon Delivery Avionics Control Unit
CDACU	Controls and Displays Avionics Control Unit
CRACU	Critical Avionics Control Unit
TFACU	Terrain-Following Avionics Control Unit
RFS/ECM	Radio Frequency System/Electronic Countermeasures
DR	Decoder Receiver
NUC SLU	Nuclear Station Logic Unit
INU	Intertial Navigation Unit
ORS	Offensive Radar System
FISC	Flight Instrument Signal Convertor
DVS	Doppler Velocity Sensor
GSS	Gyro Stabilization System
EXCM	Expendable Countermeasure
GG	Graphics Generator
WPNS	Weapons
VSD	Verticle Situation Display
DEU	Display Electronics Unit

Figure 70-2. Central Complex 1553 I/O

interval timer accordingly. On expiration of this interval timer, the TFACU recognizes the interrupt as an RTC reset and resets its RTC, thereby synchronizing to the GNACU. Each TFACU sets and maintains its own real-time clock to follow the GNACU.

70.1.4.5 Message processing. Once synchronized and initialized, each ACU begins processing its 1553 messages. ACU time is divided into major and minor frames. A major frame lasts 1/16 sec (62.5 ms) and is divided into four minor frames, each being 1/64 sec.

Error-causing retries can cause a minor frame to be longer than 1/64 sec. Part of the scheduled communications is between the ACUs. Because of the large amount of data passed between the ACUs, and because of the limited number of subaddresses available, several subaddresses are defined as general-purpose subaddresses. Messages received may change the subaddress-to-memory table. This increases the number of effective subaddresses.

A disadvantage of this technique is that this type of data transfer is very difficult to troubleshoot during development and evaluation testing.

70.1.4.6 Error detection and recovery. The presence of a status word indicates a successful message transfer. When the status word is not detected, the ACU BC will automatically retry the message on the alternate bus. Whether or not a status word is received, the BC will transmit the next message in the chain.

ACU reconfiguration. In the event of a single ACU (GNACU, WDACU, or CDACU) failure, the central complex will reconfigure (load) the CRACU to the configuration of the failed ACU. Assumption of all functional responsibilities, including BC responsibilities, is completed in less than 500 ms by the reconfigured CRACU. Loss of inter-ACU I/O for two minor frames will create a no-go situation and cause the ACUs reconfigure.

If an ACU failure or no-go occurs and the CRACU is not operating, emergency shutdown processing is initiated and, on completion, power is removed from the central computing complex.

First, the CRACU monitors each central ACU serial I/O. On detection of a loss of serial I/O for two minor frames, the CRACU will issue an abort message to the faulty computer over the D-MUX. if the computer is at all alive, this message will cause a serial I/O interrupt that will initiate ROM no-go processing.

Next, an attempt is made to read the vector word from the serial interface of the failed computer. The vector word is loaded by the ROM no-go logic with a code indicating the cause of the failure. if read successfully, this code is recorded in the central database for fault recording and reporting by the avionics integrated test function. The CRACU then requests or causes power to be removed from the failed computer (depending on whether the computer that interfaces with EMUX has failed). Finally, the CRACU seizes the serial bus belonging to the function to be assumed.

I/O wraparound test. In addition to the fault-detection capability provided by the RT internal built-in test (BIT) of the ACU, the avionics central computing software (CCS) provides terminal failure detection capability in the form of a special-purpose I/O wrap test.

Following computer initialization and synchronization, the CCS in the computer designated as the BC transmits pairs of data words with the opposite parity to all the ACU RTs on the bus. The two words, selected in pairs from a set of five designated data words, are transmitted at a 2-Hz rate. The BC then requests that the RTs return the data words. The returned words are compared with the data transmitted. A single failure, failure to compare, or failure to respond from all the RTs will cause the ACU BC to initiate no-go processing.

The CCS in the RTs determines when an I/O wraparound sequence is not received by a BC. If the CCS receives the expected i/O wraparound sequence, it compares the two data words of the first transmission with that of the second transmission for that cycle. An I/O wraparound is successful when the data words are

received from the BC and a correct comparison occurs. If the test fails for a 1 -see period (one cycle), the RT ACU initiates no-go processing.

70.l.4.7 Special features.

Bus control. To ensure that no two computers have the same load and attempt to control the same bus, the CCS, at power on, attempts to seize, in each ACU, control of the data bus associated with the function of its loaded program. The CCS alternates transmitting and listening on the bus until it either gains control or it discovers that another computer has done so. The listening periods are different for each physical computer location, and they are chosen to guarantee rapid conflict resolution. Once a bus is seized by a computer, the computer continues to transmit bus claim messages to prevent another computer from seizing its bus. If the computer fails to seize its functional bus, it declares itself unloaded.

Dynamic subaddressing. Dynamic subaddressing expands the use of memory locations in that it allows for use of the same subaddress for more pieces of data. A message is sent from the data source ACU to the receiver ACU specifying data to be sent to a particular memory location; a continuous flow of the data follows.

These memory locations consist of eight subaddresses, each of which is used to transmit 32 words. Thus, a total of 256 words can be transmitted. The table is then reset to allow another set of data flow and so forth. Figure 70-3 shows an example of a data subaddress table.

Subaddress	Receive	Transmit
0	Not usable	Not usable
1		
2		
3	Foreground DAT 1	Foreground DAT 1
4	2	2
5	3	3
6	4	4
7	5	5
8	6	6
9	7	7
10	8	8
11	Synch message	
12		
13		
14	Bus claim	
15	EMUX status	
16	Background DAT 1	Background DAT 1
17	2	2
18	3	3
19	4	4
20	5	5
21	6	6
22	7	7
23	8	8
24	Connect table	
25	Status	
26	Interrupt (on receipt)	
27	Next DAT for foreground data (receive)	
28	Next DAT for background data (receive)	
29	Next DAT for foreground data (transmit)	
30	Next DAT for background data (transmit)	
31	Not usable	Not usable

Figure 70-3. *B-1B Dynamic Subaddressing Using Data Address Table*

For example, memory location number 26 (interrupt), is particularly useful in notifying an ACU of a particular incident such as an ACU failure. An ACU could receive this notification it of its own failure and its necessity to unload. Other interrupts are for ACU load requests, special statusing, special program calling, and classified data erase.

The subaddresses marked “foreground” and “background” are those used to transmit or receive dynamically subaddressed data. If an ACU is to transmit a message, subaddress numbers 29 and 30 indicate from which foreground or background location, respectively, the data are to be pulled. Subaddresses 27 and 28 indicate into which foreground or background location, respectively, the message is to be received.

Some disadvantages with this technique are that this type of data transfer is very difficult to troubleshoot, and it is essential that the user be extremely knowledgeable about the subject to prevent ACU failure or misuse as a result.

70.1.4.8 Conclusions

a. A large 1553B system, with both 1553A and 1553B terminals, has been developed and production is nearly completed.

b. The system is virtually 100% periodic.

c. Cable lengths greater than 300 ft (per 1553A) work.

d. In a large system like the B-1B, status word interpretation is too difficult; 64-Hz real time, limited health data.

e. Mode commands were not an attractive alternative in error handling or reconfiguration.

70.1.4.9 Lessons learned.

Synchronization time. Original requirements specified restraining the synchronization time to within 100 us. Over the years, this time has not been maintained and has extended to within 500 us. There also exist certain cases where this 500-us requirement cannot be met.

As more processing and I/O was added to each frame, the frame time would fill up. If an interrupt (other than the I/O complete interrupt) occurs close to or at the end of a minor frame, the time it could take to process that interrupt could overlap into the time of the next frame before the I/O complete interrupt can be serviced and take effect.

To eliminate overlap into the time of the next frame, ACU hardware or software design should be such that it provides for servicing of more than one interrupt at a time. If an ACU does not have this capability, then provisions should be made to prevent interrupts other than the I/O complete interrupt at, or close to, the end of a minor frame.

Synchronous message competition with other I/O. Because time-critical data (such as radar data) must be processed immediately, a competition for processing arose between that data and the synch message. This conflict resulted in the synch message being slid to approximately halfway into the frame.

When designing synchronization over a bus, strict attention must be dedicated to other I/O (i.e., time-critical data) that could gain processing priority over the synch message. Time planning must properly foresee and resolve any possible conflicts.

70.2 SH-60F CV-HELO.

70.2.1 Mission requirements. Defense of the aircraft carrier within a surface fleet task group is of paramount importance. An assortment of surface ships, submarine vessels, and aircraft are deployed continuously in this role. Within a few hundred miles of the aircraft carrier, fixed-wing aircraft such as the EA-3B may use sonobuoys, radar, or magnetic anomaly detection in an attempt to locate and potentially neutralize a submarine threat. At moderate range, destroyer-based helicopters such as LAMPS equipped with similar avionics resources will operate. The last line of defense is the inner zone. Within the inner zone are deployed surface ships and helicopters that are equipped for antisubmarine warfare (AWN) and capable of using sonobuoys, dipping sonar, and carrying torpedoes.

The SH-60F CV inner zone ASW weapon system is the new Navy fleet ASW helicopter that will help provide increased protection in the 30-nmi inner zone of the carrier battle group. The CV-HELO is being built for the Navy by Sikorsky Aircraft, Division of United Technologies Corporation, with Teledyne Systems company as the mission avionics integrator.

The primary mission of the CV-HELO is ASW in a permissive air environment. The CV-HELO will normally be employed as an inner ASW zone screening unit and reactive localization system. It has the means to detect, classify,, localize, and attack submerged submarines within the inner ASW zone. Automatic approach and hover capabilities are provided to enable day or night use of an active dipping sonar. The CV-HELO is capable of performing missions of search and rescue, fleet support, medical evacuation, communication relay, logistics support, and surveillance.

The avionic system is capable of processing tactical data and controlling integrated avionic equipment, navigating accurately, communicating with other aircraft and ships, and employing acoustic sensors and weapons in both hovering and forward flight to detect, classify, localize, and attack threat submarines.

70.2.2 System architecture.

70.2.2.1 Topology. The CV-HELO mission avionics are functionally partitioned into the following areas:

a. Tactical data system.

b. Navigation sensor subsystem.

c. Crew controls and displays.

d. Communication subsystem.

e. Acoustics subsystems.

f. Armament and stores subsystems.

The CV-HELO mission avionics topology is shown in Figure 70-4. Much of the prime system equipment is interfaced via two 1553B dual standby-redundant serial data buses. Two data buses are used to provide red and black data isolation through the means of a red/black bus isolator (RBBI) unit as shown in Figure 70-5. The Navy is currently investigating the need for the RBBI.

Red bus. Mission-sensitive processed digital and acoustic data are transferred on the red bus under control of two tactical data processors (TDP). The TDPs are the BC and BBC for the 1553B data buses. Four primary crew stations exist for the ASW mission:

a. Pilot.

b. Copilot.

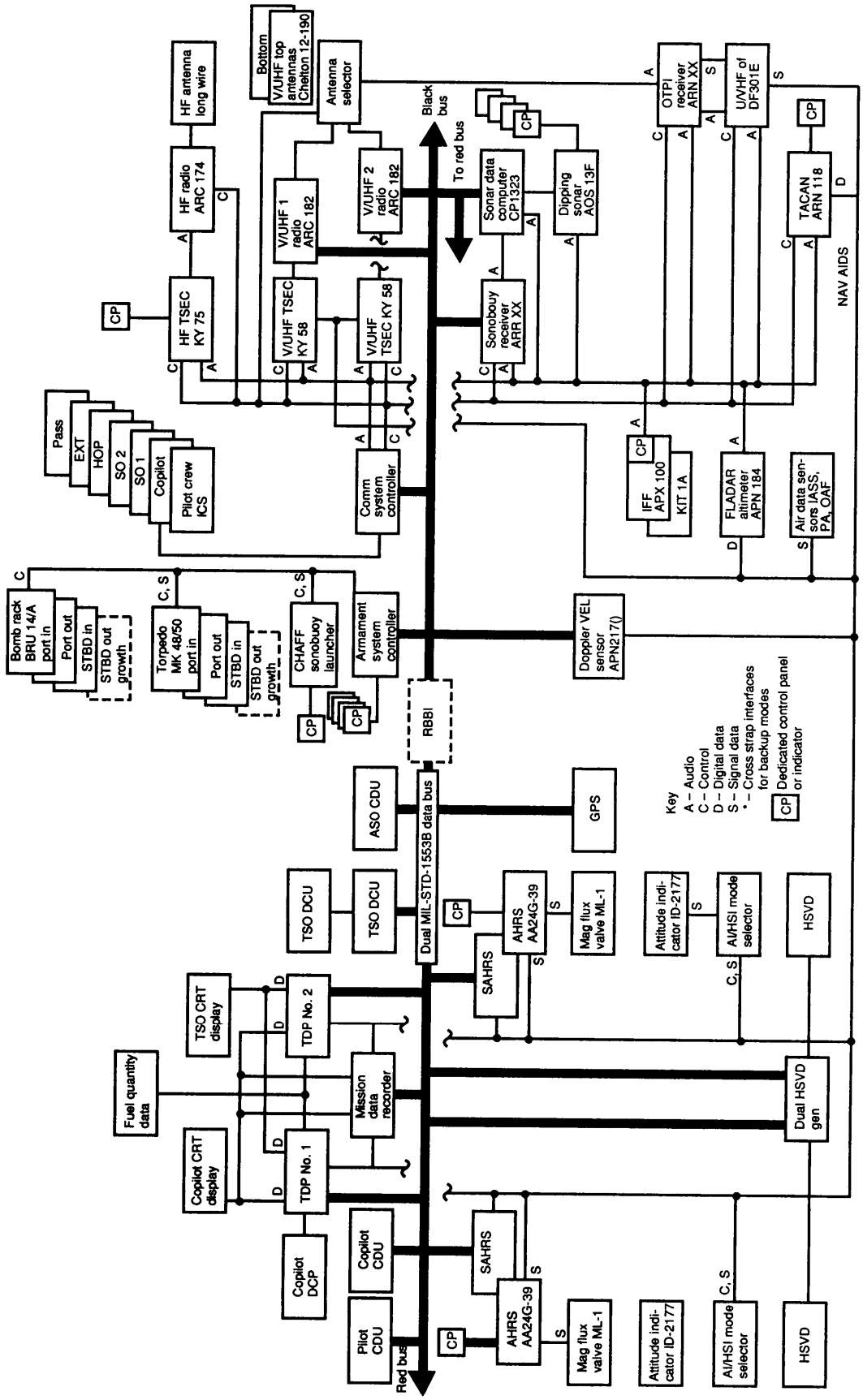


Figure 70-4. CV-HELO Mission Avionics

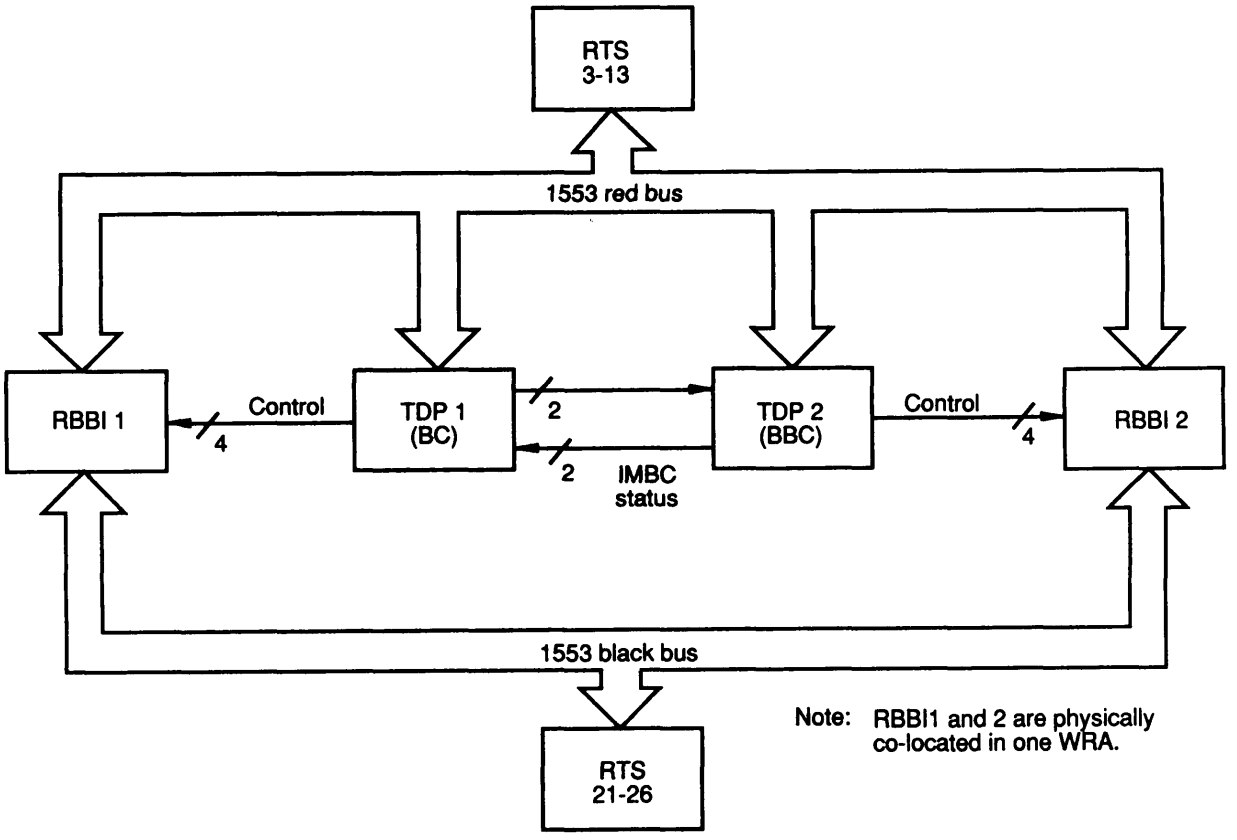


Figure 70-5. Red-Black Bus Isolation and Control

c. Acoustic sensor operator.

d. Tactical sensor operator.

The red bus is the primary interface for the four control display units at each of the stations. The following equipment is attached to the red 1553 data bus. The BC in the TDP is responsible for all data bus communication between itself and the RTs, as well as RT-to-RT communication. The number given to each item in Figure 70-5 corresponds to its RT address as follows:

	RT
BC/RT 1	1553B BC in TDP 1
BBC/RT 2	15539 BBC in TDP 2
RT 3	Control display unit (CDU) 1 (copilot)
RT 4	CDU 2 (pilot)
RT 5	CDU 3 (tactical sensor operator)
RT 6	CDU 4 (acoustic sensor operator)

RT 7	Sonar data computer
RT 8	Mission tape recorder interface unit
RT 9	Horizontal situation video display 1
RT 10	Horizontal situation video display 2
RT 11	Global positioning system (growth)
RT 12	Standard attitude heading reference system (SAHRS) 1 (growth)
RT 13	SAHRS 2 (growth)

Black bus. Those devices that handle no processed mission-sensitive data and are either intentional radiators or have the potential of radiating unintentionally are on the black bus. The RTs on the black side of the bus (again identified by their RT address) are as follows:

Address	RI
RT 21	V/UHF radio ARC-1821
RT 22	V/UHF radio ARC-1822
RT 23	Doppler APN (217)
RT 24	Sonobuoy receiver ARR-84
RT 25	Armament system controller
RT 26	Communications system controller

70.2.3 Hardware.

70.2.3.1 Media.

Remote terminals. Most subsystems interface directly with the 1553B data bus. Subsystems that do not have a 1553 interface are interfaced with special-purpose I/O within the TDPs, communication system controller, or the armament system controller.

Bus controllers. The primary control of the system bus is provided by a 1553B module resident in each TDP. The TDP is a part of the tactical data subsystem. Primary bus control is managed by TDP 1, while TDP 2 uses identical software and hardware to perform a backup bus control function, allowing it to take control of the bus should the primary bus control system fail.

Bus interface module (1553). The 1553 module provides a data bus interface that meets the requirements of a dual-redundant terminal compliant with 1553B. The 1553 module is capable of operating either as a BC or as an RT. The 1553 module is capable of interfacing with a long stub (transformer coupled) as defined in 1553B. The terminal, when acting as an RT, responds to messages whose addresses correspond to an externally wired (to the TDP connector) five-bit address code. Operation of the 1553 module is determined by an on-module microcontroller whose program code is implemented in PROM devices. The microcontroller on-module memory includes a minimum of 4096 words of program code and 256 bytes of scratchpad storage.

The microcontroller interprets and executes commands to the terminal from the TDP CPU. The interface with the CPU consists of a command latch, a ready flag, and an interrupt signal. The ready flag indicates the availability of the command latch to the CPU. The 1553 module also implements a direct memory access channel (DMA) for data and for status and polling sequence instruction exchanges with the TDP memory.

The 1553 module provides a transmit timer that is enabled at the start of a 1553 data bus transmission and times out in 768 us. If the transmission is not complete when timeout occurs, further transmission is inhibited and a fail flag is set.

The 1553 module provides timing signals to be sent to the RBBI to:

a. Select A-bus or B-bus.

b. Enable or disable red-to-black transmission.

Red/black bus isolator (RBBI). The two 1553B data buses provide red and black data isolation through the RBBI unit. Via the RBBI, mission equipment not requiring red data can be isolated on the black side of the 1553B data bus from mission equipment requiring red data on the red side of the bus. The RBBI is a dual

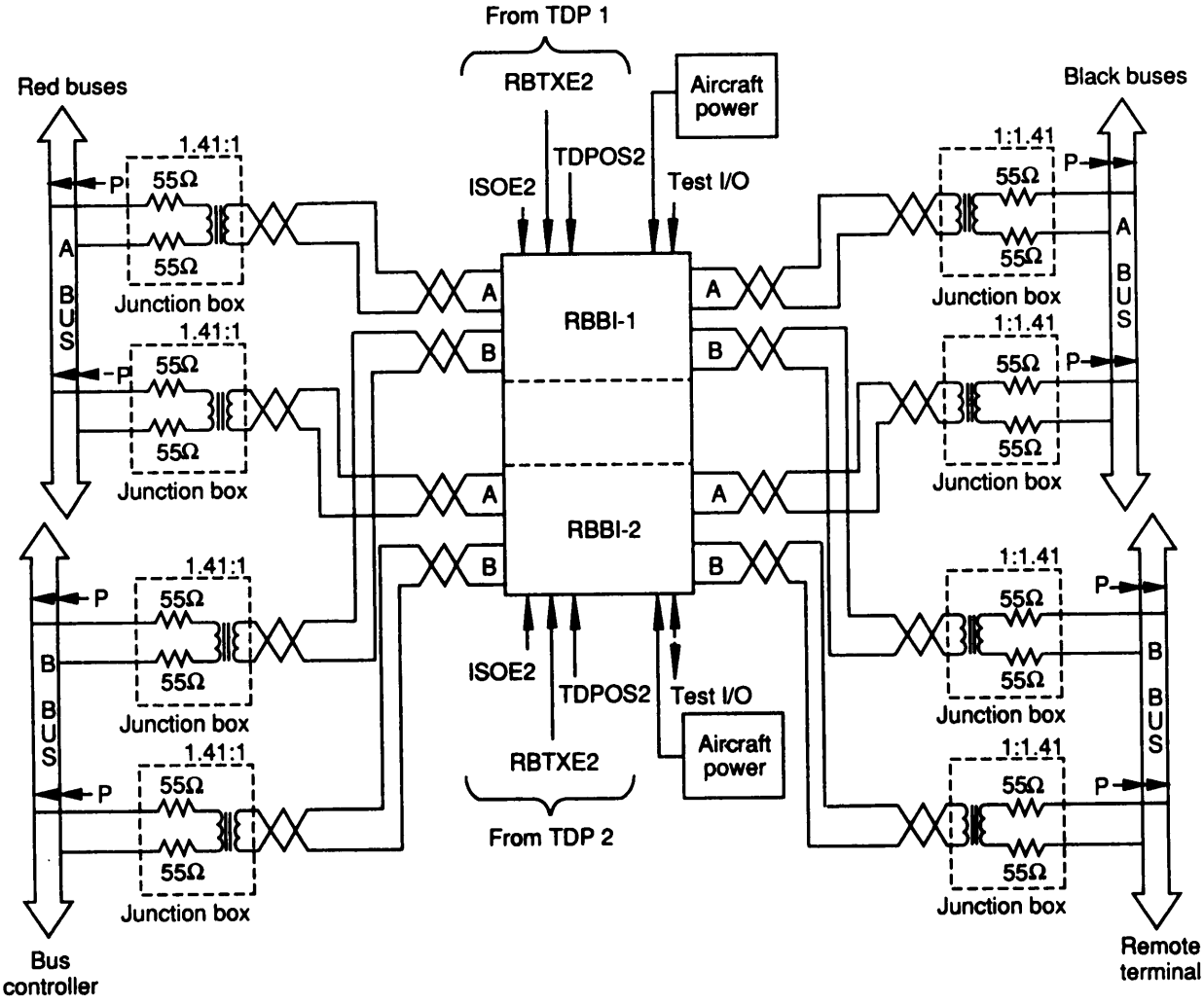


Figure 70-6. RBBI External Interfaces

15536 bus isolator whose configuration (data direction and path) is controlled by four discretes-two from each external BC. Combined within one enclosure are four bidirectional bus isolators configured as dual redundant. Figure 70-6 shows the RBBI external interfaces.

70.2.4 System control. Bus management responsibility is taken by the TDP currently handling the BC function. Assigned mode codes, as shown in Table 70-III, are used for bus control. The duties of the BC are determined by the capabilities of the individual 1553 devices that are performing as RTs on the system data bus.

Table 70-111. *Assigned Mode Codes*

T/R bit	Mode code	Function	Associated data word	Assigned
1	00000	Dynamic bus control		Not Used
1	00001	Synchronize w/o word		Not Used
1	00010	Transmit status word	No	Used
1	00011	Initiate self-test	No	Used
1	00100	Transmitter shutdown	No	Used
1	00101	Override transmitter shutdown	No	Used
1	00110	Inhibit terminal flag bit		Not USED
1	00111	Override inhibit terminal flag bit		Not Used
1	01000	Reset remote terminal	No	Used
1	10000	Transmit vector word	Yes	Used
1	10001	Synchronize with word	Yes	Used
1	10010	Transmit last command		Not Used
0	10011	Transmit BIT word	Yes	Used
0	10100	Selected transmitter shutdown		Not Used
0	10101	Override selected transmitter shutdown		Not Used

70.2.4.1 Data transfer formats. The data transfer formats used on the CV-HELO are BC-to-RT, RT-to-BC, and RT-to-RT.

70.2.4.2 Mode codes. The implemented mode codes are shown in Table 70-III.

70.2.4.3 Status word use. In addition to verifying message completion, the status words are used to indicate service requests to initiate data transfers. (See 70.2.4.6 for a description of this process.)

70.2.4.4 System startup The primary BC is, under normal conditions, TDP 1. However, the health of the BC is constantly monitored by TDP 2, the backup BC. Which of these units actually is in control of the data bus is determined as follows:

a. After successful completion of BIT functions, each TDP samples its 1553 address assignment as determined by the wiring of its external harness connector.

b. The terminal with address 1 (TDP 1) assumes the role of BC, if it passes its initialization BIT and conditions C and D are satisfied.

c. The terminal with address 2 (TDP 2) performs its power-on BIT, waits 500 ms, and then checks to see if TDP 1 has asserted itself as BC. If TDP 1 has asserted itself as BC, TDP 2 assumes the role of BBC, monitoring the bus for activity and testing a bus control assertion discrete from TDP 1. If the discrete indicates BC failure, or if no activity is on the bus for four normal polling cycles, TDP 2 asserts itself as BC.

Assertion of bus control is marked by the TDP setting its CONTROL discrete output (IAMBC). Bus activity is determined by the TDP recognizing that it is being polled (addressed) as an RT. The absence of four successive pollings constitutes no bus activity. Table 70-IV applies to the TDP monitoring control and the bus.

Power interruptions (dropouts) are not considered to be failures and can be expected during normal aircraft operation. Power interruptions may be experienced differently in each TDP. Recovery from power transients are treated as a normal power-on condition as described above.

Table 70-IV. Bus Controller Truth Table

IAMBC control input	Bus activity	Action
BC	No	Wait, switch to BC, send alert to MFD*
BC	Yes	Other TDP is BC, remain RT
RT	No	Switch to BC, other TDP is RT or Off
RT	Yes	CONTROL failed, send alert to MFD*

* MFD alert advises pilot to pull circuit breaker on other TDP.

To minimize system transients, once bus operation has started, with either TDP 1 or TDP 2 as BC, the configuration shall be maintained until either:

a. A failure of the BC or its associated RBBI is detected and the failed BC no longer asserts its bus control (IAMBC) discrete.

b. A power interruption has occurred.

c. A command for self-test (operational readiness test) is received.

70.2.4.5 Message processing. The TDP acting as BC polls all RTs in sequence at a 25-Hz rate. Polling of successive RTs continues until all the RTs have been checked, a failure is detected, or until a service request is encountered. In all cases, polling is resumed at the next RT after the last one that was polled. Polled terminals are of two types:

a. **Intelligent terminals -** These RTs are polled for their status via the transmit vector word command at a 25-Hz rate. They respond with a status word and an associated data word. The RT-to-RT, BC-to-RT, and RT-to-BC transfer modes are used as applicable.

b. **Nonintelligent terminals -** These RTs are polled for their message by the transmit status word command at a 25-Hz rate. They respond by sending their status word.

If a failure is detected, the polling process is stopped, and the host processor is interrupted with an indication of the error occurrence. Corrective action, appropriate to the nature of the fault, is taken immediately.

Data transfer. An intelligent RT requests service via a nonzero vector field. This indicates that the RT (requester) wants to initiate a data transfer. The format is as follows:

a. Target address (maybe BC or another RT).

b. Direction of the data transfer (requester to target or target to requester).

c. Number of words to transfer (word count).

The BC checks the word count to verify that a data transfer is to occur. If the word count does not indicate zero, then the transfer process can proceed.

For the BC-to-RT data transfer, the BC issues a receive command to its target RT (i.e., the requester is the BC itself).

With RT-to-BC transfers, the BC must input data from the requester. The BC checks the device address in the vector word. If the device address is the same as the device address assigned to the BC, then the BC outputs a transmit command to the requester, which contains the word count value that was received in the vector word, and then switches to a receive mode to accept the data from the requester.

For RT-to-RT transfers, the BC initiates the data transfer between the involved RTs (requester and target), and does not intercept or accept any of the transmitted data. In this case, the BC uses the device address as the RT address of the target. The BC outputs a receive command to the target and then a transmit command to the transmitter, each for the specified word count. The BC then waits for the status word from the target terminal on completion of the transfer.

An exception to this RT-to-RT transfer method is necessary when a red RT has data required by a black RT. Here, data from the red RT is moved to the BC by an RT-to-BC transfer. Subsequently, the data can be sent to the black RT by a BC-to-RT transfer. This exception allows the BC to properly command the RBBI during data transfer.

Once the health of the RT has been determined, the BC:

a. Commands data transfer as required.

b. Commands two data transfers for identical information to be transmitted-first to TDP 1, followed immediately by a transfer to TDP 2 for the following units:

   1. SDC

   2. Doppler

   3. HSVD 1 and 2

   4. CSC

   5. ASC

RBBI control. The RBBI bus control system also incorporates the requirement for red/black data separation. Red and black data are separated by a set of redundant, fail-safe switches collocated in the RBBI Four differential control discretes from each TDP are required to control the RBBI. The RBBI is configured as a dual-redundant isolator with the two independent sections defined as RBBI1 and RBB12. TDP1 controls RBBI1 and TDP2 controls RBBI2. The four discretes are defined as follows:

a. **ISOE -** Selects RBBI1 if active from TDP1; selects RBBI2 if active from TDP2.

b. **ABSEL -** Selects B-bus of RBBI1 if active from TDPI; default is A-bus select. Selects B-bus of RBBI2 if active from TDP2; default is A-bus select.

c. **TDPOS -** Status line (health) from TDP1/2 shuts off associated RBBI data path if TDP failure is detected.

d. **RBTXE -** Command discrete from TDP1/2 that enables transmission from the red side of the isolator to the black side of the isolator.

The TDPOS signal is generated by the TDP BITE watchdog timer, while the ISOE, ABSEL, and RBTXE signals are derived from the 1553 control function.

The TDP, functioning as 1553 BC, commands the RBBI into one of two operational modes, defined as follows:

a. An active, unidirectional path is enabled from the black bus to the red bus. This is the normal or default mode of the RBBI.

b. An active, unidirectional path is enabled from the red bus to the black bus. This mode is commanded only when black data are present on the red bus and an RT on the black bus (RT address 21-26) is addressed by the BC.

Timing of TDP control signals to RBBI. The TDP sets the RBTXE on just prior to sending a command to the black bus RT. As soon as the message has been completed, RBTXE turns off, allowing the black RT to send its status to the BC. The BC then identifies the status word ending the clear data transmission and opens the RBBI switch. With the RBBI switch open, data transfer proceeds normally between red terminals.

70.2.4.6 Error detection and recovery. The 1553B module incorporates a dual-redundant bus architecture. Normal operation uses the designated A-bus for all bus transactions. Detection of a fault activates the backup bus (B-bus). The backup bus shall be activated for two reasons:

a. A fault in the A-bus or a connected RT that precludes the use of that bus.

b. A fault in the BC that prevents its disconnection from the bus.

In the first case, the normal BC (TDP 1) continues operation but on the alternate bus (B-bus). All system operations are conducted exactly as they were with no performance degradation. The strategy for retry is under TDP software control. After a detected fault (no response), the primary bus is retried three times prior to switching; then, in subsequent polling, retries are alternated between buses.

The inability of the BC to disconnect requires shutting down the controller and transferring bus control to TDP 2, which acts as the backup controller (BBC). This is automatic, but it is also indicated to the crew. The crew may override the automatic selection after it has occurred.

System tests. The TDP 1553 module is capable of participating in several levels of testing, including:

a. Operational readiness testing (ORT).

b. Status monitor (inflight) testing.

c. Avionics maintenance level testing.

The ORT is activated by the host processor and is divided into the following three sections:

a. The bus module microcontroller, memory, all registers, and module-resident buses are exercised. Loop-back is provided that permits testing as close to the module terminals as possible. Results are posted in a status register that is available to the host.

b. The TDP 1553 module exercises the interface between itself and the host.

c. All RTs are polled to determine the status of the mission avionics. Polling results are available to the host.

Failure handling. Several noncatastrophic bus failure modes exist that will be handled as follows:

a. **Transmit overrun protection -** A hardware timer is provided to automatically prevent a runaway transmit condition. This timer is activated at the beginning, and reset at the conclusion, of each transmission. If still active 768 us after the start of transmission, this circuit will inhibit further transmission.

b. **Transmitter shutdown (mode code 00100) -** This command causes the RT to disable the transmitter associated with the redundant bus; for example, a command may be issued on the B-bus to disable a malfunctioning RT on the A-bus. The RT must respond with a status word on the B-bus after obeying this command.

c. **Override transmitter shutdown (mode code 00101) -** This command causes an RT to enable a transmitter, which was previously disabled, on its redundant bus. The RT must respond with a status word after obeying this command.

d. **Error or no-response detection -** The BC detects errors or no response from two or more black bus RTs, using the same TDP and its RBBI, and then switches to an alternate bus using ABSEL discrete. If the problem persists, it switches to the alternate BC and its RBBI.

70.2.4.7 Special features. The main feature of the CV-HELO system is the RBBI that separates the red and black buses. As 1553B systems are applied to more applications, secure buses may become more common. CV-HELO polls its terminals periodically, but, within a polling cycle, the message transfers occur on demand. In this sense it is aperiodic.

70.2.4.8 Conclusions. The CV-HELO is still in development.

70.3 OV-1D MOHAWK.

70.3.1 Mission requirements. The Army OV-1D Mohawk aircraft is a fixed-wing special electronics mission aircraft (SEMA) that provides a variety of survillance functions using near real-time imagery of both fixed and moving targets. The information is immediately presented to the flight crew on a display or by hard copy and simultaneously linked to aground tactical command post for intelligence and exploitation purposes. In its side-Iooking airborne radar (SLAR) configuration, it can be used for visual and photographic detection as well as SLAR surveillance.

The Army has undertaken a block improvement program to upgrade the aircraft to incorporate an advanced avionics suite, including an advanced cockpit control, a dual standby-redundant 1553B multiplex data bus, and a multifunction CRT display system. The system provides redundant multiplex data bus control, air data processing, waypoint navigation and target storage, communication management, caution/warning/advisory navigation subsystem management, aircraft survivability equipment (ASE) and mission equipment (ME) subsystem management, and system maintenance functions.

The OV-1D multiplex system is built to 1553B Notice 1.

70.3.2 System architecture. The OV-1 dual standby-redundant 1553B architecture, shown in Figure 70-7, provides the path for message control and data traffic interconnecting 16 subsystems, all of which are equipped with embedded 1553B terminals. Included are:

a. ARC-164 UHF-AM radio set.

b. ARC-186 VHF-AM radio set.

c. Two ARC-201 VHF-FM radio sets.

d. ARC-199 HF-SSB radio set.

e. ASN-141 standard inertial navigation unit.

f. USN-2(V) standard attitude heading reference system (SAHRS) or ASN-143(V) attitude heading reference system (AHRS).

g. ASN-149(V)2 global positioning system (GPS).

h. ARN-118(V) airborne TACAN system via SCU.

i. APN-232 combined altitude radar altimeter.

j. APX-100 transponder set.

k. Data loader and recorder.

l. Two master controller processor units (MCPU).

m. AM-7189(A)/ARC improved VHF-FM (IFM) amplifier subsystem.

n. ASE remote terminal unit (RTU).

The system architecture provides for the installation of one of two navigation architectures. The global positioning system (GPS) provides the primary self-contained navigation capability. It supplies three-dimensional present-position, velocity, altitude, and waypoint data to the MCPU. The GPS transmits three-dimensional velocity to either the SAHRS or AHRS, which is used for velocity damping and accepts acceleration, velocity, heading, and attitude information from the INU. GPS also provides correction data to the INU.

70.3.3 System hardware.

70.3.3.1 Terminals. The subsystems to be integrated into the OV-1D data bus architecture were provided GFE to the integration contractor. (Table 70-V shows the manufacturer, function, and capability of each of the subsystems.) Therefore, each embedded RT provides different 1553 protocol capabilities. As a result of these differences, the use of the 1553B status bits and mode codes had to be individually described for each subsystem, as shown in figure 70-8.

Address selection is established by pin programming of an external connector on each RT. Five pins define the terminal address, the sixth pin is used for parity (except for the IFM), and the seventh pin is the return. GPS also provides correction data to the INU.

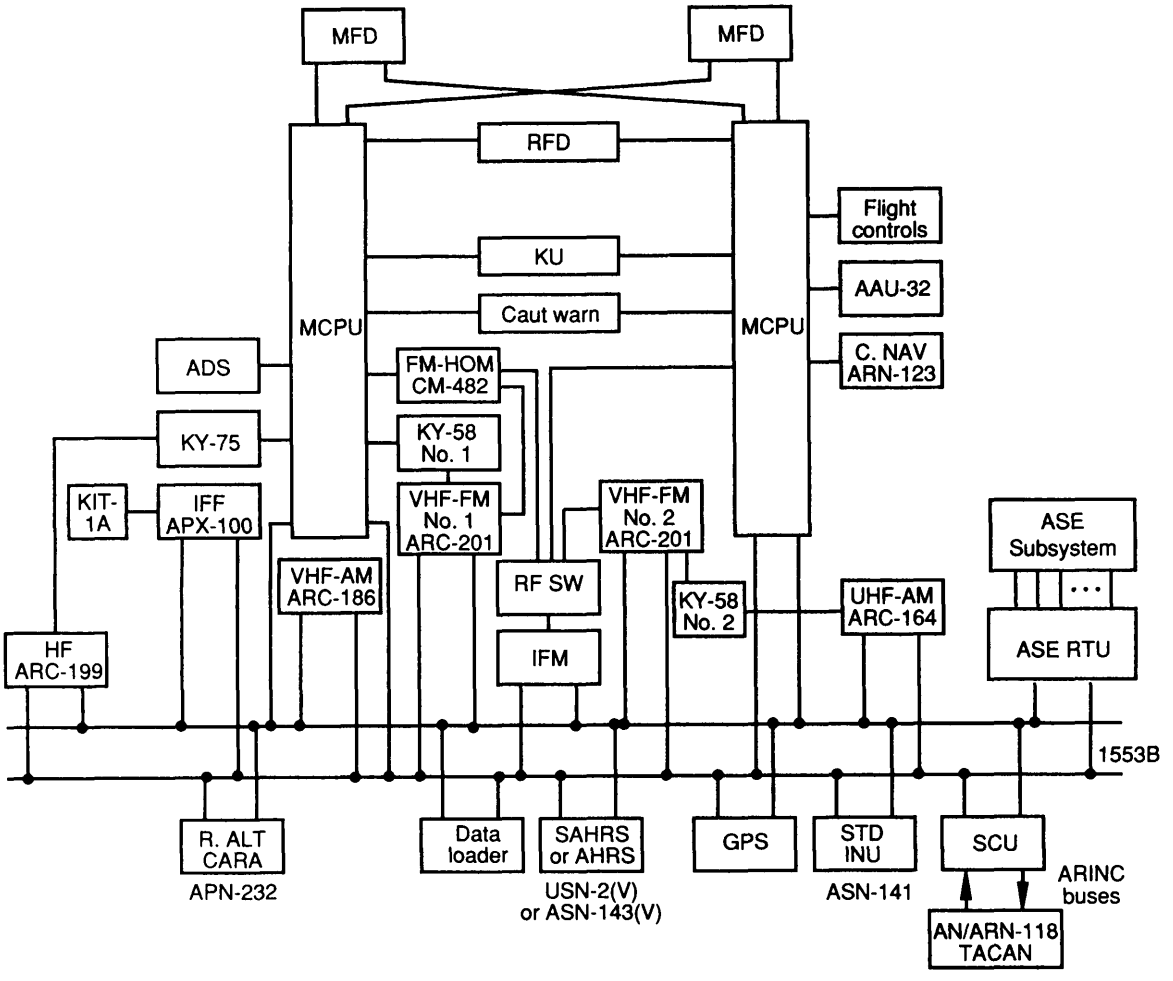


Figure 70-7. OV-1D System Architecture

The ASE RTU is the interface with the following ASE and mission equipment subsystems:

AN/APR-39	Radar warning receiver
AN/APR-44	Radar warning receiver
AN/ALQ-136	Radar jammer
AN/ALQ-147	IR jammer
AN/ALQ-156	Missile detection system
AN/ALQ-162	Radar jammer
M-130	General-purpose dispenser system
AN/AYA-10	Airborne data annotation system
AN/APS-94F	Side-looking airborne radar

Table 70-V OV-ID Subsystem Functions and Capabilities (Sheet 1 of 3)

UHF-AM Radio Set AN/ARC-164 The ARC-164 is a remote receiver-transmitter that provides AM modem communications capability on any of 7000 channels spaced at 25-kHz increments over a frequency range of 225.000 to 399.975 MHz. A separate guard receiver is provided for monitoring AM voice signals on the UHF emergency guard channel (a single frequency in the range of 238 to 248 Mhz).	Manufacturer;Magnavox Amplitude modulated (AM) voice; tone transmission (MCW); Secure speech interface; HAVE QUICK ECCM capability.
VHF-FM Radio AN/ARC-201 The ARC-201 radio specified herein will provide air-to-air and air-to-ground-to-air communication of voice and data, secure or plain text, in single channel (SC) or frequency hopping (FH) modes, Single Channel Ground and Airborne System (SINCGARS). The ARC-201 is a receiver/transmitter (R/T) that provides FM and external modem communications on any one of 2319 channels in the 30.000-to 87.975-MHz range in 25-kHz increments. In addition, a frequency offset tuning capability of -10kHz, -5kHz, +5kHz, and +10kHz is provided in the single-channel mode.	Manufacturer: ITT FM voice and secure speech, transmit/receive in 30.00 to 87.975-MHz frequency band; radio relay (retransmit); homing in the frequency band from 30.000 to 87.975 MHz, and SINCGARS frequency hopping (FH) in the frequency band from 30.000 to 87.975MHz. The R/T shall operate in aircraft installations as a remote-controlled receiver/transmitter and in conjunction with other Line Replaceable Units (LRUs).
VHF-AM Radio Set AN/ARC-186 The VHF2 radio provides air-to-air and air-to-ground-to-air communication of voice and data, secure or plain text, in single channel mode. The ARC-186 is a receiver/transmitter (R/T) that provides AM and external modem communications on any one of 1440 channels in the 116.000- to 151.975-MHz range in 25-kHz increments. The range between 108.000 and 115.975 MHz is receive only.	Manufacturer: Rockwell-Collins AM voice, transmit/receive in the 116.000- to 151.975-MHz frequency band; AM voice receive only in the 108.000-to 115.975-MHz frequency band; radio relay; and ADF in the frequency band from 108.000 to 151.975 MHz. The R/T shall operate in aircraft installations as a remote-controlled receiver/transmitter and in conjunction with other Line Replaceable Units (LRUs).
Amplifier, Radio Frequency AM-7189(A)/ARC Improved VHF-FM Amplifier Subsystem The IFM is a power amplifying accessory to be used with VHF-FM radios that are designed to operate in the central battle area from helicopters using nap-of-the-earth (NOE) flight techniques. The subsystem will amplify signals from a standard VHF-FM radio in the frequency range of 30 to 88 MHz to an effective radiating power of 2.5 to 6 watts (low), 10 to 18 watts (normal), or 35 to 49 watts (high).	Manufacturer:Rockwell-Collins Selectable power levels which allow an aircraft on nap-of-the-earth tactical missions to operate on a parity with existing ground communications systems.

Table 70-V OV-1D Subsystem Functions and Capabilities (Sheet 2 of 3)

HF-SSB Radio Set AN/ARC-199 The ARC-199 is a high-frequency, single-sideband radio with selectable output power levels of 4, 40, and 150 watts PEP (peak envelope power). Frequency of operation from 2.0 to 29.9999MHz. Transmit and receive frequencies are programmable in 100-Hz increments on 21 presettable channels, for a total of 280,000 possible frequencies. Emission modes available are: upper and lower sideband (USB,LSB), amplitude modulation equivalent (AME), and modulated carrier wave (MCW).	Manufacturer: King Radio Corporation Selective squelch, or selective addressing (SELADR); retransmission of data or voice; built-in-test (BIT) securable with TSEC/KY-75 voice security equipment.
Transponder Set AN/APX-100 The AN/APX-100 is a space diversity transponder, functioning to receive the RF interrogations from two antennas and to transmit the reply to the antenna from which the stronger interrogation signal was received. The AN/APX-100 provides six modes of interrogation and reply: Modes 1, 2, 3/A, C, test, and 4.	Manufacturer:Bendix Mode 1 permits a total of 32 different codes; Mode 2 permits a total of 4096 codes (aircraft number); Mode 3A provides a possible 4096 codes (flight status in formation); Mode C provides a total of 2048 codes (aircraft altitude); Mode 4 codes are under the control of an external computer; a possible 4096 codes are provided in the test mode.
AN/USN-2(V) Standard Attitude Heading Reference System The USN-2 is a strapdown , self-contained, all-attitude set that provides analog and digital outputs of vehicle pitch, roll, heading, angular rate, angular acceleration, linear acceleration, velocity and position.	Manufacturer: Singer-Kearfott. NORTHROP The SAHRS accepts an external velocity reference for velocity damping. The SAHRS is provided position from the INU through the MCPU. The SAHRS can use position for inflight gyro compassing and magnetic variation lookup.
Global Positioning System (GPS) The ASN-149 provides the primary self-contained navigation capability.	Manufacturer: Rockwell-Collins The GPS supplies velocity to the SAHRS for velocity damping, correction information to the INU, and data to the MCPU for a non-precision landing approach and CONUS NAV. The GPS accepts acceleration, velocity, position, heading, and attitude information form the INU and accepts waypoint information from the data loader via the MCPU.

Table 70-V OV-ID Subsystem Functions and Capabilities (Sheet 3 of3)

AN/ASN-143(V) Attitude Heading Reference System The ASN-143 is a strapdown system wherein the gyro and accelerometer sensors are mounted in a fixed position with respect to the user vehicle. It is a self-contained, all-attitude LRU that provides digital outputs of vehicle dynamic state data (i. e., pitch, roll, heading, angular, rate, angular acceleration, linear acceleration, velocity, and position In MGRS and lat./long, coordinate systems.)	Manufacturer: Litton Guidance and Control System The AHRS may be used as a back-up source for velocity, position, and low-accuracy free-nertial navigation. Position data may be input in either UTM or lat./long. Position outputs are provided in both UTM and lat./long.
CV-3739/ASN-132(V) Signal Data Converter Unit The SCU performs the data processing as required to convert the RT-1159A TACAN receiver-transmitter (R/T) two-wire tertiary serial data inputs and outputs, in conformity with ARINC characteristics, to the corresponding serial data formats on MIL-STD-1553 for transfer to and from external systems.	Manufacturer: Litton The RT-1159/A airborne TACAN system, through the SCU, provides slant-range distance, relative bearing, course deviation, to-from, and audio identification Information for use by the flight crew. The system produces distance information, bearing, course deviation, and to-from information with respect to a suitably equipped, cooperation aircraft. The TACAN system supplies the navigation information to instruments and to external systems.
Data Loader The DL is a Data Transfer System that consists of three main components: a portable, self-contained memory cartridge, a ground based terminal, and an onboard receptacle. The memory cartridge is the means by which data is transferred back and forth between the ground based terminal and the onboard receptacle. The onboard receptacle transfers data to and from the operator and onboard avionic equipment during fright.	Manufacturer: N/A The type of data stored on the memory cartridge are navigation flight plan, navigation waypoints, target avoidance areas, communication frequency list, mission checklist, and a status/BIT failure report.
AN/ASN-141 Standard Inertial Navigation Unit The AN/ASN-141 is an inertial navigation unit (INU) that provides present position, waypoint/markpoint insertion, sign status, built-in-test (BIT), attitude, true heading, velocity, and position update.	Manufacturer: Litton The INU supplies 3-dimensional velocity, acceleration, position, altitude, and steering data to the MCPU. It receives updates from the MCPU computed from very accurate navigation data supplied by the GPS to correct INU navigation outputs. The INU provides acceleration, velocity, position, heading, and attitude information to GPS.
Combined Altitude Radar Altimeter (CARA) AN/APN-232 The CARA is a receiver/transmitter (R/T) that functions as the emitter and receptor of radio frequency (RF) energy, within the frequency band of 4200 and 4400 MHz. It also processes the altitude information contained in the received signal.	Manufacturer: Clifton Precision The CARA, as a minimum, shall provide accurate indication of absolute height of an aircraft over a range of 0 to 50,000 feet above prevalent terrain. The CARA shall transmit an RF signal to the prevalent terrain, receive the reflected signal, and derive and display an indication of height from 0 to 50,000 feet.

		Terminals														
Mode code function	Associated data word	ARC-164	ARC-201	ARC-186	IFM	ARC-199	APX-100	ASN-141	USN-2	ASN-149	Data LDR	ASN-143	ARN-118	ASE RTU	APN-232	MCPU
Synchronize	No							X		X		X				X
Transmit status word	No	X	X	X	X	X	X		X	X	X	X	X	X	X	X
Initiate self-test	No	X	X					X			X			X		X
Transmitter shut-down	No	X	X	X	X	X	X		X	X	X			X	X	X
Override trans. shutdown	No	X	X	X	X	X	X		X	X	X			X	X	X
Inhibit terminal flag bit	No	X	X			X				X				X		X
Override inhibit term. flag bit	No	X	X			X				X				X		X
Reset remote term.	No	X	X	X		X		X	X	X	X		X	X	X	X
Transmit vector word	Yes										X			X		X
Synchronize	Yes									X						
Transmit last command word	Yes	X	X			X			X	X	X	X		X	X	X
Transmit BIT word	Yes	X	X							X	X			X		X
Status flag function																
Message error		X	X	X	X	X	X		X	X	X	X	X	X	X	X
Service request						X					X			X		
Busy		X	X				X		X				X			
Subsystem flag		X	X	X		X			X	X			X	X	X	
Dynamic bus																X
Terminal flag		X	X	X		X			X	X			X	X	X	X

Figure 70-8. MIL-STD-1553 Mode Code and Status Flag Usage in the OV-1D System Architecture

70.3.3.2 Bus controller. The OV-1 bus controller function is performed by the OV-1 control/display system, which consists of two identical MCPUs (MCP1 and MCP2). For the normal mode of operation, MCP1 is the BC and MCP2 is the BBC and an RT. An MCPU is capable of performing as either the BC or an RT.

Each MCPU, depicted in Figure 70-9, contains two SDP-175 central processing units (CPUs). The processors are built around a 2901 bit-slice circuit and contain 16-bit address and data buses. Each processor is capable of executing 500K to 800K instructions per second, depending on the instruction mix. Eight priority-encoded interrupts are available for each CPU. Each CPU has 56K (16-bit) words of erasable programmable read-only memory (EPROM) available for program storage, 8K (16-bit) data words of random access memory (RAM), and 2K (16-bit) data words of nonvolatile memory for long-term data storage. The CPUs share a three-port RAM containing 8K (16-bit) data words, 4K of which can be accessed by the bus interface circuitry using a round robin polling scheme for access.

Two multifunction displays (MFDs) provide the operator interface. These displays can be configured as a horizontal situation display (HSD), vertical situation display (VSD), or information display such as communications control and status or navigational way point/flight plan. The MFD is an 875-line video raster scan CRT with a 4:3 aspect ratio. Information to be displayed is received from the MCPU vector generator CCA. Each MFD is capable of being driven by either MCPU, with the video source switch selectable by the operator.

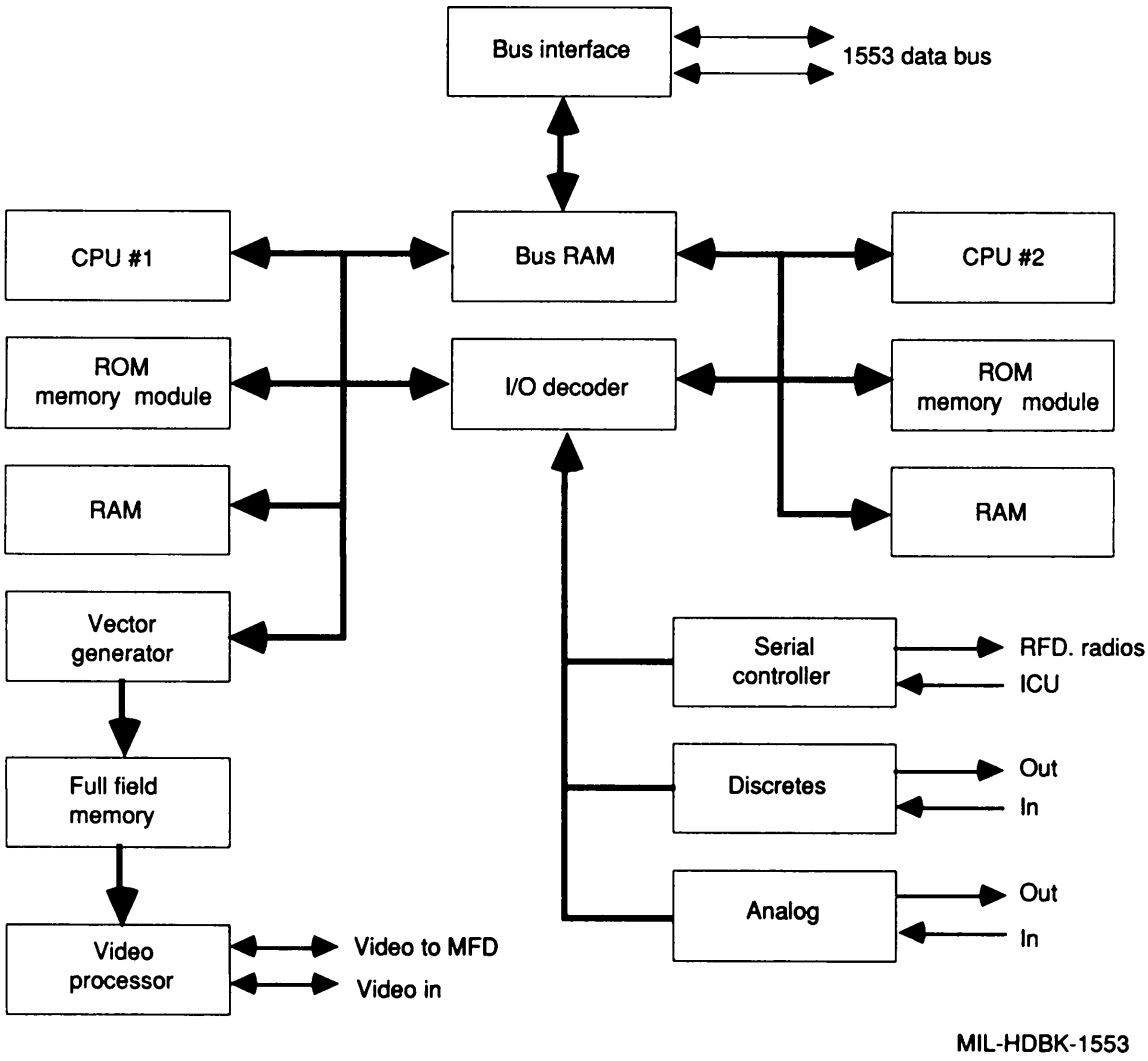


Figure 70-9. MCPU Architecture

70.3.4 System control. The OV-1 multiplex system architecture, depicted in Figure 70-7, consists of a dual standby-redundant 1553 multiplex data bus, which provides the information path for 16 embedded terminals, connected to the bus using transformer-coupled stubs. Two MCPUs provide the primary and BBC functions.

70.3.4.1 Data transfer formats. The data bus is controlled through use of the following 1553 information transfer formats:

a. Bus controller to remote terminal (BC to RT).

b. Remote terminal to bus controller (RT to BC).

c. Remote terminal to remote terminal (RT to RT).

d. Mode command without data word.

e. Mode command with data word.

70.3.4.2 Mode code use. Only a subaddress/mode field of 00000 is utilized as an indication that the data word count/mode code field contains a mode code.

70.3.4.3 Status word use. Figure 70-8 shows the individual status word capabilities of each RT. Refer to 70.3.4.6 for BC use of this status.

70.3.4.4 System startup. MCP 1 is always started as the BC, and MCP 2 is the BBC. At the beginning of each minor frame, a sync mode code is sent to the BBC.

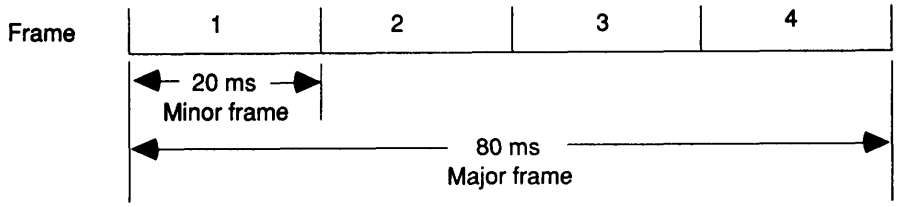
70.3.4.5 Message processing. The data bus is controlled within the frame structure depicted in Figure 70-10. This frame structure is characterized by a major frame of 80 ms duration, which is composed of 20-ms minor frames. Therefore, the maximum data transfer rate over the bus is 50 Hz.

In normal data collection operation (transmit message), all information transfers use the RT-to-RTformat over the primary data bus, with the receiving terminal being the BBC. The BC, after issuing a command, monitors the bus and collects all the data words, as well as the status words, allowing both MCPUs to have simultaneous access to subsystem data without increasing the data bus loading. Bus loading in any given 20-ms period is limited to a maximum of 80% during normal fault-free operation. Typical message traffic for normal operations is depicted in Figure 70-11.

At the beginning of each time period, the transmit command sequence togather data from subsystems on the data bus is initiated within the BC by a real-time interrupt. Subsequent transmissions are controlled by an interrupt service routine. The receive command sequence to output data to the various subsystems on the bus are subsequently initiated so as to allow sufficient time for the completion of the messages before the end of the frame.

70.3.4.6 Error detection and recovery. The A-bus is used initially for all data transfers (except testing). On detection of an error, the system is switched to the standby bus (B-bus) for subsequent transfers of all messages with that subsystem. As subsequent errors are encountered, transmission is switched back and forth between the A-bus and B-bus, and error counters are incremented. Any message that has failed (protocol or no response) is not retransmitted during the same minor frame in which that message was originally sent.

The BC periodically (once every 20-ms minor frame) tests the communications data path between the two MCPUs by commanding a data wraparound message. This message consists of a receive command of six data words to the RT MCPU, followed by a transmit command on the same data bus. The bus controller performs a bit-by-bit comparison of the transmitted and received data, and, on detection of an error,



Frame	1 (20 milliseconds)
	MCPU-MCPU transfers
	GPS
	INU
	CARA
**	AHRS
	GPS and INU platform corrections
Frame	2 (20 milliseconds)
	MCPU-MCPU transfers
*	Radio 1
*	Radio 2
**	SAHRS/AHRS
	GPS-INU transfers
	GPS and INU platform corrections
Frame	3 (20 milliseconds)
	MCPU-MCPU transfers
	GPS
	INU
*	Radio 3
*	Radio 4
**	GPS-SAHRS transfers
*	TACAN (SCU)
**	AHRS
	GPS and INU platform corrections
Frame	4 (20 milliseconds)
	MCPU-MCPU trtansfers
*	Radio 5
*	IFM
	IFF
	Mission
**	AHRS
	GPS and INU platform corrections

* Messages may be only aperiodic.
** These messages are dependent on which LRU (SAHRS or AHRS) is installed.
x MCP1 or MCP2 depending on direction of data flow.

Figure 70-10. OV-1D Frame Structure

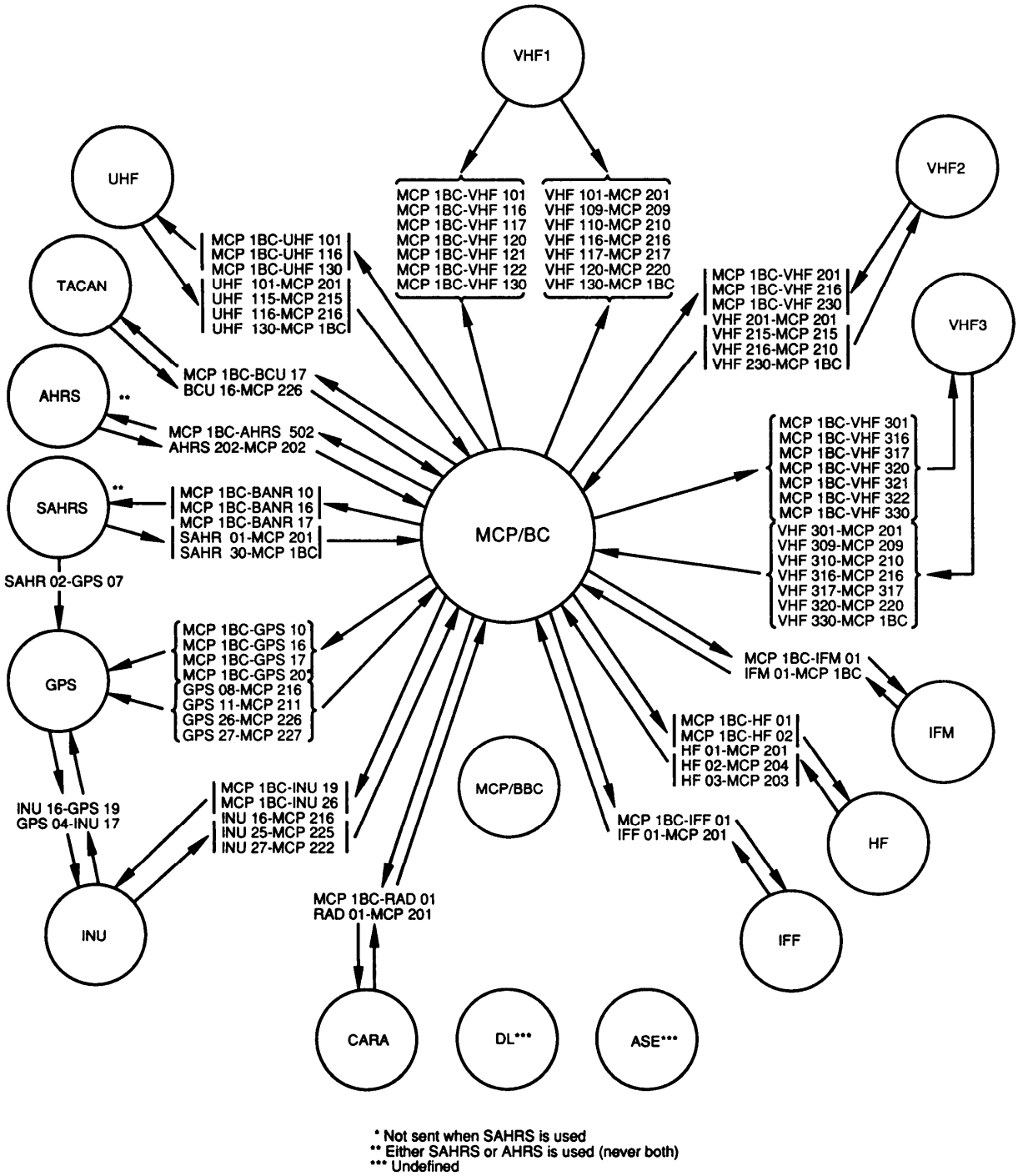


Figure 70-11. Typical OV-1D Message Traffic During Normal Operations

increments an error counter. When the error counter reaches eight on a particular bus, a bus failure flag is set. This flag is cleared following an error-free transmission over the failed bus between the MCPUs. The BC alternates transmission of this test sequence between data bus A and data bus B in order to continuously verify the integrity of both data buses.

In addition to monitoring the bus for protocol errors, the BC examines each status word for help in determining the state of the subsystem and the health of the system. Status bits tested include the busy, terminal flag, and subsystem bits. If the busy bit is set, the message containing the same data will continue to be transmitted in its assigned timeframe until received by the subsystem. The setting of the terminal flag or subsystem bits by a subsystem will cause caution and warning indicators to be set for that subsystem.

The BC monitors itself via responses on the data buses. If in a 40-ms period the BC receives no valid messages (all messages fail protocol test or no response), the BC will automatically become the BBC. The BBC continuously monitors the data bus for a failed or inactive BC, defined as a BC that does not transmit any command for 80 ms.

When either MCPU fails, data are transferred directly between the RT and the active BC, using the appropriate 1553B information transfer formats. These same information transfer formats are used during normal operation for the output of data (receive messages) to subsystem terminals and for information transfer between the MCPUs.

70.3.4.9 Special features. Two aspects of the OV-1D system design are instructive. First, the differences in the RT capabilities with respect to mode codes and status word bits make the BC design more complex, but a simplified error-handling setup reduces this problem.

The second aspect that deserves recognition is the method of maintaining BBC data. Advantages of using the RT-to-RT information transfer method from an RT to the BBC include (1) the BC and the BBC both receive the information from the RT simultaneously, preventing potential problems of different data in the BC and BBC, and (2) bus traffic is reduced.

70.3.4.10 Conclusions. The multiplexed OV-1D is presently in flight test.

70.4 AH-64A APACHE ADVANCED ATTACK HELICOPTER

70.4.1 Mission requirements. The AH-64A Apache, developed by McDonnell Douglas Helicopter, was the first production Army aircraft to employ a 1553A multiplex data bus. The mission of the AH-64A Apache is to deliver antiarmor and area-suppression fire in day, night, and adverse weather.

The Apache is a twin-engine, four-bladed helicopter operated by a tandem-seated crew of two. To assist the Apache in performing it's mission requirements, the avionics, controls and displays, and the visionic and weapon subsystems have been integrated. The integrated avionic subsystems include the doppler navigation system (DNS) and the attitude heading reference system (AHRS). The visionic subsystems include the pilot night vision system (PNVS) with forward-looking infrared sensor, a target acquisition and designation system (TADS) with laser designator, and an integrated helmet and display sighting system (IHADSS) with associated symbol generator. Aircraft control is provided by the digital automatic stabilization equipment (DASE) computer, including a limited authority control of pitch, roll, and yaw axes, and a backup control system in the event of a mechanical linkage failure. The Apache integrated weapons system includes the fire control computer (FCC), Hellfire missiles, 2.75-in aerial rockets, and a 30-mm chain gun.

70.4.2 System architecture. The AH-64A multiplex system is used primarily to integrate the Apache weapon and visionic systems, including stores management, weapon fire control, and weapon controls and displays. The multiplex system provides a flexible, dual standby-redundant interface.

70.4.2.1 Data bus topology. A block diagram of the Apache multiplex data bus system is shown in Figure 70-12. The multiplex system consists of:

a. Dual standby-redundant data buses.

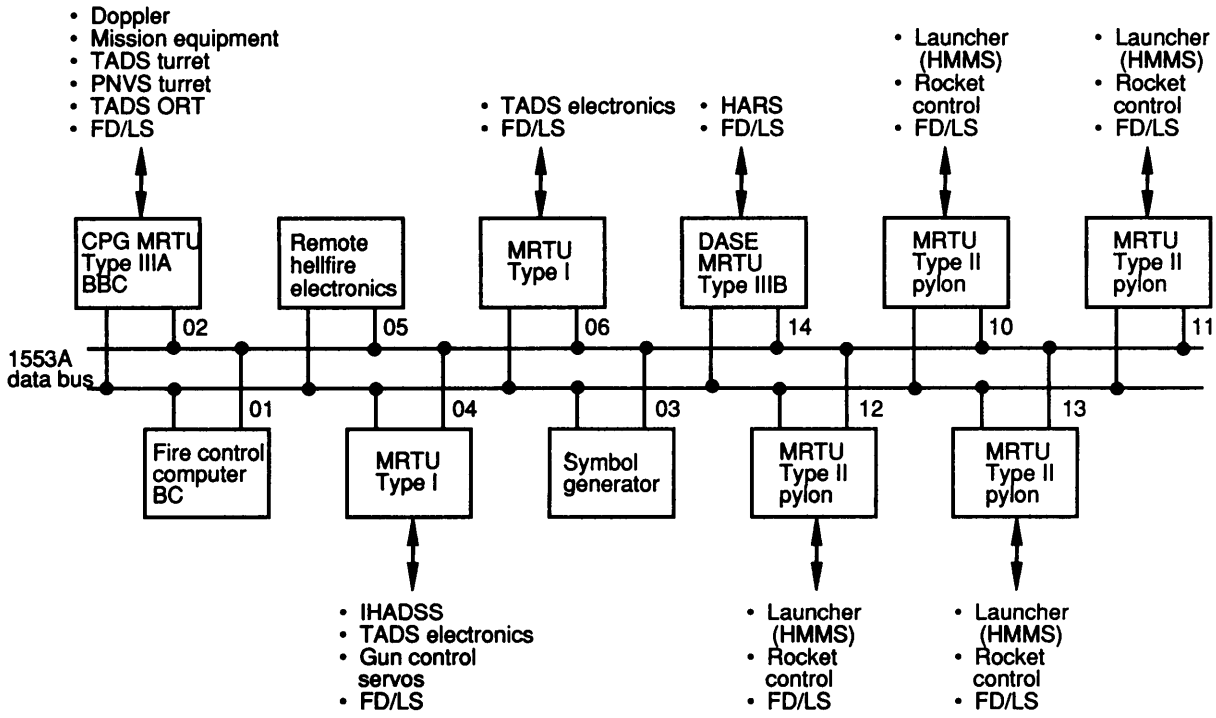
b. A primary BC located in the fire control computer.

c. A symbol generator.

d. A remote Hellfire electronics (RHE) unit.

e. Four pylon MRTUs (type II), one in each pylon, to interface with the missile and rocket subsystems.

f. Two general-purpose MRTUs (type I) located in the right hand and left hand forward avionic bays (FAB).



TADS:	Target Aquisition/Designation System
PNVS:	Pilot Night Vision System
DASE:	Digital Automatic Stabilization Equipment
FD/LS:	Fault Detection and Location System
ORT:	Optical Relay Tube
HARS:	Heading and Attitude Reference System
HMMS:	Hellfire Modular Missile System
CPG:	Copilot/Gunner
MRTU:	Multiplex Remote Terminal Unit
BBC:	Backup Bus Controller
BC:	Bus Controller
IHADSS:	Integrated Helmet and Display Sighting System

Figure 70-12. AH-64A Multiplex System Block Diagram

g. A special-purpose MRTU (type IIIB) containing the DASE computer.

h. A secondary (backup) BC located in the copilot/gunner (CPG) MRTU (type IIIA).

i. Twenty-two data link terminal units (DLTUs).

The subsystems receiving or transmitting data via the multiplex data bus areas follows:

a. Fire control computer (FCC).

b. Doppler navigation system (DNS).

c. Target acquisition and designation system (TADS).

d. Pilot night vision system (PNVS).

e. Integrated helmet and display sight subsystem (IHADSS).

f. Hellfire missile system and control.

g. Gun control.

h. Rocket control.

i. Heading and attitude reference system (HARS).

j. Symbol generator (SG).

k. Cockpit and control stick switches.

l. Air data sensor (ADS).

m. Digital automatic stabilization equipment (DASE).

n. Electronic attitude director indicator (EADI).

o. Fault detection and location system (FD/LS).

The various subsystems and functions that interface with a typical terminal are indicated in Figure 70-12 using the AH-64A as an example. Figure 70-13 illustrates the location of the terminals within the helicopter. The primary data bus is routed along the left side of the aircraft, while the secondary data bus is routed along the right side of the aircraft. Critical signals are routed into separate MRTUs via separate signal paths, precluding the loss of critical functions by a failure within a single MRTU. The primary and backup controllers have been isolated and located in separate compartments to increase survivability. The primary controller is located in the right side forward avionic bay (FAB), while the backup controller is located in the CPG crew station compartment.

70.4.3 System hardware.

70.4.3.1 Media. Only transformer coupling (long stubs) is used on the Apache. Each of the dual-redundant data buses consists of a low-loss, twisted, shielded, 24-gauge, Teflon-insulated wire pair. All connections to the data bus use small coupler units called data link terminal units (DLTU). The DLTUs provide the system with short-circuit isolation, impedance matching, and cable termination. Each DLTU supplies a coupling

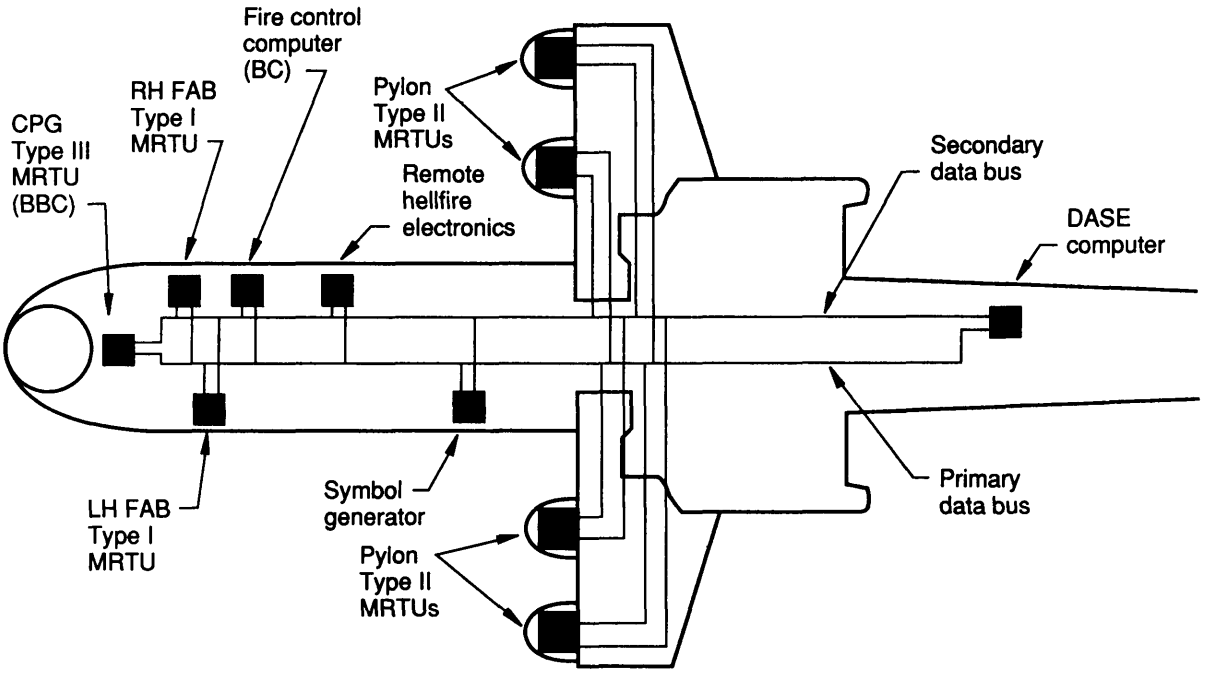


Figure 70-13. AH-64A Terminal Locations

transformer, isolation resistors, and termination resistors. Only the DLTUs located at each end of the data bus cable are wired to the termination resistors. One DLTU is used for each bus connection to a terminal.

70.4.3.2 Remote terminal. Eleven terminals are connected to the multiplex data bus. Three of these terminals (the fire control computer, remote Hellfire electronics unit, and symbol generator) were specifically designed for the Apache and have embedded 1553A interfaces. All other terminals are MRTUs designed to provide the interface between the 1553A data bus and the non-1553 systems and subsystems.

70.4.3.2.1 Multiplex Remote Terminal Units (MRTUs). Developed in the late 1970s prior to an abundance of 1553 interfaces being embedded within subsystems, the Apache multiplex system consists primarily of multiplex remote terminal units (MRTU) that are the interface between equipment that is not 1553 compatible and the data bus. Eight MRTUs are used as interfaces, and they process more than 1,300 signals to and from the subsystems that are not 1553 compatible. Where possible throughout the aircraft, subsystem interfaces have been standardized. The MRTU interface signals include bidirectional, serial, ac inputs and outputs; dc inputs and outputs; 28V discrete inputs and outputs; 5V discrete inputs and outputs; switch closure inputs; and ARINC 582-4 serial signals.

The MRTUs are designed and manufactured by the Sperry Defense Systems Division of Honeywell. The MRTUs, identified as types I,II, III, and DASE, provide an assortment of input and output signals which have been standardized for use throughout the Apache aircraft. The characteristics and signal mix for each MRTU are provided in table 70-VI.

All circuitry within the MRTUs is on standard 4- by 6-in circuit cards. These circuit cards are interchangeable between all MRTUs. The type II MRTU was designed to mount in the stores pylon, so it has a unique skewed packaging. Circuit cards are mounted vertically in the type I, III, and DASE MRTUs and horizontally in the type II MRTU. Keying is provided on the motherboards to prevent installation of a circuit card in a noncompatible (similarly wired) slot.

The power supplies are interchangeable between the types I, IIIA, and IIIB units. The unusual form factor and

Table 70-VI. MRTU Characteristics

MRTU	I	II	III	DASE
Dimensions				
Height (in)	5	3.1	5	5
Width (in)	7	4.28	7	7
Depth (in)	7.5	8.8	10.25	10.25
Weight (lb)	9	4	12.5	12.5
Power (W)	25	16	57	60
1553 interface	RT	RT	RT/BC	RT
Input/output				
Bidirectional serial	3	2	3	2
ac input	4	-	4	-
ac output	8	-	-	-
dc input	20	8	20	24
dc ouput	20	4	20	8
28 v input	24	-	24	16
28 v output	16	8	16	8
5 v input	48	-	48	32
5 v output	56	8	56	8
Switch closure	48	-	48	-
ARINC 582-4	-	-	1	-
Total I/O	247	30	240	82

limited current requirements mandated a special power supply be designed for the type II MRTU. Each MRTU is designed for conventional cooling and is hard-mounted without shock absorbers.

Each MRTU contains sufficient built-in-test (BIT) circuitry to detect 95% of all failures (weighted by failure rate) within itself. In addition, software contained within the primary and secondary controllers supports fault isolation and reporting.

70.4.3.2.2 Other remote terminals. Two other terminals, specifically designed for the Apache, are connected to the multiplex system. These terminals are the remote Hellfire electronics (RHE) unit and the symbol generator (SG).

The RHE receives fire control parameters, operator selections, and TADS and laser data from the bus. It transfers these data to the missiles. Missile status and launcher errors are received from the missiles and transferred to the BC. The RHE is located in the right hand FAB.

The SG receives equipment status, mission data, coded display symbology, and video switching data from the BC and sends it to the IHADSS, TADS, or electronic attitude display indicator (EADI) for display. The SG is located in the left hand FAB.

70.4.3.3 Primary bus controller. The primary bus controller (BC) resides in the fire control computer (FCC).

The FCC performs as the mission computer for all integrated functions. The FCC contains no subsystem I/O with the exception of handshake signals passed between it and the backup controller. The FCC (MECA-43) is designed and manufactured by Teledyne Systems. It contains a hybrid digital microcomputer that is a 16-bit microprogrammed, parallel, 2's complement processor with 32K words of PROM and 4K words of RAM. Bus control software requires less than 350 words of code and 2K words of data buffering. A battery is provided to "hold up" the RAM in the event of power interruption or when the system power is turned off.

The 1553 interface circuitry is designed to enable the FCC to function as either a BC or a RT. The interface is hybridized for minimum weight and size. Within the 1553 interface circuitry there are three functionally unique hybrids: (1) the driver-receiver, (1) the multiplex terminal unit (MTU), and (3) the device control unit (DCU). Figure 70-14 is a block diagram of the 1553 interface circuit.

The driver-receiver hybrid couples the 1553A data bus to the MTU hybrid. Bus switching is under software

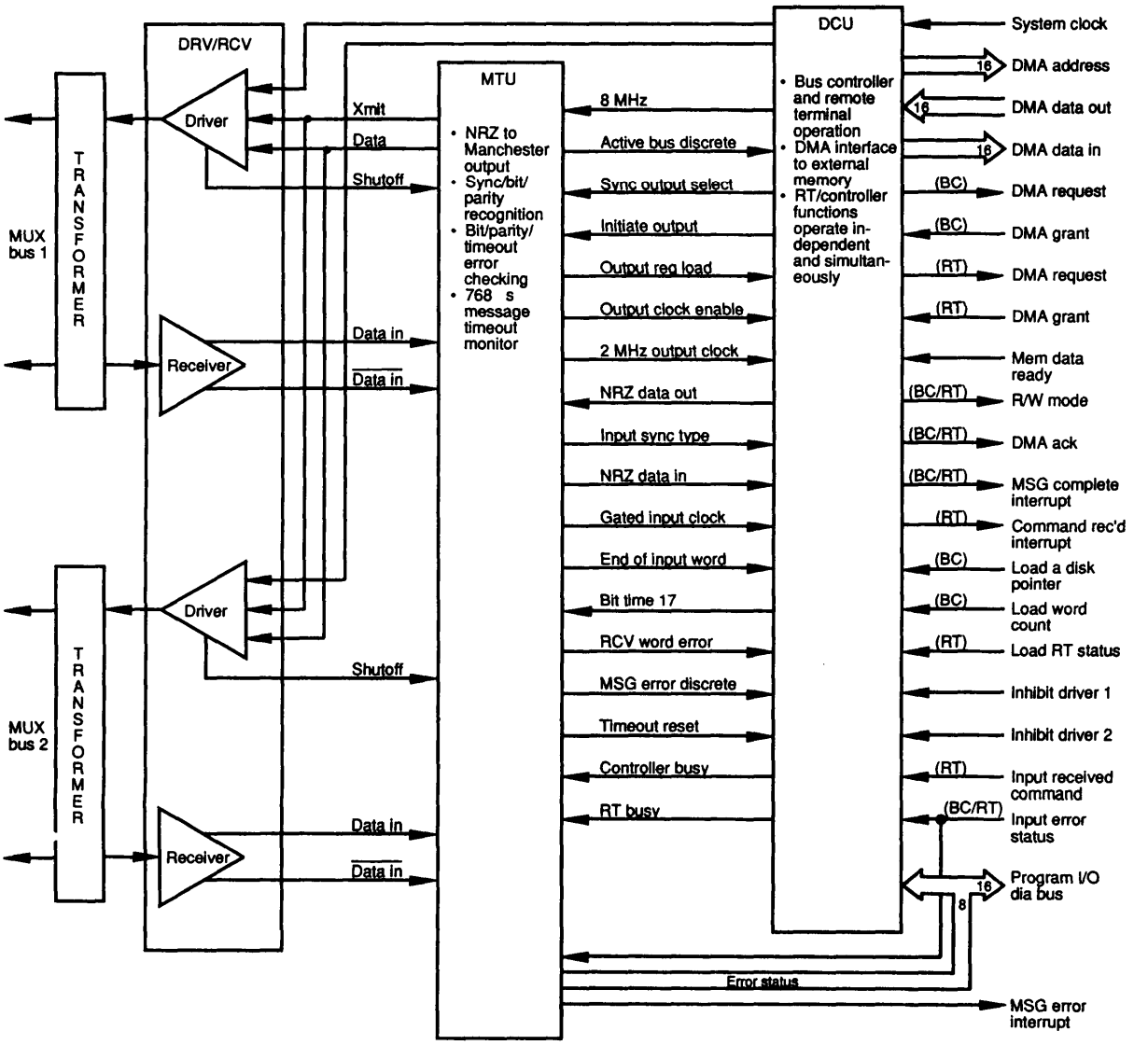


Figure 70-14. AH-64A 1553A Hybrid Bus Controller Interface

control. Isolation resistors and the coupling transformer are external to the hybrid. A separate driver-receiver is used for each data bus.

The MTU becomes the interface between the driver-receiver and the DCU by performing all bit and word serialization to and from the data bus. The MTU accepts Manchester-encoded data from the driver-receiver and sends NRZ data to the DCU. Similarly, it takes NRZ data from the DCU and supplies Manchester-encoded data to the driver-receiver (both drivers). Input and output occur independently and simultaneously, thus providing a full duplex serial interface with the DCU. The MTU also performs bit error checking, word parity checking, and a total message length time check. A deadline discrete is also sent when there is no traffic on either bus for a time exceeding 65.5 ms.

The DCU performs those functions required of a BC or RT for message processing. The DCU is responsible for all message input and output between the MTU and the subsystem memory. The computer (MECA-43) controls the operation of the DCU by initializing the bus control logic via two control words. This initialization includes the address of the message list in memory, the number of words (command and data) to be transmitted, and the number of words (data and status) to be received (see figure 70-15). From this, the DCU also provides the necessary subsystem memory addressing (up to 64K for BC operation and 2K for RT operation) and next message queuing for continuous Controller operation. The DCU also provides a message error register with interrupts to the subsystem computer and a register for the last command word operated on.

The RT operations of the DCU are performed without computer intervention other than initialization, specifying

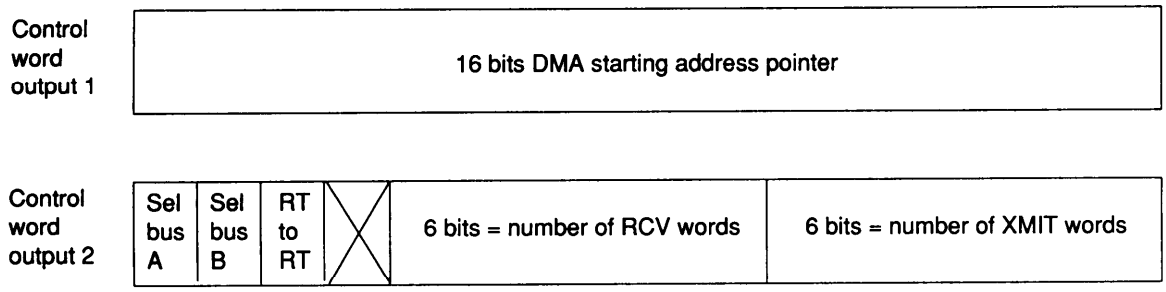


Figure 70-15. DCU Control Words

the terminal address, providing a memory buffer block, and setting the bits within the 1553A status word. The five most significant bits of the DMA address define which 2K memory block the messages are to be buffered in.

The DCU is capable of independently and simultaneously operating as a BC and an RT. Separate DMA channels are provided for both controller and RT operation. This allows the FCC to "talk" to itself as a means of providing a closed-loop self-test capability.

70.43.4 Backup bus controller. The backup bus controller (BBC) is contained within the type IIIA MRTU. This unit is designed and manufactured by the Sperry Defense Systems Division of Honeywell. The BBC computer (SDP-175) is based on a bit-slice microprogrammed, digital 2's complement processor with 24K of PROM and 2K of RAM. Bus control software requires less than 250 words of code and approximately 1.6K words for data buffering. In addition to backup bus control, the BBC provides the Apache with a degraded mode of mission computer functions (i.e., less accurate fire control) in the event of an FCC failure.

The BBC is unique in it's design in that, while the computer is located in the same housing as the RT, it is

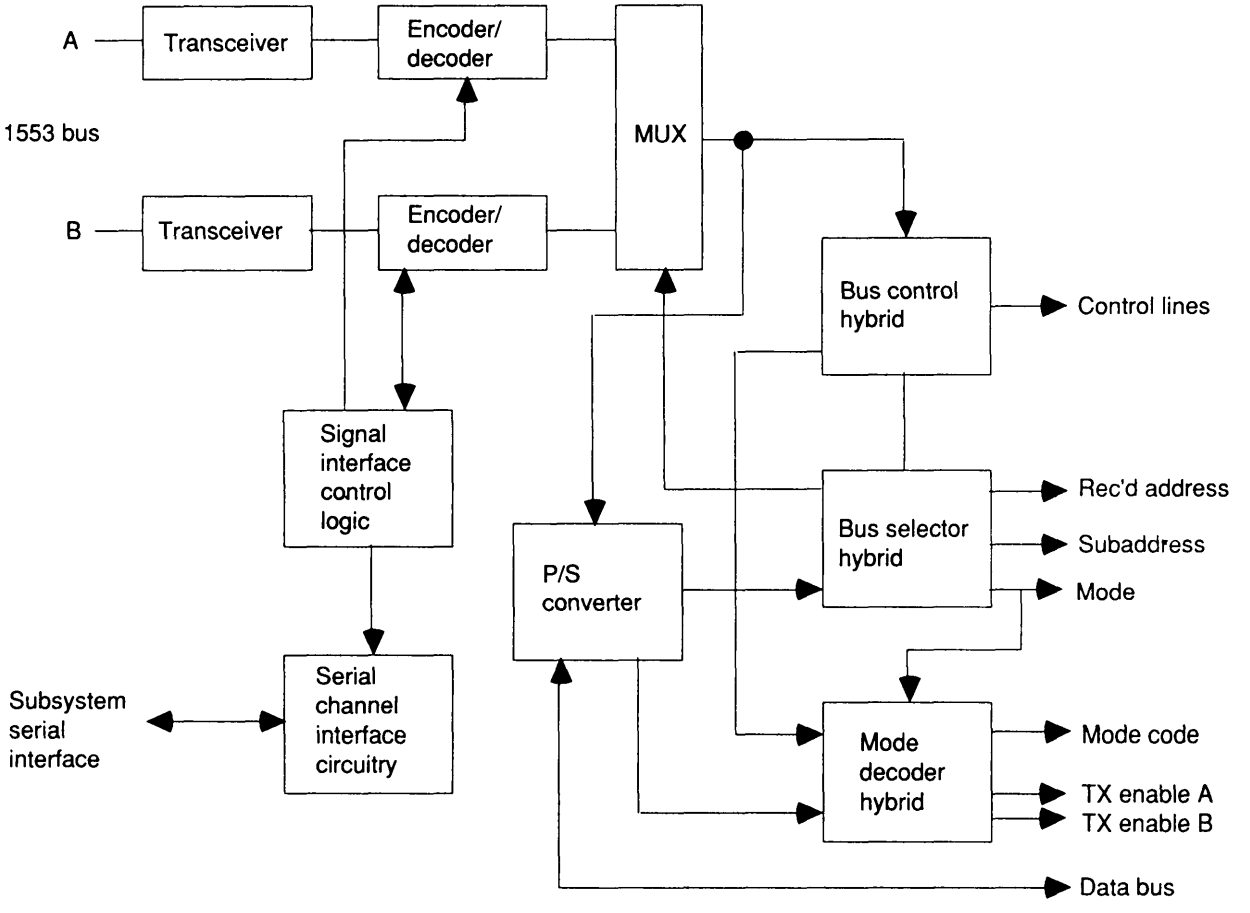


Figure 70-16. AH-64A Backup Bus Controller Block Diagram

functionally separate from the I/O subsystem interfaces at the terminal. This means that, for the BBC to communicate with a subsystem connected to the terminal, it must issue a command onto the data bus as if the terminal were located elsewhere in the system. The BBC and RT functions are isolated in such a manner that the RT cannot determine whether it is receiving a command from the primary or backup controller. Both the BBC and RT functions transmit their information on the data bus and respond as though receiving information from a source outside their own housing. This functional separation allows either to operate in the case of a failure in the other, barring a failure of a physically shared component (i.e., power supply or bus interface electronics).

A block diagram of the BBC is shown in figure 70-16. While the BBC is in the standby mode performing as an RT, the BBC computer is basically idling. With the exception of checking the data bus for "dead" time and monitoring the handshake discretes with the FCC, the BBC computer is limited to performing test functions on itself. This limitation is due to processor inability to access memory associated with the terminal functions resulting from the isolation previously mentioned.

When the BBC is in the bus control mode, the SDP-175 computer processes the same message list as the FCC. The FCC is not communicated with. The SDP-175 processor initializes the bus control circuitry by setting pointers to the starting address in memory containing the message list and the number of data words to be transmitted or received. Specialized microcode within the SDP-175 handles each word as it is transferred and takes care of the pointer and counter registers.

The 1553 portion of the interface circuitry is also common and interchangeable between all MRTUs. The

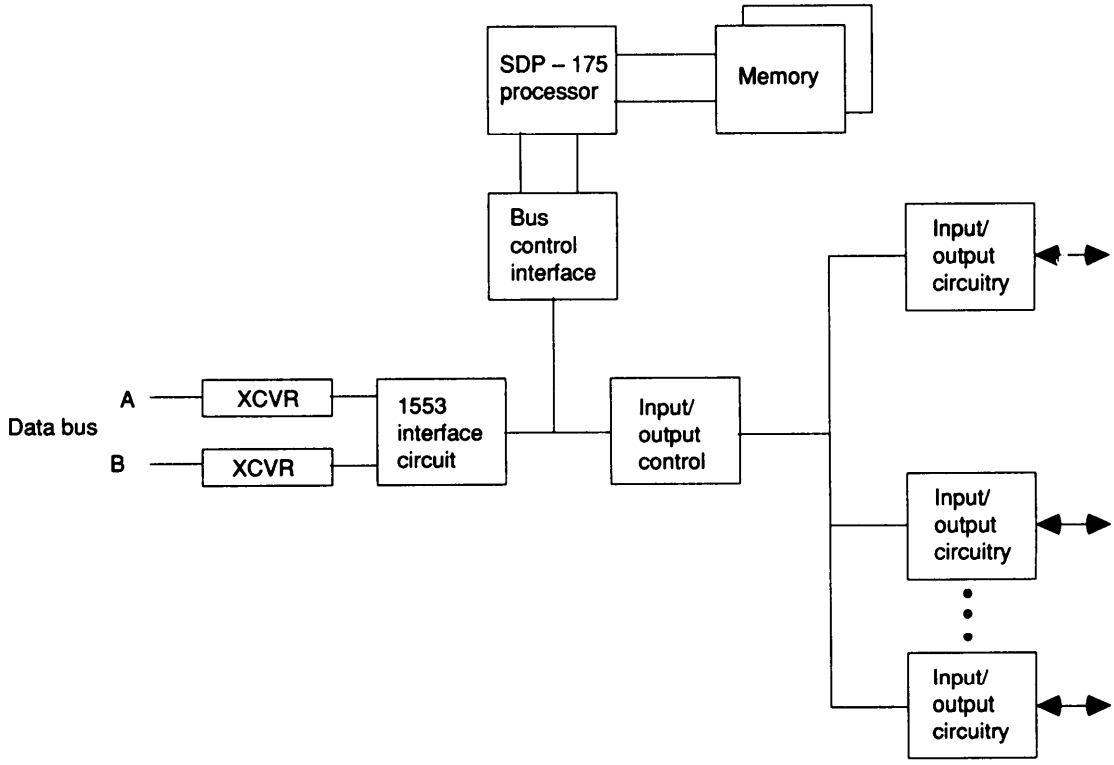


Figure 70-17. MRTU 1553 Interface

MRTU 1553 interface (Figure 70-17) is designed using LSI Manchester encoder/decoder circuitry (Harris 15530) and three custom hybrids. These hybrids are the bus selector, mode decoder, and the bus control.

The bus selector hybrid monitors each data bus for a valid command sync followed by a valid terminal address (five bits only, no parity).

> Note: On receipt of a valid command, control of the bus interface is switched to the bus from which the command was received.

The mode decoder hybrid controls and monitors the number of data words received or transmitted, decodes the mode codes, and provides the transmitter enable control and fail-safe monitor timing.

The bus control hybrid controls the 1553 protocol and manages the transfer of data between the 1553 interface and the MRTU subsystems.

The transmitter, receiver, and isolation transformer for each MRTU 1553 interface is located in the power supply of the unit.

In addition to the 1553 interface circuitry, each MRTU bus interface card also provides three terminal to/from subsystem serial digital interfaces, as defined in the 1553A standard.

70.4.4 System control.

70.4.4.1 Data transfer formats. The AH-64A uses command, data, and status words per the 1553A standard. Information flow on the data bus is composed of BC-to-RT and RT-to-BC messages. No RT-to-RT messages are used within the current system and no broadcast messages of any type are used.

70.4.4.2 Mode code use. McDonnell Douglas Helicopter, within the guidelines of the 1553A standard, has defined mode codes peculiar to the Apache application. The two mode commands provided for are:

a. BBC interrupt [00000], a form of dynamic bus control (the only 1553A-defined code).

b. Clear RT [00001], a form of reset RT.

Two other mode codes [00010 and 11111] are decoded by a majority of the terminals but are not used. All other mode codes (bit combinations) are ignored.

70.4.4.3 Status word use. The Apache 1553 status word is unique. The 1553A standard only requires that the message error bit (bit time 9) and the terminal flag bit (bit time 19) be used. All other status bits are optional and their definition is left to the terminal or system designer.

The Apache application uses the optional status word bits to report the state of the terminal input and output circuitry. Use of the status word bits is shown in Table 70-VII.

Table 70-VII AH-64A Status Bits

BIT time	Definition
10	Serial Digital Error - Used by terminals with subsystem serial interfaces circuitry to indicate a failure of one (or more) of those interfaces.
11	Reserved
12	Reserved
13	A/D Fail - Indicates a failure of an A/D converter to pass BIT
14	I Fail - Indicates a failure of descrete input sampling circuitry to pass BIT performed at power up.
15	DCO Fail - Indicates a failure of dc output circuitry to pass BIT.
16	DO Fail - Indicates a failure of a discrete output circuit to pass BIT.
17	Output Clear - Indicates that terminal outputs are being held in a clear state.
18	BBC - Used only in the BBC to indicate that the computer is up and running.

70.4.4.4 System startup. Two discrete handshake signals are passed between the FCC and BBC (Figure 70-18). The first signal (from the FCC to the BBC) indicates that the FCC is "healthy," having passed it's internal BIT, and is in control of the data bus. The second signal (from the BBC to the FCC) indicates that the BBC is in control of the data bus. The FCC executive assumes control of the bus on power-up initialization, assuming it's power-up BIT passes. When the FCC is in control, the BBC monitors both buses for activity. The BBC will automatically assume control of the bus if the handshake discrete from the FCC indicates a failure (no longer in control) or if there is an absence of bus transmissions on either bus for a specific period of time (programmable but typically in the area of 120 ms). If the FCC has relinquished control of the data bus to the BBC, it can regain control of the bus by indicating to the BBC via the handshake discrete that it is ready to resume control.

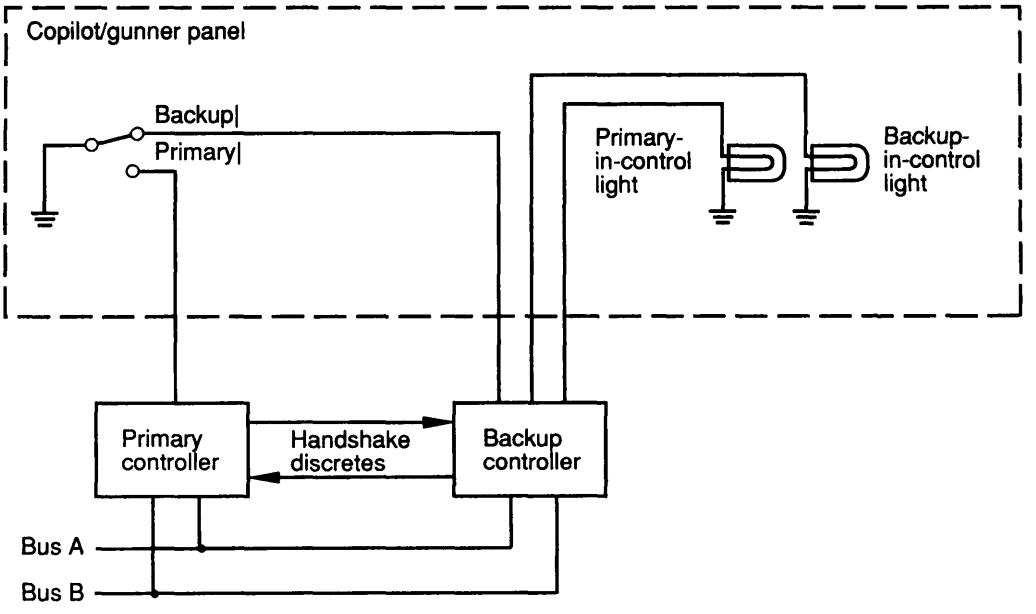


Figure 70-18. Primary and Backup Bus Controller Selection Logic

The Apache is also unique in that there is a switch in the copilot/gunner cockpit that allows for selecting the active controller. Originally placed there for system integration testing, this switch has remained in the production version. Advisory lights on the caution/warning panel indicate whether the FCC or BBC is in control and also cue the operator that the BBC has detected an inactive bus when the FCC was supposed to be in control.

70.4.4.5 Message processing. All messages on the Apache are periodic. Message update rates are based at 50 Hz (20 ms) with a two-frame sequence (odd and even) providing a lower 25-Hz rate for various subsystems. The messages within the odd or even frame are based on the operational mode of the selected weapon systems.

During the 20-ms frame, the controller collects data from all the terminals (transmit commands), processes it, and sends the output to the appropriate using terminal (receive commands). Data collection requires approximately 6 ms while data output requires approximately 7 ms. The remaining time is used for message processing. At present, bus loading is between 65% to 70%, depending on the frame and the weapons processing taking place.

In both controllers, a real-time clock interrupt initiates the beginning of a new frame. The executive will initiate collection of the data by setting the bus control pointers to the start of the transmit command message list. The start of the data output is also tied to a real-time interrupt. At the 13-ms timing point, the executive initializes the bus control pointers to the start of the receive command message list. When all commands have been processed, the computer enters a BIT cycle until the next new frame interrupt occurs.

70.4.4.6 Error detection and recovery. As per the 1553A standard, all terminals respond with their status word when processing a message regardless of an error condition. This status word provides the active controller with information regarding message processing (message error bit), terminal health or status (terminal flag bit), and status of the subsystem (optional status bits). Both controllers use these data to develop a degraded mode of operation for the system if necessary.

The data bus (primary or secondary) for which command words are to be transmitted on is selectable on a message-by-message basis. Messages for which a terminal responds with the message error bit set in the

status word will be tried on the alternate bus the next time around. Messages will continue to alternate between buses until valid communication are restored. The Apache uses no automatic retry within the same data frame and no reconfiguration of the message lists based on message errors or terminal errors (i.e., subsystem or terminal flag bits set within the status word). Terminals responding with terminal or subsystem bits set in the status word or a no response from the terminal are logged into the fault detection and location system as a subsystem fault.

70.5 F-16 C/D FALCON MULTIPLEX SYSTEM. The F-16 is an air combat fighter supplied to the Air Force by General Dynamics, Fort Worth Division. The F-16 development program coincided closely with the publication of the initial standard for multiplex systems, MIL-STD-l553 (USAF), and became the first aircraft to implement and flight test a multiplex data bus system compatible with MIL-STD-l553. There have been significant updates of the avionic and weapon capabilities of the aircraft during the Multinational Staged Improvement Program (MSIP) leading to the C/D (Block 40) version of the F-16.

70.5.1 Application area. The F-16 C/D (Block 40) is the latest version of the aircraft and includes significant updates of the avionic systems. The block diagram of the F-16 C/D (Block 40) is presented in Figure 70-19. The system comprises four multiplex data buses;

A-mux Avionics (core) multiplex bus

B-mux Avionics (defensive) multiplex bus

D-mux Display multiplex bus

W-mux Weapons multiplex bus

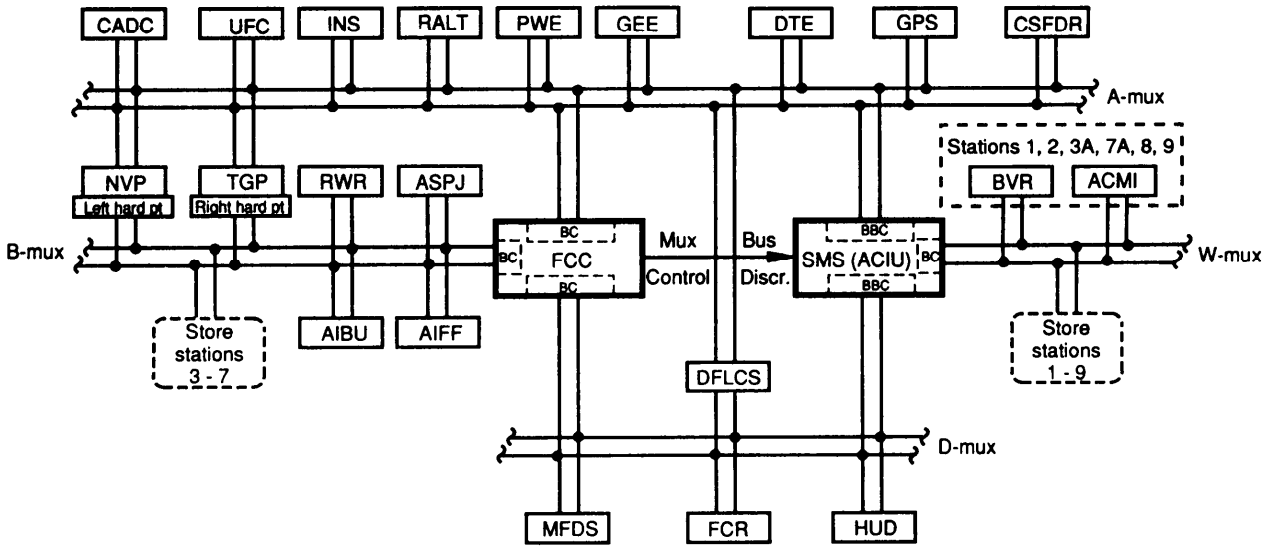
All buses are dual standby redundant (A- and B-buses). The system is partitioned with sensor functions processed within each sensor subsystem, and symbol generation and display processing are included in each display. Each display and sensor implement all functions and interfaces with other processors over the multiplex bus to receive data from processors in other subsystems or to transmit control information to other subsystems. Sensors, displays, and other subsystems are integrated into system modes by the two processors–fire control computer (FCC) and advanced central interface unit (ACIU)-commonly referred to as the stores management set (SMS).

The FCC is the primary integrating element because it provides primary bus control for the A-mux and D-mux and is the only bus control for the B-mux. The SMS (ACIU) provides backup bus control for the A-mux and D-mux and is the only bus control for the W-mux.

70.5.2 Bus protocols. The bus controllers (BC) for the A-mux, B-mux, and D-mux are capable of operating dual protocols: MlL-STD-1553 and MlL-STD-1553B (referred to as 1553 and 1553B in this section). The 1553 protocol is the initial implementation of the multiplex bus in the first F-16 aircraft. The 1553B protocol reflects the implementation in the F-16 C/D employing the latest version (B) of 1553. The BC for the W-mux is capable of operating with three protocols: 1553, 1553B, and RIU (remote interface unit). The RIU is the remote terminal (RT) for the W-mux. The protocol of the weapons (RIU) multiplex bus is significantly different from 1553 and 1553B. The electrical characteristics are compatible so that the same cable network will accommodate the protocols.

All four buses may have subsystems that communicate over the bus in 1553 (F-16) protocol while other subsystems use the 1553B (F-16) protocol. In addition, the W-mux uses a non-1553 bus protocol for communicating with the weapons RIU at the store stations.

The 1553 and 1553B (F-16) implementations generally conform to the requirements of the standard in the following areas:



ACMI – Aircraft Maneuvering Instrumentation Pod
AIBU – Advanced Interference Blanker Unit
AIFF – Advanced Identification Friend of Foe
ASPJ – Airborne Self Protection Jammer
BVR – Beyond Visual Range (AMRAAM) Missile
CADC – Central Air Data Computer
CSFDR – Crash Survivable Flight Data Recorder
DFLCS – Digital Flight Control System
DTE – Data Transfer Equipment
FCC – Fire Control Computer
FCR – Fire Control Radar
GEE – F110 Engine Monitoring System Computer
GPS – Global Positioning System
HUD – Heads Up Display
INS – Standard Inertial Navigation Set
MFDS – Multifunction Display Set
NVP – Navigation Pod
PWE – F100 Engine Diagnostic Unit
RALT – Radar Altimeter
RWR – Radar Warning Receiver
SMS – Stores Management Set
TGP – Targeting Pod
UFC – Up Front Controls

Figure 70-19. F-16 C/D (Block 40) Avionic Systems Block Diagram

a. Centralized control (BC).

b. Basic command and response operation.

c. Word and message structure (bits per word, words per message).

d. Communication modes (BC to RT, RT to BC, and RT to RT).

e. Signal and bus network characteristics.

Paragraphs 70.5.2.1 through 70.5.2.4 describe the differences between the 1553 and 1553B protocols, as installed on the F-16, and the approach to accommodating the various subsystem designs.

70.52.1 Implementation of 1553. The original F-16 data bus system, designated 1553 (F-16), was designed to be compatible with the requirements of 1553 (USAF). Because the standard did not contain sufficient information to specify procurable hardware, General Dynamics chose to include all the multiplex data bus requirements in the F-16 interface control document (ICD).

In addition to the specification sheets normally included in the ICD, the F-16 document (16PP188) includes the essential requirements of 1553 (USAF). Additional details are included that allow the ICD to be used for procurement of compatible subsystems. Supplementary requirements contained in 16PP188 and the succeeding ICDs for avionics updates include:

a. Status word failure and status bit definition.

b. Bus redundancy.

c. Terminal address and subaddress assignments.

d. Timing constraints.

As implemented, the 1553 (F-16) system contains few actual deviations from the standard. Most would be more accurately classified as clarifications or additions to the original standard. For example, the input/output signal interface was changed from the bus side to the user subsystem side of the coupler network. This eliminates any subsystem supplier responsibility for the aircraft bus network wiring that is supplied by General Dynamics.

Message formats. The F-161553 message formats follow the requirements of the standard as follows (refer to Figure 70-20):

a. Controller-to-subsystem transfer.

b. Subsystem-to-controller transfer.

c. Subsystem-to-subsystem transfer.

d. Broadcast function command.

Included in the ICD is the use of all 1's in the terminal address or subaddress fields. An all-1s terminal address is defined as a broadcast command and allows terminals (subsystems) that are implemented with broadcast to receive the broadcast message without responding with a status word. Instead, on receipt of a broadcast command, a broadcast function bit is set in the status register for transmission after the next normal command. Broadcast is specified in the ICD and implemented in hardware; however, it is not used in the system.

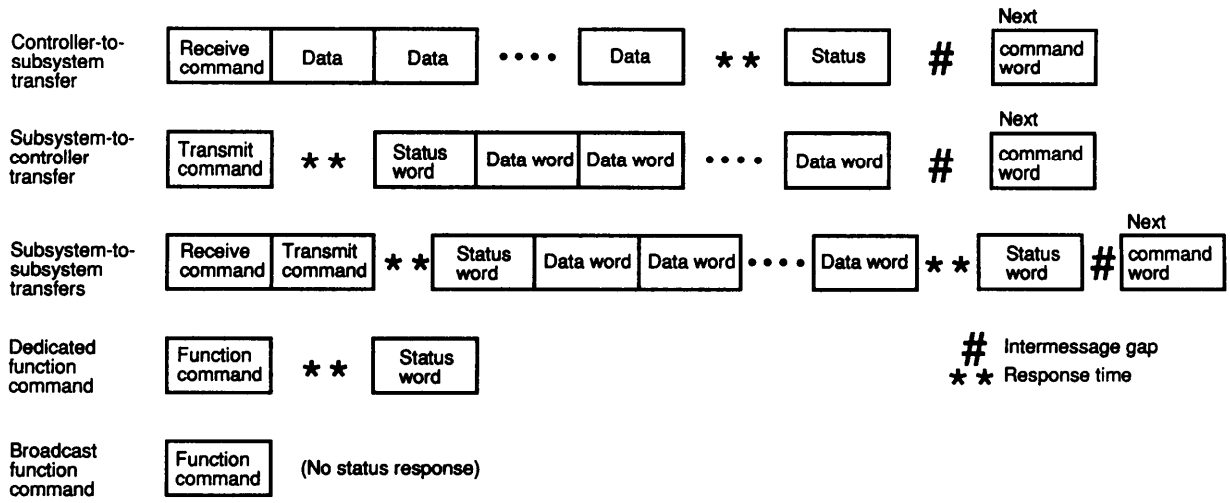


Figure 70-20. F-16 1553 Message Formats

Function modes. All 1's in the subaddress/mode field designates a dedicated function command that is coded in the word count field. The only function command code allowed for 1553 operation is the following:

Word Count Field	Function Command
00001	Reset timer

If a subsystem receives a function command with the word count field all O'S, or with a bit pattern in the word count field that the subsystem is not mechanized to execute, the subsystem will reset or initialize its receiver logic and respond with the status word.

Status word. The status word provides a response to the BC from the subsystem that receives a valid command word. The status word structure is shown in Figure 70-21. The failure/status bits will be set to logic zero following transmission. The failure/status bits (9-19) of the status word are defined as follows:

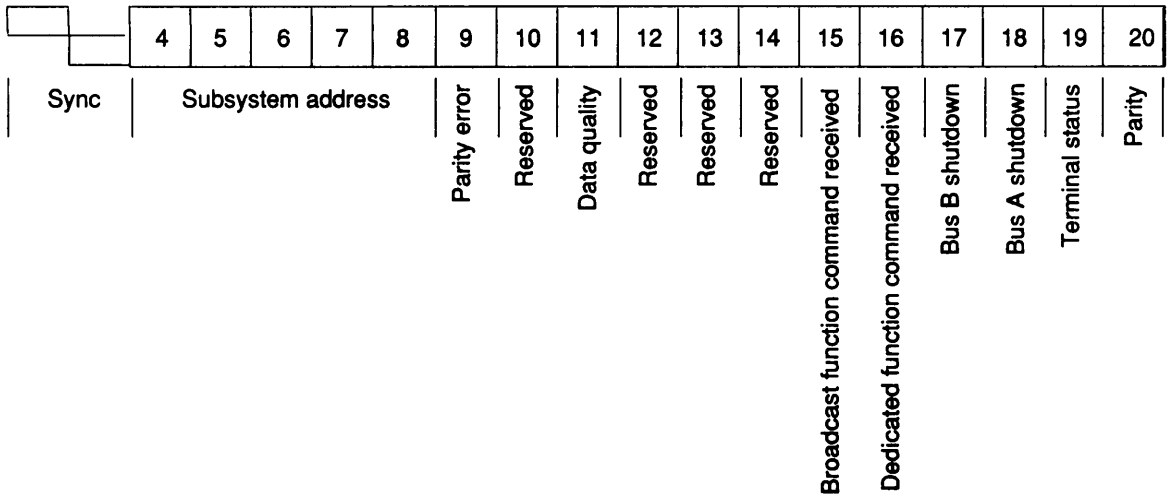


Figure 70-21. F-16 1553 Status Word

Bit 9 **Parity error –** Indicates a parity error in one or more data words associated with the preceding receive command word.

Bit 10 **Reserved.**

Bit 11 **Data quality -** Indicates the occurrence of a data word validation error or errors in one or more of the data words associated with the preceding receive command word.

Bit 12-14 **Reserved.**

Bit 15 **Broadcast function command received -** Indicates receipt of the broadcast function command.

Bit 16 **Dedicated function command received -** Indicates receipt of a dedicated function command.

Bit 17 **B-bus shutdown -** Indicates that the transmission on the B-bus was terminated by (1) receipt of a valid command on the A-bus during a transmission on the B-bus or (2) detection of an abnormal transmission.

Bit 18 **A-bus shutdown -** Same as for B-bus.

Bit 19 **Terminal status -** Indicates the presence of a fault condition that destroys the credibility of certain bits (mode, self-test, or data validity). In the event of a failure that results in the inability of the subsystem software to set the mode, self-test, or data valid bits, bit 19 will be set by the terminal hardware.

Subsystem/bus interface. The subsystems are connected to the bus with couplers (isolation transformers and resistors) and cable stubs up to 20 ft long. The turns ratio (N) of the coupler transformer is specified to be 1:1 for 1553 (F-16) subsystems. Because the 1553B (F-16) coupler transformers have a turns ratio of 1:1.41, the subsystem/bus interface signal voltages and impedances are specified differently for the two cases.

The following is a summary of the input/output conditions specified for the 1553 subsystems.

Output

Output voltage	±12V, ±10% peak
Load impedance	143 ohms
Rise and fall times	120 ns, ±80 ns

Input

Waveform	Square wave or sine wave
Signal level	4.0V to 6.0V peak, response 0.0V to 0.45V peak, no response
Input impedance 100 KHz to 1.0 MHz	2000 ohms (minimum)

70.5.2.2 Implementation of 1553B. As the capabilities of F-16 avionics has increased in the Multinational Staged Improvement Program (MSIP) the complexity of the avionic systems has increased as reflected in the block diagram of Figure 70-19. Also, military standards have been updated and new standards developed for avionic hardware and software. The F-16 C/D advanced avionic designs feature use of MIL-STD-1553B, MIL-STD-1750A Computer Instruction Set Architecture, JOVIAL J73 High Order Language (MIL-STD-1589B), and MlL-STD-1760 Aircraft/Store Electrical Interconnection System.

The following paragraphs describe the F-16 implementation of 1553B and the achievement of compatibility with the earlier 1553 version.

Message formats. The F-16 1553B protocol message formats conform with the requirements specified in 1553B, except that the broadcast function command is not implemented. The following is a listing of the message formats. (Refer to Figure 70-22.)

a. Controller-to-subsystem transfer.

b. Subsystem-to-controller transfer.

c. Subsystem-to-subsystem transfer.

d. Mode command without data word.

e. Mode command with data word (transmit).

f. Mode command with data word (receive).

All 1's or all 0's in the command word subaddress/mode field define the command as a mode command. The bit pattern contained in the word count/mode field determines the specific mode command to be executed when the subaddress/mode field contains all 1's or all 0's. All 1's in the terminal address field is reserved for broadcast and is not implemented in the 1553B (F-16) system.

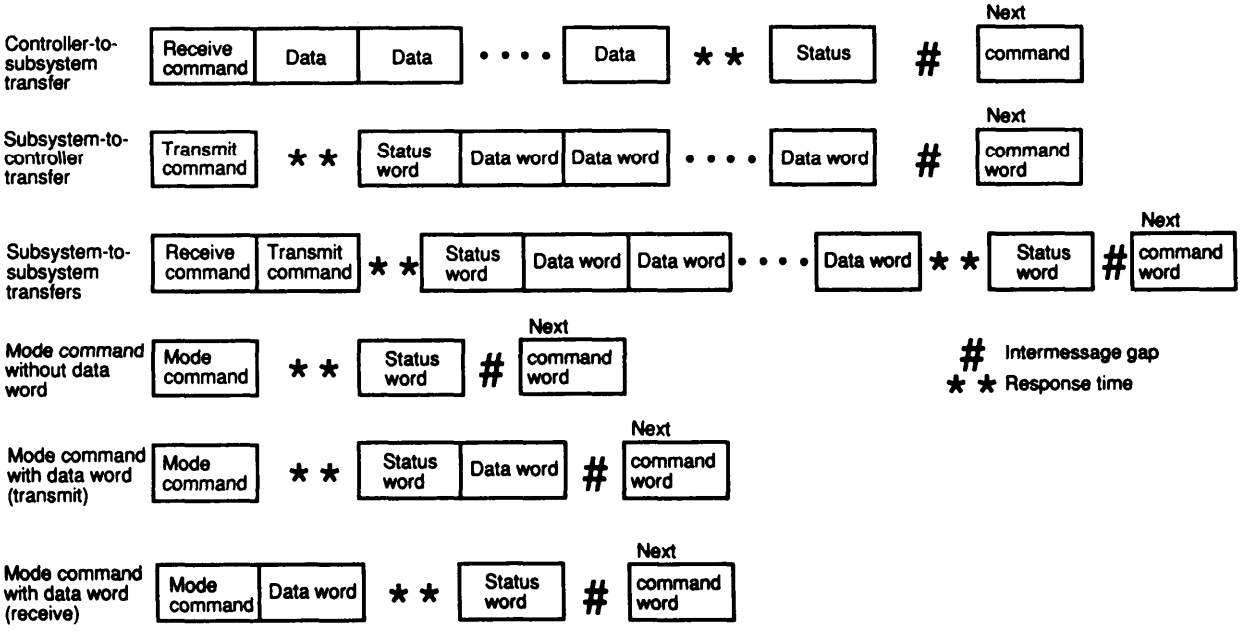


Figure 70-22. F-16 15536 Message Formats

Function modes. All 1's or all 0's in the subaddress/mode field of the command word designates a dedicated mode command that is coded in the word count/mode field. Table 70-VIII is a list of the mode commands and the mode code assignments allowed to be used in the F-16 1553B bus system.

Table 70-VIII. F-16 Mode Commands and Assignments

T/R bit	Mode code	Function	Data word
1	00001	Synchronize	No
1	00010	Transmit Status Word	No
1	00011	Initiate BIT	No
1	00100	Transmitter Shutdown	No
1	00101	Override Transmitter Shutdown	No
1	01000	Reset Terminal Electronics	No
1	10000	Transmit Vector Word	Yes
0	10001	Synchronize	Yes
1	10010	Transmit Last Command	Yes
1	10011	Transmit BIT Word	Yes

Unless specifically exempted by General Dynamics, each subsystem is required to mechanize the mode commands listed in Table 70-VIII. Other mode commands specified in 1553B are not allowed to be used because Air Force Notice 1 to the standard prohibits their use in Air Force avionic applications.

Status word. The status word provides a response to the BC from the subsystem that receives a valid command word. The status word structure is shown in Figure 70-23. Subsystems reset to 0 all status word failure/status bits following receipt of a valid command word, with the exception of the transmit status word and transmit last command mode commands. The failure/status bits (9-19) are defined as follows:

Bit 9 **Message error –** Indicates that one or more of the data words associated with the preceding receive command word has failed to pass the validity tests or transmission continuity, illegal command, and invalid data reception checks.

Bit 10 **Reserved.**

Bit 11 **Service request -** Indicates a service request by the subsystem.

Bit 12-15 **Reserved.**

Bit 16 **Busy –** Not to be used unless specifically agreed to by General Dynamics.

Bit 17 **Subsystem fail -** Indicates the presence of fault conditions in the subsystem or subsystem-to-terminal interface that destroys the credibility of subsystem mode or data valid bits seen in data words at the multiplex interface.

Bit 18 **Reserved.**

Bit 19 **Terminal error -** Indicates fault conditions that destroy the credibility of valid mode and data bits seen at the multiplex bus interface within the subsystem multiplex terminal electronics.

Electrical interface. As discussed for the 1553 protocol in 70.5.2.1, the subsystems are connected to the bus with couplers. The isolation transformer for 1553B subsystems has a turns ratio of 1:1.41, with the larger

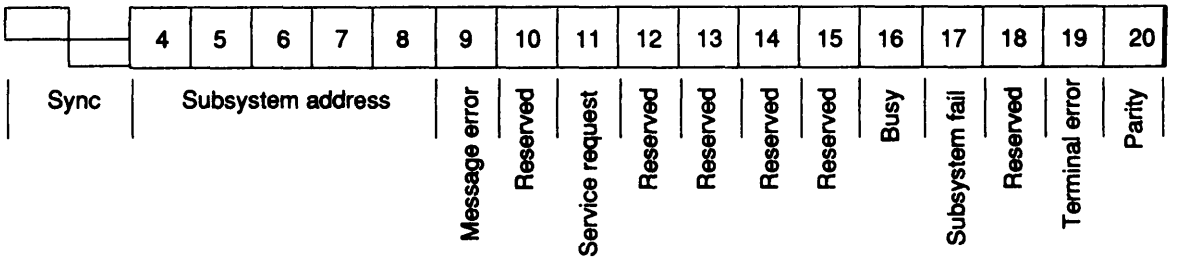


Figure 70-23. F-16 Status Word Format. Output

number of turns at the bus side. The subsystems interface input/output conditions are summarized as follows:

Output

Output voltage	18V to 25V p-p
Load impedance	70 ohms
Rise and fall times	100 to 300 ns

Input

Waveform	Square wave or sine wave
Signal level	0.86V to 14.0V p-p, response required 0.0V to 0.20V p-p, no response
Input impedance	1000 ohms (minimum) 75 KHz to 1.0 MHz

70.5.2.3 Dual-protocol subsystems. Certain subsystems are required to be compatible with both the 1553 (F-16) and the 1553B (F-16) protocols. These subsystems are divided into two categories: full F-16 1553/1553B and restricted F-16 1553/1553B subsystems. The following is a summary of the characteristics of the two categories.

a. Full F-16 1553/1553B subsystem-

1. Meets 1553 protocol requirements when 1553 mode is selected.

2. Meets 1553B protocol requirements when 1553B mode is selected.

3. Meets the electrical requirements of 1553B when either mode is selected.

b. Restricted F-16 1553/1553B subsystem-

1. Meets the protocol requirements of F-16 1553B when 1553 mode is selected, with the following exceptions:

   – Function and mode commands with data words not allowed.
   – Status word failure and status bits 16 and 17 are logically "ORed" with bit 19.

2. Meets the electrical requirements of 1553B.

The capability to select protocol is provided in the subsystem terminal hardware and software. The selection is made using a jumper on the external connector of the LRU. The 1553 mode is selected when the jumper is installed.

70.5.2.4 Bus control. In the F-16 avionics architecture (shown in Figure 70-19), the fire control computer (FCC) is the primary system integrator. The stores management set (SMS) with the advanced central interface unit (ACIU) serves as the backup control for the A-mux and D-mux in case of an FCC failure. The SMS/ACIU is dual redundant internally and provides control for the W-mux in addition to the backup function. The FCC also provides bus control for the B-mux. All buses are required to operate in both protocols-1553 (F-16) and 1553B (F-16)—as described in detail in 70.5.2.1 and 70.5.2.2. The BC for the W-mux is also required to support the weapons RIU bus protocol.

Control concept. There are two key considerations for the bus control algorithm design: (1) the predominant transmission mode, periodic or on demand, and (2) the error-handling procedures. In the F-16, a predominantly periodic transmission operation is implemented. This has enabled a computer program structure that takes advantage of scheduled inputs and outputs to minimize data latency. Also, functional partitioning is facilitated to ease the interface requirements for the subsystem suppliers.

The development of efficient error-handling procedures is critical to overall system operation. The method of error handling implemented is a simple approach: (1) a detected error causes a software interrupt, and (2) software marks a log of errors and either retries the command on the alternate bus or skips the command. The command is skipped if only the retry on the alternate bus fails. This method can be summarized as "fail once, retry on alternate, fail twice, go to next command."

Controller architecture. The F-16 controller is required to implement most of the 1553B protocol and also accommodate those subsystems designed to use the 1553 (F-16) protocol. The controller must support the transfer of time-consistent blocks of input and output data. There is also a requirement that normal bus operations need a minimum of intervention from the host computer CPU. Therefore, a certain degree of intelligence is incorporated into the controller to ensure that the bus control task does not adversely affect the throughput of the host computer. Provisions are made to interrupt the CPU when required, but these are very limited and selectable so that the CPU is not burdened with needless overhead.

The architecture of the controller is required to be compatible with MIL-STD-1750A and MIL-STD-1589B.

The controller executes a control program stored in the memory of the host computer. The I/O channel executes independently from the host when provided the start address of the program. All input and output data needed by the channel are obtained from the host computer memory via direct memory access. The instructions of the I/O channel program consist of four words each.

Channel instruction word 0 includes an operation code (OPCODE) and other control information. Two bits specify the protocol (1553 or 1553B) of the transmitting and receiving subsystems. The other bits specify the CPU interrupt and retry instructions for error conditions. Word 1 is the first 1553 command word to be transmitted over the bus for the transaction. Word 2 contains the second command word, a word required only for subsystem-to-subsystem operation. The last word (word 3) of the command contains the host memory address for data retrieval or storage, or the new channel program address in the case of the branch operation code.

Fault isolation and redundancy management. All bus control is based on the ability to communicate. Communication status assessment is established through periodic polling of each subsystem. Polling occurs at the basic frame rate of 1.5625 Hz. Messages are transmitted at this rate or a binary multiple of the frame rate up to 50 Hz. Based on the integrity of the response from the subsystems, data communications are either established or deleted. If the subsystem responds to the BC command with an error-free valid transmission, then data communications are established. If the subsystem fails to respond with a valid transmission for two consecutive commands, the data transfer commands of that subsystem are deleted from the current command table of the BC.

This approach also results in a simple method for selecting the channel (A-bus or B-bus). The controller uses the channel that worked the last time communications were established with that subsystem. For example, a successful transfer on A-bus would result in the next transfer of the same block being attempted on A-bus. If the first attempt on A-bus failed, then the retry of that transmission would be attempted on B-bus. Communications would continue on the channel that is functional. Retry is limited to once per scan of the command table and is always initiated on the alternate channel.

Primary and backup control. The F-16 FCC normally functions as the system integrator and provides the primary control for the A-mux, D-mux, and B-mux. If the FCC power is off or a failure is detected by the internal BITE, the SMS will assume control of the A-mux and D-mux. Bus control is passed to the backup controllers in the SMS by a discrete signal connected from the FCC to the SMS. The discrete is monitored by circuitry in the SMS to determine when control is to be accepted or relinquished. Backup control is limited to selected subsystems on the A-mux and D-mux buses.

A form of backup operation is provided in the SMS for an internal failure because the ACIU is dual redundant. Therefore, operation of the SMS/ACIU will be maintained for normal operation on all three buses and backup bus control of the A-mux and D-mux in the event of a single SMS failure.

The B-mux has no provision for backup control in the event the FCC power is off or there is a failure condition.

Detailed discussions of the A-mux, B-mux, D-mux, and W-mux operation and data flow are provided in 70.5.3.

70.5.3 Bus descriptions (architecture).

70.5.3.1 A-mux.

Bus architecture. The A-mux bus consists of two bus controllers, primary and backup, and 13 remote terminals identified as follows:

a. **Bus controllers-**

1. Primary-fire control computer.
2. Backup-stores management set.

b. **Remote terminals-**

1. Central air data computer (CADC).
2. Crash-survivable flight data recorder (CSFDR).
3. Digital flight control system (DFLCS).
4. Data transfer equipment (DTE).
5. F110 engine monitoring system computer (GEE).
6. Global positioning system (GPS).
7. Inertial navigation system (INS).
8. Navigation pod (NVP).
9. F100 engine diagnostic unit (PWE).

10. Radar altimeter (RALT).

11. Stores management set (SMS).

12. Targeting pod (TGP).

13. Up-front controls (UFC).

A block diagram of the A-mux bus is shown in Figure 70-24. Note that the SMS normally acts as an RT, but it assumes bus control on failure of the FCC, which is the primary controller. There are several units on the bus that also communicate with one of the other buses through multiple RTs. The NVP and TGP also interface with the B-mux bus at the left and right hard points. The FCC is also the primary bus control for the D-mux and the only bus control for the B-mux buses. The SMS advanced central interface unit (ACIU) provides the backup bus control for both the A-mux and D-mux as well as the only bus control for the W-mux. The SMS and the DFLCS also communicate with the D-mux bus through separate internal RTs.

All A-mux terminals use 1553B protocol except for the CADC, which uses 1553.

Signal flow. A functional block diagram depicting A-mux system signal flow in primary and backup modes is shown in figures 70-25 and 70-26.

The A-mux system signal flow in the primary mode of operation consists of 83 possible messages ranging in length from one word to the full 32 words. Data set transfers from the DTE can take up to twenty 32-word message transmissions. Extensive use is made of RT-to-RT transfers.

In the backup mode, there are 29 possible messages ranging in length from one to 32 words. Because the DTE is not included in the backup signal flow, no multiple transmissions are required for any message.

System control. The A-mux system uses a relatively simple control philosophy. The FCC, when operating, acts as the BC. If the FCC is not operating, the SMS assumes bus control. The simplicity of the F-16 system is again apparent in the mechanization of the bus control transition technique. If the FCC power is off or it becomes inoperative, bus control is passed to the SMS by a single discrete between the two units. During operation, the SMS periodically samples the discrete for a high-voltage or high-impedance condition. If two consecutive samples are in either the “pass control” or “no go” state, the SMS assumes bus control responsibilities. The SMS then continues periodic sampling of the discrete and relinquishes control to the FCC immediately on detection of a low-voltage “go” condition on the discrete.

Bus controller. The FCC is the primary integrating element because it provides primary bus control for the A-mux, B-mux, and D-mux buses. The bus control is dual protocol, meaning that it can communicate with both 1553 and 1553B multiplex bus terminals on either of two multiplex buses.

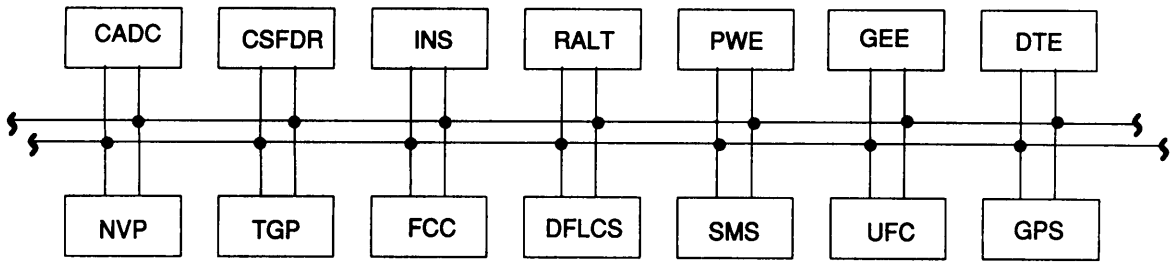


Figure 70-24. A-mux System Architecture

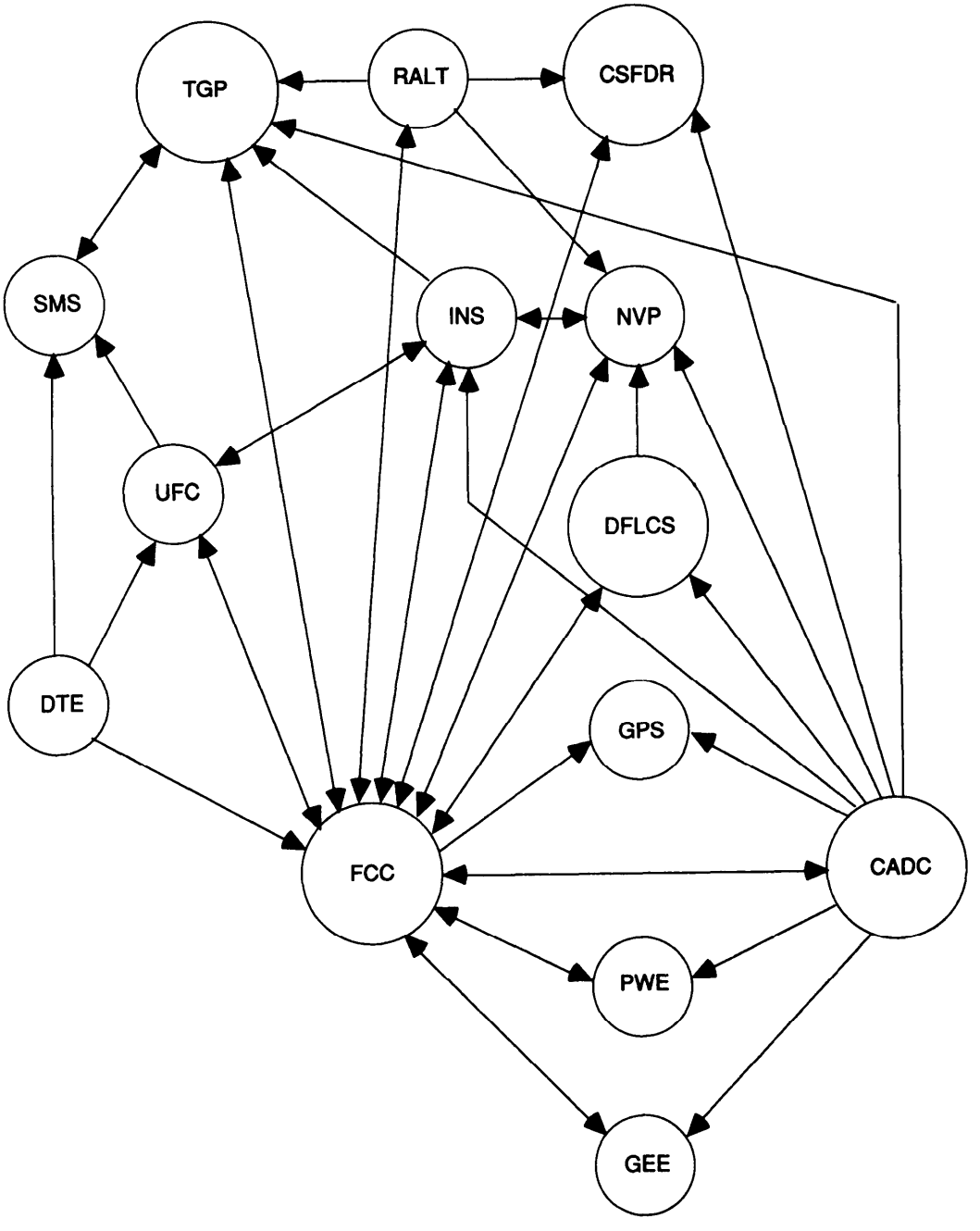


Figure 70-25. A-mux System Signal Flow (Primary Mode)

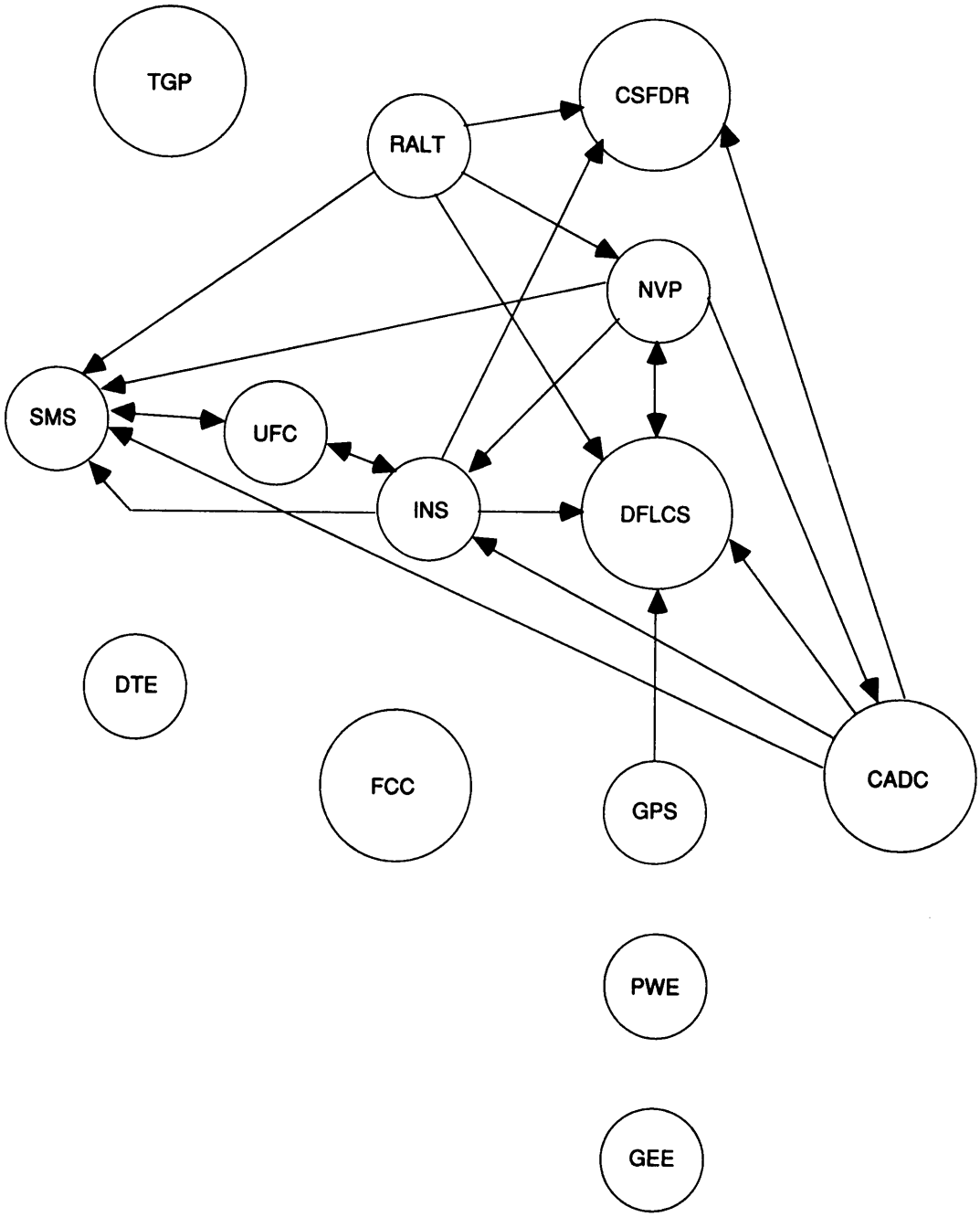


Figure 70-26. A-mux System Signal Flow (Backup Mode)

The SMS ACIU provides backup bus control on the A-mux bus. In addition to their bus control functions, both the FCC and ACIU are fully functional system processors that (1) coordinate sensors, displays, modes, etc., and (2) provide system-level processing, such as air-to-surface bombing solutions that require inputs from several sources. The system processors are not deeply involved in supporting sensor functions because that would result in complex signal interfaces and decreased flexibility. Likewise, the system processors supply the displays with the data they require but generally are not involved in the actual positioning and formatting of the displays.

Remote terminals. The F-16A-mux data bus system interfaces with and provides complete communication with 14 major subsystems, as listed previously under "Bus architecture" in 70.5.3.1. All bus interfaces are integral to the subsystems they serve. There are no standalone RTs.

The only mode codes used by the A-mux system are reset terminal electronics and synchronize. The synchronize code is used by the INS. The nonimplemented mode code 00000 is sent to the INS and CADC for polling purposes. All other RTs recognize the reset terminal electronics mode code.

70.5.3.2 B-mux.

Bus architecture. The B-mux bus consists of a BC and six RTs as follows:

a. **Bus controller–**

1. Fire control computer (FCC).

b. **Remote terminals-**

1. Advanced interference blanker unit (AIBU).

2. Advanced IFF (AIFF).

3. **Airborne self-protection jammer (ASPJ).**

1. Radar warning receiver (RWR).

2. Navigation pod (NVP).

3. Targeting pod (TGP).

A block diagram of the B-mux system is shown in Figure 70-27. The FCC provides the only bus control. There is no provision for backup bus control. All B-mux terminals use 1553B protocol.

Signal flow. The B-mux data bus signal flow is depicted in Figure 70-28. There are 36 possible messages ranging in length from 1 to 27 data words. No messages require multiple transmissions.

System control. System control is provided by the FCC and is dual protocol, operating with both 1553 and 1553B RTs.

Bus Controller. B-mux bus control is provided by a third bus controller in the FCC. There is no backup bus controller.

Remote terminals. The F-16B-mux data bus system interfaces with and provides communication with six RTs, including the right and left hardpoints, as listed previously under "Bus architecture" in 70.5.3.2. All bus interfaces are integral to the subsystems they serve. There are no standalone RTs.

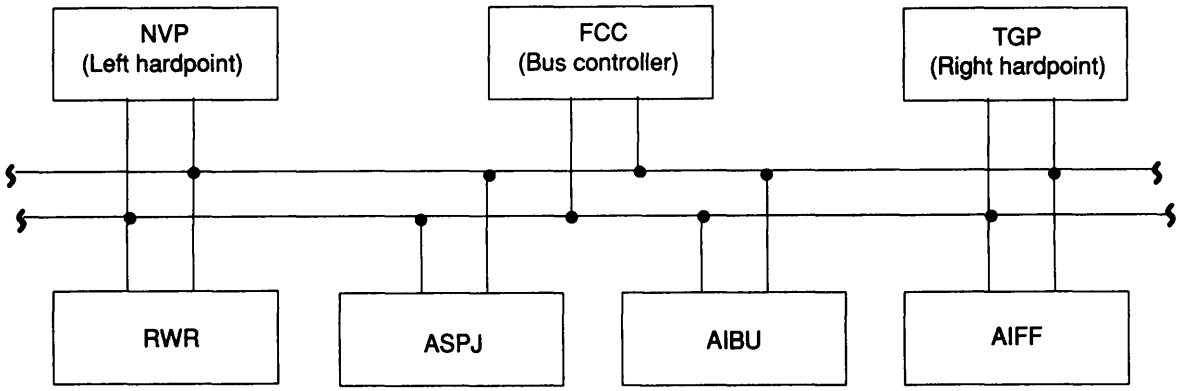


Figure 70-27. B-Mux System Block Diagram

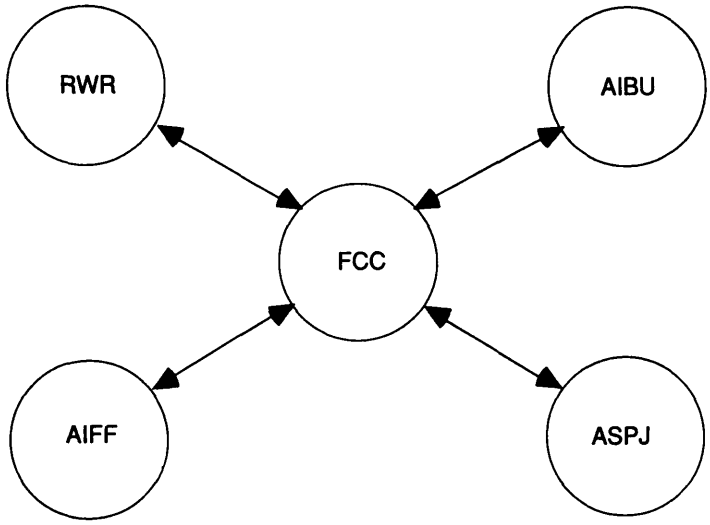


Figure 70-28. B-Mux System Signal Flow

All RTs recognize the reset terminal electronics mode code. The RWR also uses the synchronize mode code.

70.5.3.3 D-mux.

Bus architecture. The D-mux bus consists of two BCs, primary and backup, and five RTs identified as follows:

a. **Bus controllers-**

1. Fire control computer (FCC).

2. Stores management set (SMS).

b. **Remote terminals-**

1. Digital flight control system (DFLCS).

2. Multifunction display set (MFDS).

3. Fire control radar (FCR).

4. Head-up display (HUD).

5. Stores management set (SMS).

A block diagram of the D-mux bus is shown in Figure 70-29. Note that the SMS normally acts as an RT, but assumes bus control on failure of the FCC, which is the primary controller. The DFLCS also communicates with the A-mux bus through a second RT.

The D-mux system uses the same control philosophy as the A-mux. The FCC, when operating, provides bus control. If the FCC is not operating, the SMS assumes bus control. The same bus control discrete is used in the same manner as described for the A-mux.

All D-mux terminals use 1553B protocol except for the FCR, which uses 1553.

Signal flow. Functional block diagrams depicting D-mux system signal flow in both the primary and backup modes are shown in figures 70-30 and 70-31.

The D-mux system signal flow in the primary mode of operation consists of 83 possible messages ranging in length from 1 to 32 words in length. Multiple transmissions are not required. In the backup mode, there are 33 possible messages ranging in length from one to 31 words.

System control. D-mux system control is identical to that of the A-mux system.

Bus controller. Primary and backup bus control for the D-mux system is provided by the same processors that control the A-mux (FCC and SMS). Bus control is handled in an identical manner through second, independent BCs in each of the two processors.

Remote terminals. The F-16 D-mux system interfaces with five subsystems as listed previously under "Bus architecture" in 70.5.3.3. All RTs are integral to the subsystem that they serve. There are no standalone RTs.

The reset terminal electronics mode code is accepted by the DFLCS, HUD, MFDS, and SMS. The FCR and SMS use the synchronize command and the invalid mode code 00000 is sent to the FCR for polling purposes.

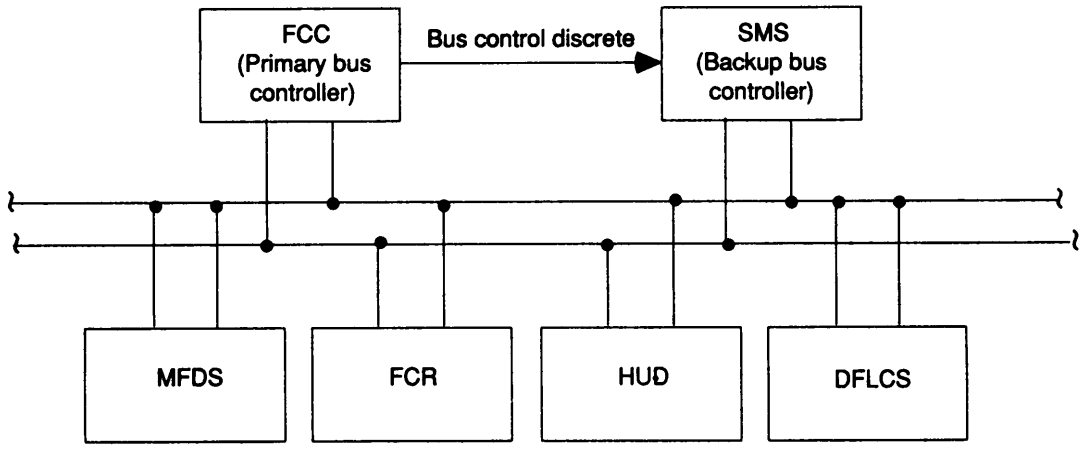


Figure 70-29. D-Mux System Block Diagram

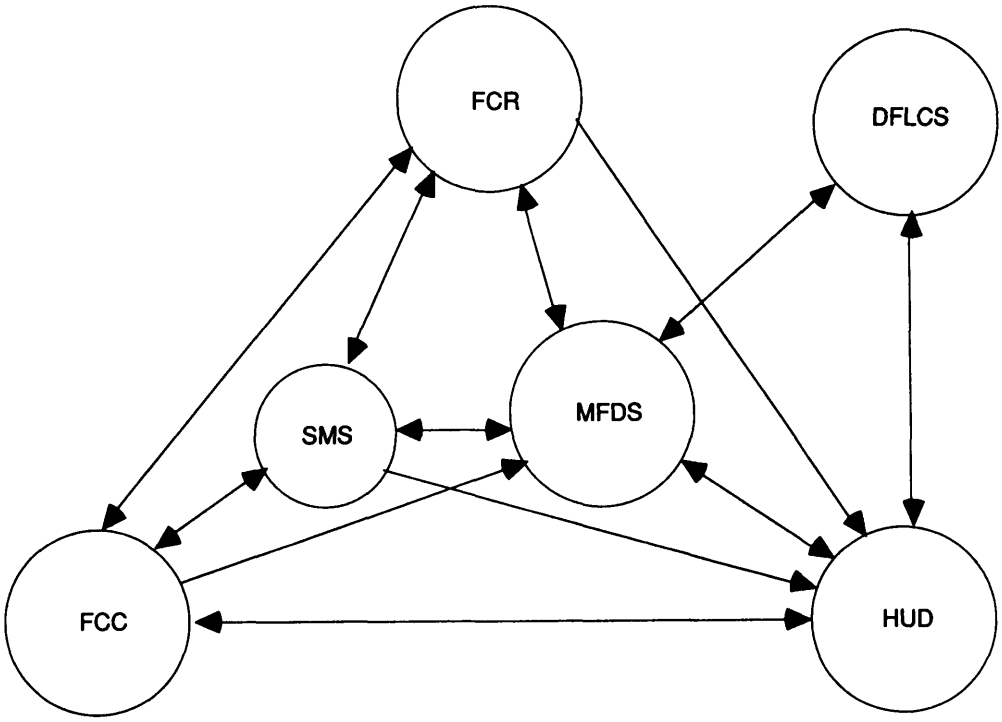


Figure 70-30. D-Mux System Signal Flow (Primary Mode)

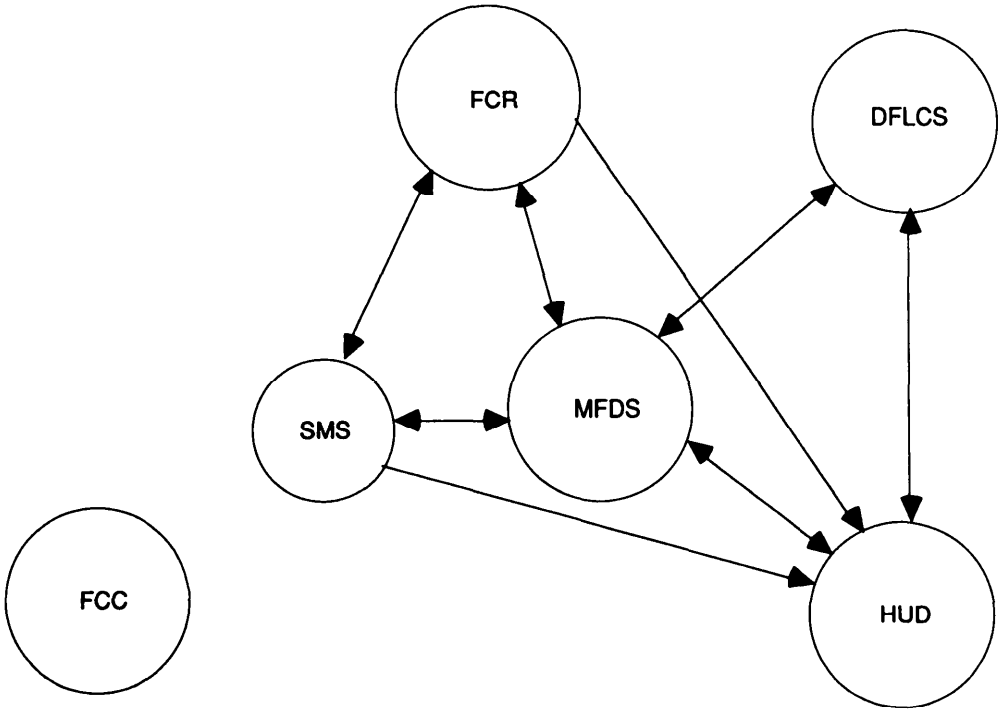


Figure 70-31. D-Mux System Signal Flow (Backup Mode)

70.5.3.4 W-mux. The weapons multiplex (W-mux) bus serves the stores management set (SMS) that performs stores control and monitor functions.

Bus architecture. The SMS has three multiplex bus ports. One interfaces with the W-mux bus and the other two with the A-mux and D-mux buses as shown in Figure 70-32. The W-mux is available at all nine of the weapon store stations and provides the interface requirements for advanced weapons and sensors in compliance with MIL-STD-1760.

The only 1553 stores presently planned for the W-mux bus are the beyond visual range (AMRAAM) missile and the aircraft maneuvering Instrumentation pod (ACMI), which will be loaded on stations 1,2, 3a, 7a, 8, or 9. ACMI uses 1553 protocol and AMRAAM uses 1553B.

The F-16 RIU mux bus extends to store stations 1 through 9.

Signal flow. A functional block diagram depicting W-mux system signal flow is shown in Figure 70-33.

The D-mux system signal flow consists of only five possible messages ranging in length from 1 to 29 words. No messages require multiple transmissions.

System control. W-mux system control is provided by a third BC in the SMS ACIU.

Bus controller. The advanced central interface unit (ACIU) provides the sole bus control on the W-mux and is triple protocol (1553/1553B/RIU mux) capable. There is no provision for backup bus control.

Remote terminal. The F-16 W-mux system interfaces with only two subsystems using 1553-type protocol, as listed previously under "Bus architecture" in 70.5.3.4. All RTs are integral to the individual store (AMRAAM or ACMI).

F-16 SMS remote interface units (RIUs) are supported at each store station using standard F-16 RIU protocol.

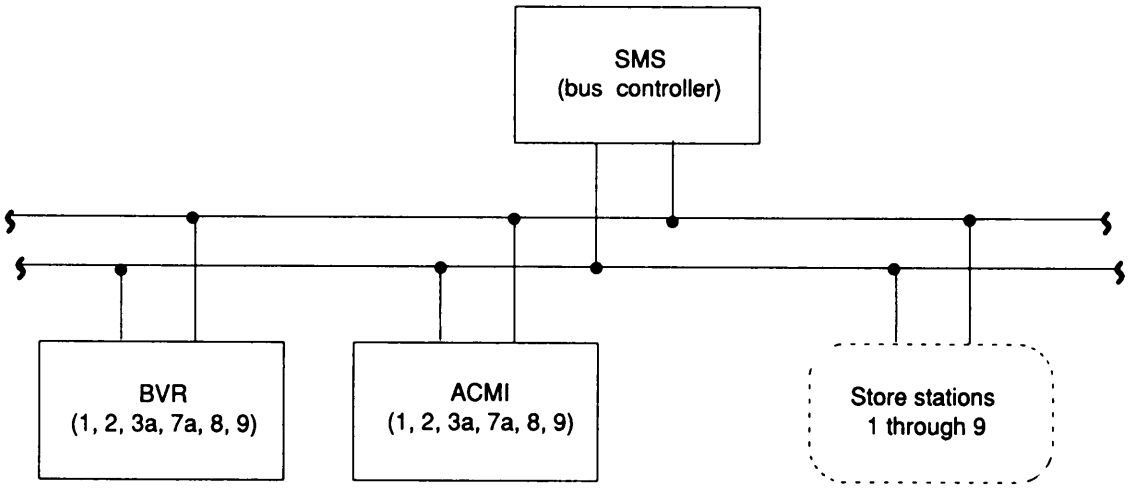


Figure 70-32. W-Mux System Block Diagram

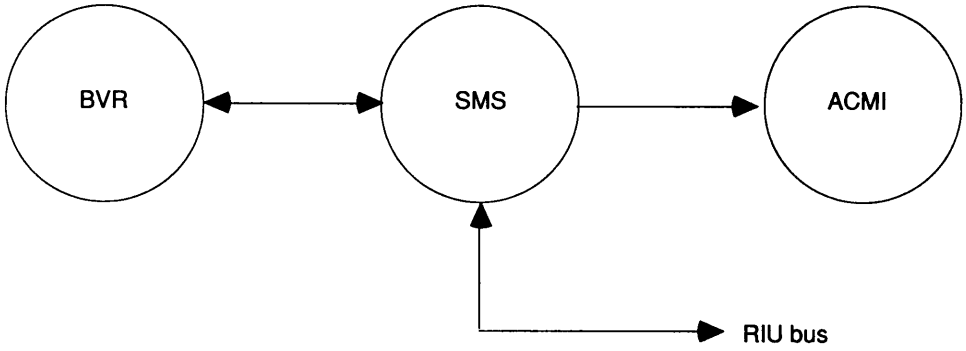


Figure 70-33. W-Mux System Signal Flow

70.6 **C-17A TRANSPORT MULTIPLEX SYSTEM**

The C-17 is a Multipurpose Airlifter supplied to the U.S. Air Force by McDonnell Douglas Corporation. The C-17 is designed to provide high payload/long range performance with the ability to deliver its cargo into somewhat austere runways. The aircraft uses an externally blown flap for powered lift to achieve short landing lengths under full load.

70.6.1 Application Area.

The C-17 Avionics System is divided into two major control subsystems: The Communications subsystem and the Mission Computer subsystem. The mission computer subsystem provides all navigation, flight and aircraft maintenance control through the following subsystems:

- Mission Computer/Electronic Display Subsystem (MC/EDS)
- Electronic Flight Control Subsystem (EFCS)
- Head up Display Subsystem (HUD)
- Aircraft Propulsion and Data Management Subsystem (A/PDMS)
- Spoiler Control/Elevator Fuel Subsystem (EC/EPS)

The Communications Subsystem provides control for all audio in the C-17 System and includes only one subsystem: the Integrated Radio Management System (IRMS). The IRMS performs four major control functions for the C-17A system: (1) Control of external communications (air-to-air and air-to-ground) and distribution of associated audio, (2) control of the IFF and radar transponders and associated equipment, (3) navigation audio monitoring and (4) control and distribution of all internal communications (flight and service interphones and public address).

The Communications Subsystem and Mission Computer Subsystem are configured as independent bus systems with separate bus controllers. These control systems are required to pass information to each other through the MCK (part of the MC/EDS). Therefore, each subsystem is required to interface to and function with, the co-existing subsystem, without degradation or interference to either subsystem.

Two other subsystems, the Warning and Caution System (WACS) and the Flight Control Computer (FCC) System also interface to the Mission Computer Subsystem. The WACS interfaces through the Aircraft Propulsion Data Management Computers to provide warning and advisory information to the C-17 crew. The Quad-redundant Flight Control Computer System interfaces to the Mission Bus through the four FCC's.

The Mission Computer and Communications subsystems each have two separate busses. The WACS consists of a single bus. The FCC System has four busses, providing quad redundancy to the critical Electronic Flight Control System. Thus, the C-17A has a total of nine completely independent MlL-STD-1553

data bus systems operating simultaneously. Each data bus system utilizes fully redundant A and B channels per MIL-STD-1553B. The interconnection of the nine C-17 A busses is shown in simplified block diagram form in figure 70-34.

70.6.2 General System Characteristics.

All four C-17 Multiplex data bus systems employ essentialiy the same general MIL-STD-1553B protocol. The paragraphs which follow present a general description of the C-17 bus systems. Unless otherwise noted in this discussion, bus protocol and other descriptions of a general nature apply equally to all nine busses. The general discussion is followed by a more specific description of each of the four bus systems.

70.6.2.1 Overall System Architecture.

An overall block diagram of the C-17A data bus system is shown in figure 70-35. The two major subsystems, Mission Computer and Communications, each consist of two essentially independent data bus systems with maximum physical isolation and minimum functional commonality between them.

The data bus system and all its components associated mainly with the left or pilot's side of the aircraft are identified by -1 designations and the right or co-pilot's side system and components are identified by -2 designations. Data bus Remote Terminals (RT's) are built into the subsystem LRU's and provide the interface functions between the user subsystems and the data busses. Most of the subsystems utilize dual redundant LRU's, with the same configuration units connected to Mission Busses M1 and M2 on the Mission Computer Bus and C1 and C2 on the Communication bus. Redundant RT's have the same address on either bus. Each bus has a primary and a backup bus controller. Mission Computer No. 1 serves as bus controller for Mission bus No. 1 (bus M1) and contains a remote terminal on bus M2. Mission Computer No. 2 is the primary controller for bus M2 and contains an RT on bus M1. Mission Computer No. 3 contains the backup controllers for both busses. Communications Control Unit (CCU) No. 1 serves the communications subsystem as primary bus controller on Communications bus No. 1 (bus C1) and CCU-2 is the backup. CCU-2 is the primary controller on bus C2 and CCU-1 contains the backup.

The WACS bus utilizes a similar architecture except that the WACS system has only one data bus.

The FCC system consists of four essentially independent data bus systems, each controlled by one of four identical Flight Control Computers. The FCC's are cross-coupled by a series of fiber-optic data links.

70.6.2.2 MIL-STD-1553 Compatibility.

The C-17A data busses meet all the electrical characteristics and limits defined by MIL-STD-1553B, Notice 1. Selection of options, interpretations, and additions to the MIL-STD-1553B requirements are contained in three Douglas Aircraft specifications, 17M9U1001 for the Mission Computer bus, 17M9U4001 for the IRMS bus and 17MU9U3005 for the WACS bus.

Acronymns used in Figures

ABC	Anti-Skid, Braketemp Computer
ADC	Air Data Computer
ADI	Attitude Direction Indicator
ADS	Aerial Delivery System
AFCP	Automatic Flight Control Panel
APM	Aircraft Propulsion Data Management Computer
BFPC	Base Flight Plan Computer
CAW	Central Aural Warning

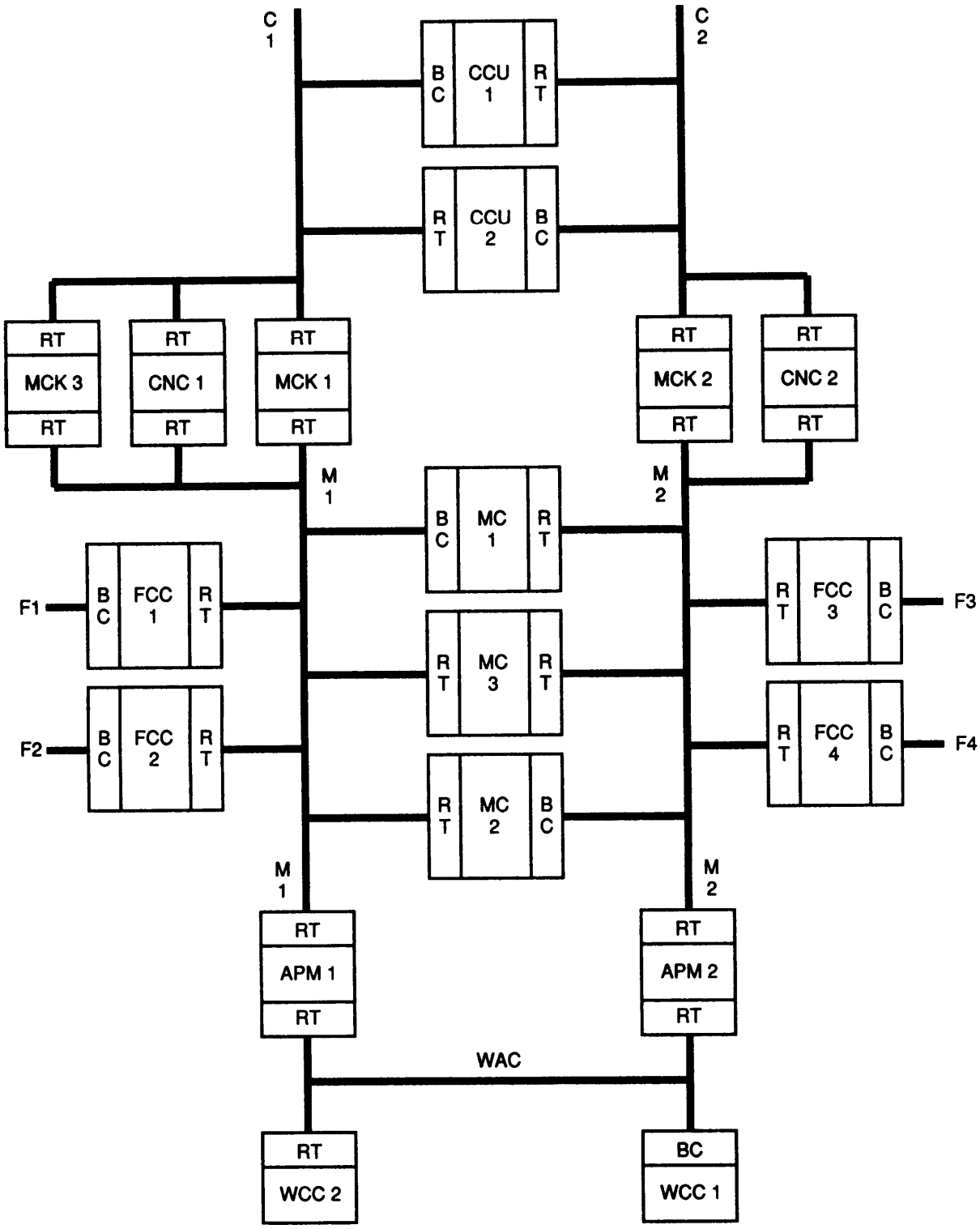


Figure 70-34. Basic Architecture of C- 17A Data Bus System

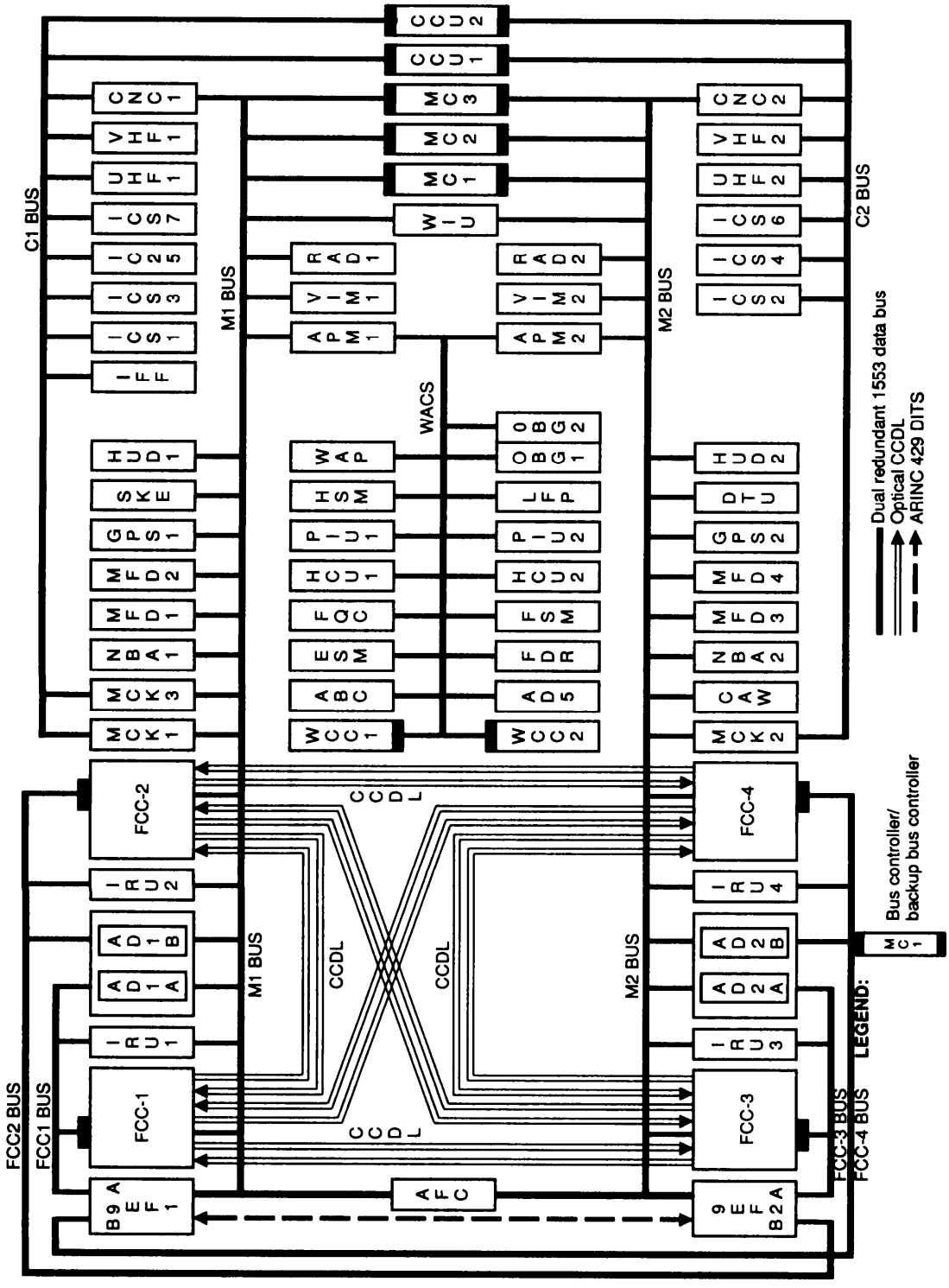


Figure 70-35. C-17 Data Bus System Block Diagram

CCU	Communications Control Unit
CNC	Comm/nav control panel
DTU	Data Transfer Unit
ESM	Environmental System Module
FCC	Flight Control Computer
FDR	Standard Flight Data Recorder
FSM	Fuel System Module
FQC	Fuel Quantity Computer
GPS	Global Positioning System
HSM	Hydraulic System Module
HUD	Head up Display System
HCU	Hydraulic Control Unit
ICS	Inter-Communication Set
IFF	Identification Friend or Foe
IRU	Inertial Reference Unit
MC	Mission Computer
MCK	Mission/Communications Keyboard
MFD	Multi-Function Display
NBA	Navigation Bus Adapter
OBIGG/OBI	On-Board Inert Gas Generating System
PIU	Proximity Interface Unit
RAD	Radar Altimeter
SEF	Spoiler Control/Elevator Feel Computer
SKE	Station Keeping Equipment
VIM	VOR/lLS/Marker Beacon
WACS	Warning and Caution System
WAP	Warning Annunciator Panel
WCC	Backup — Warning and Caution Computer
WIU	Weather Radar Interface Unit

70.6.2.3 **MIL-STD-1553 Deviations.**

The C-17 data bus system implementation contains no deviations from MIL-STD-1553B, Notice 1. The Dynamic Bus Control and Broadcast functions are not allowed per Notice 1. The Bus Controller implements all mode codes and may use all mode codes not restricted by Notice 1. Newly developed RT's, however, need only be able to respond to the C-17 applicable mode codes.

70.6.2.4 **MIL-STD-1553 Options**

Options of MIL-STD-1553B which are implemented in C-17A terminals are shown in table 70-IX.

Table IX. C-17A MIL-STD-1553B Options

MIL-STD-1553B PARAGRAPH	DESCRIPTION	REQUIRED for BC	RT or RT/MON
4.3.3.5.1.2	Terminal Address 31 for Broadcast Option	No	No
4.3.3.5.1.7	Optional Mode Control	Yes	Yes
4.3.3.5.1.7.1	Dynamic Bus Control	No	No
4.3.3.5.1.7.2	Synchronize (without data word)	Yes	Optional
4.3.3.5.1.7.3	Transmit Status Word	Yes	Optional
4.3.3.5.1.7.4	Initiate Self-Test	Yes	Optional
4.3.3.5.1.7.5	Transmitter Shutdown	Yes	Yes
4.3.3.5.1.7.6	Override Transmitter Shutdown	Yes	Yes
4.3.3.5.1.7.7	Inhibit Terminal Flag (T/F) Bit	No	No
4.3.3.5.1.7.8	Override Inhibit T/F Bit	No	No
4.3.3.5.1.7.9	Reset Remote Terminal	Yes	Optional
4.3.3.5.1.7.10	Reserved Mode Codes	No	No
4.3.3.5.1.7.11	Transmit Vector Word	Yes	Optional
4.3.3.5.1.7.12	Synchronize (with data word)	Yes	Optional
4.3.3.5.1.7.13	Transmit Last Command	Yes	Optional
4.3.3.5.1.7.14	Transmit BIT Word	Yes	Optional
4.3.3.5.1.7.15	Selected Transmitter Shutdown	No	No
4.3.3.5.1.7.16	Override Selected Transmitter Shutdown	No	No
4.3.3.5.1.7.17	Reserved Mode Code	No	No
4.3.3.5.3.3	Message Error Bit	Yes	Yes
4.3.3.5.4	Instrumentation Bit	Yes	No
4.3.3.5.5	Service Request Bit	Yes	Optional
4.3.3.5.7	Broadcast Command Received Bit	Yes	No
4.3.3.5.8	Busy Bit	Yes	Optional
4.3.3.5.9	Subsystem Flag	Yes	Yes
4.3.3.5.1	Dynamic Bus Control Accept. Bit	Yes	No
4.3.3.5.1	Terminal Flag Bit	Yes	Yes
4.3.3.6.7	Optional Broadcast Command	No	No
4.4.3.4	Illegal Command Monitors		
	Illegal Subaddress	No	Yes
	Illegal Mode Code	No	Yes
	Illegal Word Count (see Note)	No	Yes
4.5.1.5.1	Transformer Coupled Stub	Yes	Yes
4.5.1.5.2	Direct Coupled Stubs	No	No
4.6	Redundant Data Bus (Dual)	Yes	Yes

NOTE: The Word Count Field of a bus command shall be considered illegal if it exceeds the allowable word count limit for the the associated Terminal Address, T/R and Subaddress fields of the command as specified in the Avionics Interface Control Document (AICD).

70.6.2.4.1 **Status Word Bit Use.**

The following status word bits are implemented by the C-17 Avionics System:

Bit # 9 Message Error
Bit# 11 Service Request (optional)
Bit# 16 Busy (optional)
Bit# 17 Subsystem Flag
Bit# 19 Terminal Flag

Other status word bits defined by 1553B maybe implemented in C-17A RT's, but must be set to logic zero and not used during system-operation. The bus controller is capable of monitoring specific status word bits to recognize RT service requests, RT busy conditions and to detect RT faults.

70.6.2.4.2 Mode Codes

The C-17A Bus Controllers have the capability of using subaddress/mode field 00000 or 11111 to indicate a mode code in a command word, per Notice 1. In the C-17A system, however, subaddress/mode field 00000 is used for mode indication and new C-17 RT's recognize this subaddress as the only mode indication. Subaddress/mode field 11111 is used only with GFE RT's that specifically require use of that mode code.

The Bus Controllers implement all mode codes and may use all mode codes identified in table 70-X and not restricted by Notice 1. Newly developed RT's must be able to respond to the C-17 applicable modes codes listed in table 70-X as a minimum.

70.6.2.5 **Multiplex Cable Assemblies.**

The C-17 data bus cable assemblies are implemented with primary component failure or battle damage. Maximum physical isolation is maintained between the two redundant systems. All MIL-STD-1553B bus stubs are transformer coupled in the ship's wiring at a location remote from the LRU, thus preventing LRU and bus stub failure generated signals from contaminating the bus.

70.6.2.6 **Bus Protocol.**

Each C-1 7 mission computer bus terminal is able to function as a Bus Controller (BC), Bus Monitor (Men) or a Remote Terminal/Bus Monitor (RT/Mon) as determined by its position within the bus system and in subsequent reconfiguration procedures. The terminals in the mission computers function as remote terminals, bus controllers, backup bus controllers, or as secondary backup bus controllers. The terminal performs all these functions as specified by the applicable sections of MIL-STD-1553B.

In addition to the normally defined MIL-STD-1553B transactions, the C-1 7 system also makes use of what is referred to as indirect RT to BC transactions. In this format, the BC commands an RT to RT transaction, and during the transaction the BC itself accepts and validates the message words. The BC has complete control in this transaction since it receives status words from both the transmitter and the receiver as in a normal RT to RT transaction and also performs an independent validation of its received message as in a normal RT to BC transaction.

Table 70-X. C-17A Mode Code Usage

T/R BIT	MODE CODE	ASSOCIATED FUNCTION	DATA WORD
1	00001	Synchronize	No
1	00010	Transmit Status Word	No
1	00011	Initiate Self-Test	No
1	00100	Transmitter Shutdown	No
1	00101	Override Transmitter Shutdown	No
1	01000	Reset Remote Termina	No
1	10000	Transmit Vector Word	Yes
0	10001	Synchronize	Yes
1	10010	Transmit Last Command	Yes
1	10011	Transmit BIT Word	Yes

70.6.2.6.2 **Time Frames.**

Transmissions of data on the data bus are organized in terms of time frames or time slots. A major frame consisting of several minor time frames is used. Data requiring the highest update rates are transmitted during every minor time frame, data requiring lower update rates are transmitted on selected minor time frames.

For example, for preliminary analysis of bus loading, the minor timeframe of the C-17 Avionics System was derived from the maximum data transmit rate requirement of 50 times per second and was 20 milliseconds. Thus, data transmitted in every minor time frame resulted in a transmit rate of 50 times per second. Data transmitted every frame, every other frame, every fourth, and every eighth frame then provided transmit rates of 50.0,25.0,12.5, and 6.25 times per second, respectively. Some examples of data assignments (message assignments) to time frames (slots) are shown in figure 70-36. These examples are for the MC bus. Similar assignments are used for the Communications and WACS busses.

C-17 AVIONICS SYSTEM MIL-STD-1553B DATA BUS M1
MESSAGE ASSIGNMENTS FOR TIME SLOT 1

Source Term.	Dest. Term.	Message I.D.	No. of Words	Data Rate	Message Type
INS1	FCC1	INS1SA-FCC1SA	16	50.0	RT-RT
INS2	FCCI	INSRSA-FCC1SA	16	50.0	RT~-RT
MC2	FCC1	MC2LSX-FCCISY	4	25.0	RT-RT
ADC1	FCC1	ADC117-FCC104	24	25.0	RT-RT
ADC1	INS1	ADC116-INS130	4	25.0	RT-RT
APM1	FCC1	APMI 24-FCC1 SA	18	25.0	RT-RT
APM1	FCC1	APM127-FCC1 SA	19	25.0	RT-RT
FCC1	MC2	FCCISA-MC2LSY	9	25.0	RT-RT
INS1	MC2	INS1SA-MC2LSY	28	25.0	RT-RT
INS1	MC2	INS1SA-MC2LSY	26	25.0	RT-RT
VIM1	FCC1	VIMI SA-FCC1 SY	6	25.0	RT-RT
RAD1	FCC1	RAD1SA-FCC1SY	2	25.0	RT-RT
MC2	MC3	MC2LSA-MC3LSY	12	12.5	RT-RT
ADC1	APM1	ADC117-APM106	25	12.5	RT-RT
AFC1	FCC1	AFC102-FCC1 27	15	6.25	RT-RT
MCD3	USER	MCD3SX-USERSY	14	6.25	RT-RT
APM1	MC2	APM1 18-MC2LSY	13	6.25	RT-RT
SKE	MC2	SKE SX-MC2LSY	14	6.25	RT-RT
VIM1	FSP1	VIM1SX-FS1ISY	2	6.25	RT-RT

Figure 70-36. Example of C- 17A Message Assignments

70.6.2.6.3 **Data Messages.**

Data messages consist of command words, data words and status words per MIL-STD-1553B. The messages and their ID's are constructed and described per Section 80 of this Handbook.

70.6.2.6.4 **Data Blocks.**

Transmitted data words originating at a bus terminal are ordered into functionally related groups or blocks in order to provide efficient transmission of the data to various destinations and at ivarious transmission rates. Each of these groups or parts of groups of words transmitted in a message is assigned a unique block identification, consisting of one alpha and two numeric characters. The alpha character indicates the source of the data and the numeric character identifies the block. Whenever possible, existing block ID's previously assigned to data of GFE or existing equipment is used. Examples of Block ID assignments for the MC bus are shown in figure 70-37.

C-17 AVIONICS SYSTEM MISSION BUS MI
TRANSMITTING SUBSYSTEMS SUBADDRESS/WORD COUNT/RATES

SUBSYS NAME	TERM ADDR	BLOCK I.D.	SUB-ADDR	RECVR	WORD CNT	REFRESH RATE	XMIT RATE	DEST
ADC1	28	C01	17	FCC1	24	25.0	25.0	FCC1
		C06	16	INS1	4	25.0	25.0	INS1
		C06	16	INS3	4	25.0	25.0	INS3
		C07	17	AFC1	15	25.0	25.0	AFC1
		C01	17	APM1	24	12.5	12.5	APM1
		C08	17	SCU1	10	12.5	12.5	ACU1
AFC1	12	X01	02	FCC1	15	6.25	6.25	FCC1
APM1	09	A01	24	FCC1	18	25.0	25.0	FCC1
		A02	27	FCC1	19	25.0	25.0	FCC1
		A03	20	MC2L	32	12.5	12.5	MC2
		A04	23	FCC1	18	6.25	6.25	FCC1
		A05	18	MC2L	13	6.25	6.25	MC2
CNP1	19	P07	02	MC3L	4	6.25	6.25	MC3L

Figure 70-37. Example of C- 17 Block ID Assignments

70.6.2.6.5 **Subaddresses.**

Subaddresses are used to identify messages with different data content originating at the same source RT or arriving at the same destination RT. For C-17A RT's, the following subaddresses are reserved for the function indicated:

T/R Bit	Subaddress	Function
0/1	00000	Mode command indication
0/1	11111	Mode command indication
0	11110	Receive wrap-around test words
1	11110	Transmit wrap-around test words
0	10100	Initiate subsystem built in test
1	10100	Transmit subsystem BIT words

70.6.2.7 **Bus Topology.**

Each C-17 Data Bus consists of dual redundant linear data busses, providing redundant communication channels A and B between the subsystem units. All busses meet the electrical characteristics and limits defined by MIL-STD-1553B, Notice 1.

70.6.2.8 **Fault Isolation and Redundancy Management.**

The bus controller performs all fault management functions associated with the operation of its data bus system. System design is such that the performance of fault management functions do not degrade the operation of the bus system.

On the Mission Computer buses, for example, faults of either the Bus Terminal (channels A and B), Display Processor or Mission Computer functions are considered as faults of the total Mission Computer Unit and cause initiation of bus control reconfiguration procedures.

No reconfiguration is required under RT fault conditions. The mission computer acting as bus controller, is capable of rerouting messages under RT fault conditions.

70.6.2.8.1 **RT and Bus Faults.**

The general philosophy of RT and Bus Fault Management is summarized as follows: Whenever, during a transmission to or from an RT unit, a fault is detected by the BC, the other data bus channel is used to repeat the message. if this message succeeds, all messages to and from that RT are transmitted via the second channel. if the message via the second channel does not succeed, the BC skips the message until its next sceduled occurance. If messages to a given LRU fail the retry three times in succession, all normal messages from that RT are suspended. If the RT is failing in the receiving mode, only messages going to the RT that do not involve an indirect RT to BC message are suspended; i.e., RT to RT messages that go to that RT but are also monitored by other terminal(s) are not suspended.

Periodic polls are conducted for all RT's to check their status. If recovery of an RT is detected, all normal messages with it are re-established. All faults of RT's are recorded and made available for cockpit displays and the BIT/Maintenance System. The fault list for each LRU contains a count for each time the LRU is declared inoperative.

The bus controller uses the following critetia for determining a fault of an RTor the data bus and initiating further fault management actions:

a) No reception of status word.
b) Reception of status word with terminal flag or subsystem flag set.
c) Reception of invalid words or messages.
d) Out-of-tolerance timing of words or messages.

All fault detection methods described in MIL-STD-1553B are utilized. These methods include word and message validation, timing verification and status word bit verification. The analysis and reporting of illegal commands is implemented in the RT's. An RT cannot be adversely affected in its operation by illegal commands.

Polling of all RT's to detect faulty units is conducted only during the BC power-up initialization process and after bus control take-over by the BC. Polling of individual RT's is utilized for fault detection and fault recovery testing during normal operation. Polling includes testing of both data bus channels.

The BC stores all detected and located RT faults in non-volatile memory for its own use and for maintenance purposes. The fault information stored includes identification of the RT, the faulty channel and the type of fault.

The memory is resettable during maintenance actions. The BC provides the Mission Computer with detected RT and bus fault information for fault indication outputs. The BC also makes the fault information available on request to the BIT/Maintenance system.

70.6.2.8.2 **Bus Controller Faults.**

The general philosophy for BC fault management is summarized as follows: If a BC detects its own fault, it hands over bus control to the primary or secondary Backup Bus controller, in that order of priority. All BC faults are recorded and made available for cockpit displays and the BIT/Maintenance System. Backup bus controller can force takeover of bus control from a faulty BC when two healthy BBCs are in agreement via the discrete interface.

The critetia that the BBCs use for determining faults of the Bus Controller are:

a) Generation of invalid or illegal words and messages on either bus channel for 20 milliseconds.
b) Absence of message transmission on both data bus channels for 20 milliseconds.
c) RT/MON (BBC) fails to receive valid minor frame synchronization message during a 22 millisecond period.

In addition to the 1553B fault detection methods such as word and message validation, timing and status word verification, the Bus Controller performs self-testing to detect internal failures and malfunctions and monitors its own data bus outputs. The self-monitoring has the ability to identify a single channel fault and is able to determine whether it is an internal (BC) or an external (data bus) fault.

The Backup Bus Controllers monitor the message traffic on the data bus and verify the validity and legality of the active Bus Controller's words and messages and the absence of any messages.

Failure of the Active Bus Controller results in the transfer of bus control to a backup bus controller either as a handover or a forced takeover.

Bus Control Handover

An active Bus Controller (normal BC, Primary BBC or Secondary BBC) upon detection of any fault, except a single channel fault, hands over bus control to one of the other bus controllers depending on their status. The handover priority is such that the handover is to the the Primary BBC first and if the primary BBC is faulty then to the Secondary BBC. The bus control handover time is less than ten milliseconds.

Backup Bus Controller Takeover

Forced takeover of bus control from a faulty BC is accomplished when both BBCs determine a condition where an active Bus Controller is malfunctioning and is not detecting its malfunction. In this case, the faulty unit is shut down by use of a discrete interface. Examples of takeover criteria would be the absence of any message on both busses during a minor frame, or detection of repeated invalid or illegal messages. Bus takeover will take place in less than ten milliseconds.

Manual BC Selection

The Bus Controllers have the capability to override the normal automatic reconfiguration logic when discrete functional selection inputs are provided from external manual switches on the pilot's and copilot's Avionics Switching Control Panel (ASCP). When the switch is moved from the AUTO position, the Mission Computer specified by that switch becomes the BC regardless of health of the MC. An MC which has previously failed due to a self-detected fault, however, will not become active when manually selected. Switching either the pilot's or co-pilot's MC Select switch from the AUTO position with not inhibit automatic bus control reconfiguration on the other side.

70.6.2.9 **Inter-Bus Transactions.**

The MC's and MCK's act as gateways, transferring data between two data bus networks, the MC's between Mission buses and the MCK's between a Mission bus and a Communication bus. In both cases the inter-bus data transfers are accomplished by the bus interface (BI) without host assistance or intervention.

70.6.2.9.1 **Between Mission Busses.**

Within the MC's, data transfer between data buses may be accomplished by two methods. The first method consists of using an RT to BC or RT to RT indirect transfer to the BC on the source data bus, with the BC storing the data in RAM which is accessible to the BI interfacing the MC to the destination RT on the other bus, then an RT to RT (director indirect) transfer from the MC to the RT on the destination bus.

The second method consists of an RT to RT (MC) transaction on the source bus to the MC containing the BI which is BC on the other bus, with the RT storing the data in RAM which is accessible to the BC on the destination bus, then a BC to RT transaction on the destination bus.

For those cases where data required by the application software of the MC/BC and the MC/SBBC is transferred via an RT to RT (indirect) message to a non-MC RT on the source bus, the MC/BC on the source bus receives and validates the data, then an RT to RT indirect transfer is used on the destination bus to provide the data from the gateway MC to a non-MC RTand the MC/BC on the destination bus (which is the MC/SBBC on the source bus).

The MC's have the capability to execute both methods of transferring data between the Mission Buses as described above. The selection of the method used is be made with the objective of minimizing bus loading, data latency and Bus Controller complexity, and maximizing inter-bus fault isolation and maintainability.

A sample list of various inter-bus transactions from Mission bus M1 to bus M2 is shown in figure 70-38.

70.6.2.9.2 **Mission Bus to Other Busses.**

Certain subsystem LRU'S on the Mission and and Communication Busses are connected to other MIL-STD-1553B data busses. These LRU's are capable of transferring data to and from the other busses. All C-17A data busses operate asynchronously. Within the MCK's, for example, data transfer between data buses is accomplished via shared memory. The MCBI receiving gateway data from the source bus stores the data in RAM which is accessible to the MCK/BI interfacing to the destination bus.

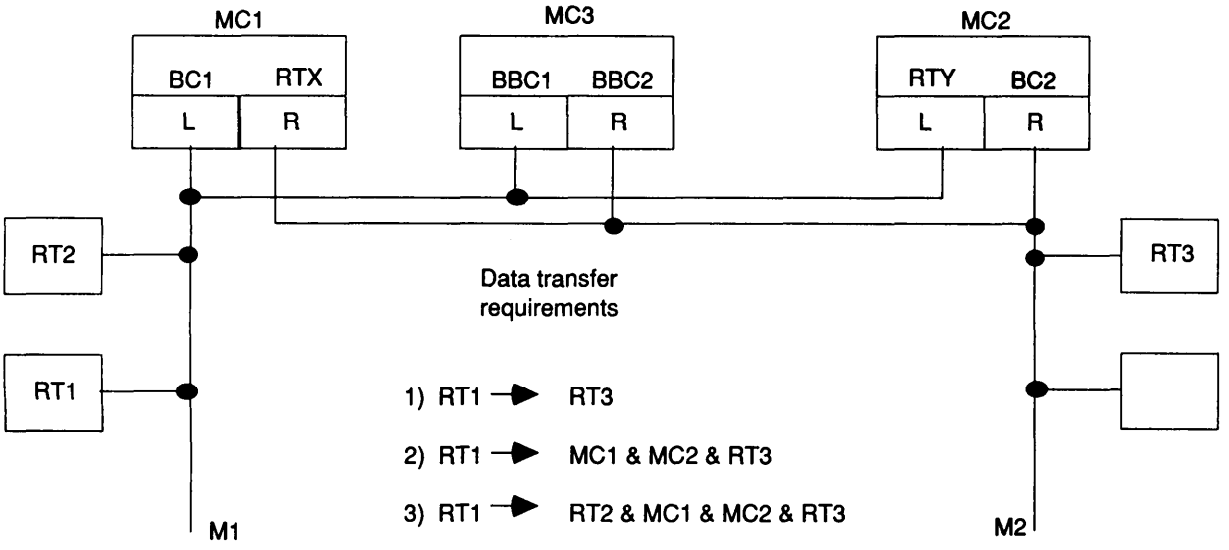
Terminals acting as gateways between two buses have the following inter-bus data transfer capabilities:

a. The MC implements extended addressing so that data transfers from one bus to the other will not be limited by the normal quantity of 30 subaddresses, but will allow identification and tracking of a large number of messages and meet the inter-bus data latency requirements. Note that extended addressing is not required in the MCK.

b. The LRU has the capability to associate a receive subaddress on one bus with a transmit subaddress on the other bus such that when the bus terminal is required to transmit a message from the transmit subaddress, it will transmit the message previously received by the associated subaddress on the other bus.

c. The LRU is able to associate a single receive subaddress on one bus with multiple transmit subaddresses on the other bus.

d. It is possible to allocate all unreserved subaddresses on each bus for inter-bus data transfer. The same subaddress number may be used for a transmit and a receive subaddress.



Available transactions

	BUS M1			BUS M2
1.A)	RT1-BC1	and		RTX-RT3
or 1.B)	RT1-RTY	and		BC2-RT3
2.A)	RT1-BC1	and		RTX-RT3, BC2
or 2.B)	RT1-RTY, BC1	and	or	BC2-RT3 RTX-RT3
3.A)	RT1-RT2, BC1	and		RTX-RT3,BC2
3.B)	RT1-RT2, BC1 and RT1-RTY	and	or	BC2-RT3 RTX-RT3, BC2
3.C)	RT1-RT2 and RT1-RTY, BC1	and	or	BC2-RT3 RTX-RT3, BC2

Figure 70-38. C-17A Inter-Bus Transactions

e. Messages received on one bus are available for transmission on the other bus such that inter-bus data latency requirements are met.

f. No Main CPU intervention is required to effect the transfer of message data between buses.

g. The transmit subaddress on one bus has the capability to transmit the number of words specified by the command word even if the number of words is less than the number of words contained in the message received on the other bus.

Inter-bus communication is held to a minimum and represents a very small percentage of total bus loading, as summarized in table 70-XI.

Table 70-XI. C-17A Inter-Bus Communication Summary

TRANSFER BUSSES	GATEWAY	DATA TYPE	% LOADING
IRMS TO MISSION		NONE	0.0
	MCK 1,2	IRMS FAULT DATA/ RADIO KEYING	0.2
		TOTAL LOADING	0.2
MISSION TO IRMS		VIM ECHOS	0.2
	MCK 1,2	IFF Air Data, GMT, CNC/MCK Fault Data	0.1
		TOTAL LOADING	0.3
MISSION TO WACS	A/PDMC	Air Data	0.2
		Recorder Data	0.4
		Inertial Data	0.01
		Alerts	0.01
		TOTAL LOADING	0.6
WACS TO MISSION	A/PDMC	Brake Data	0.3
		Airdrop	0.08
		Fuel	0.1
		Hydralic	0.1
		OBIGG	0.2
		Plu	0.2
		WACS Fault Data	0.2
		TOTAL LOADING	1.2

70.6.2.9.3 **Inter-Bus Data Latency.**

The maximum data latency, i.e., the time between its transmission from an RT on one bus and its reception by an RT on the other bus,including latency jitter and internal data transfer within the MC or MCK connected to the two buses is as follows under normal conditions:

DATA RATE (Samples/Second)	MAXIMUM LATENCY (Milliseconds)
50	21
25	41
12.5	81
6.25	161

Data bus faults, LRU faults and fault management procedures may cause data to have additional latency and may cause intermittent absences of data. Under these conditions the above maximum latency numbers do not apply.

70.6.2.10 **Bus Loading.**

The total LRU count and estimated bus loading for each of the busses in the C-17A data bus system is summarized in table 70-XII.

Table 70-XII. C-17A LRU Count and Bus Loading Summary

BUS	TERMINAL COUNT	SPARE RT ADDRESSES	BUS LOADING (%) NOMINAL	PEAK
IRMS C-1	12	20	16	N/A
IRMS C-2	10	22	<16	N/A
MISSION M-1	24	7	65	68
MISSION M-2	24	7	61	64
WACS	26	5	38	N/A
FCC-1	4	28	17	N/A
FCC-2	4	28	17	N/A
FCC-3	4	28	17	N/A
FCC-4	4	28	17	N/A

70.6.3 **Bus Descriptions (Architecture)**

70.6.3.1 **Mission Computer Bus.**

70.6.3.1.1 **Bus Architecture.**

A block diagram of the C-17A Mission Computer Data Bus System is shown in figure 70-39. The Mission Computer Bus (also called the Mission Bus or the Avionics Bus) consists of two essentially independent MIL-STD-1553B dual bus systems. The two busses are controlled by three Mission Computers. MC-1 normally provides bus control on bus Ml and acts as an RT on bus M2. Likewise MC-2 is bus controller for bus M2 and RT on M1. MC-3 contains two bus controllers and provides backup bus control for both busses. The RT's contained in MC-1 and MC-2 are also capable of bus control and act as secondary backups to MC-3, providing triply redundant bus controllers. Thus, the two Avionics busses share a combined total of six bus controllers and 43 remote terminals identified as follows:

BUS CONTROLLERS

Bus M1 Normal — Mission Computer No. 1 (MC-1L)
Bus M2 Normal — Mission Computer No. 2 (MC-2R)
Bus M1 Primary Backup — Mission Computer No. 3 (MC-3L)
Bus M2 Primary Backup — Mission Computer No. 3 (MC-3R)
Bus M1 Secondary Backup — Mission Computer No. 2 (MC-2L)
Bus M2 Secondary Backup — Mission Computer No. 1 (MC-1 R)

Mission Computer No. 1 (MC-1 R)
Mission Computer No. 2 (MC-2L)
Mission Computer No. 3 (MC-3L, MC-3R)
Mission/Communication Keyboard 1 (MCK-1)
Mission/Communication Keyboard 2 (MCK-2)
Mission/Communication Keyboard 3 (MCK-3)
Communication/Navigation Control Panel 1 (CNC-1)
Communication/Navigation Control Panel 2 (CNC-2)

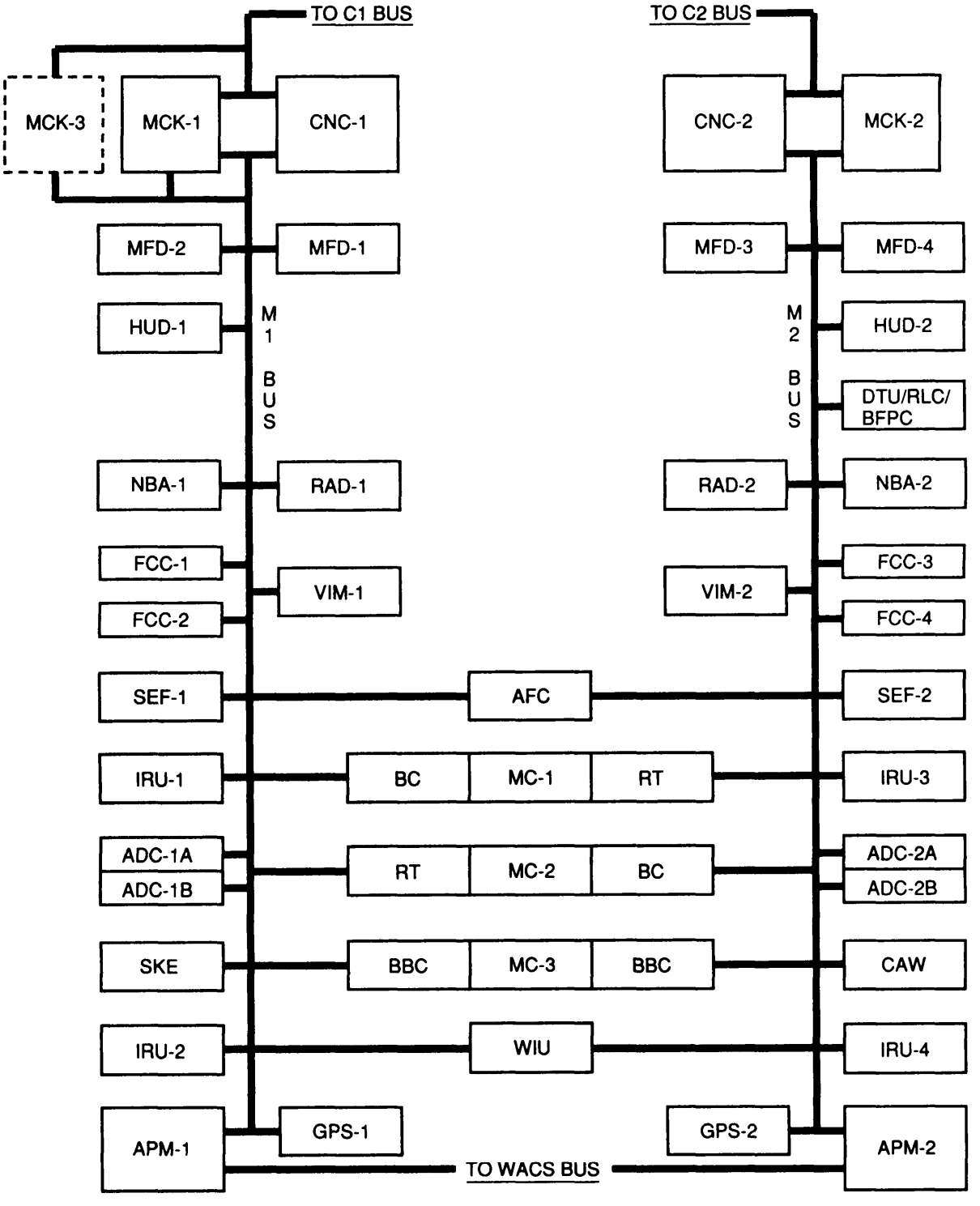


Figure 70-39. C-17A Mission Computer Bus Block Diagram

Multifunction Display 1 (MFD-1)
Multifunction Display 2 (MFD-2)
Multifunction Display 3 (MFD-3)
Multifunction Display 4 (MFD-4)
Head-Up-Display 1 (HUD-1)
Head-Up-Display 2 (HUD-2)
Data Transfer Unit/Remote Laptop Computer/Base Flight Plan Computer (DTU/RLCBFPC)
Nav Bus Adapter 1 (NBA-1)
Nav Bus Adapter 2 (NBA-2)
Flight Control Computer 1 (FCC-1)
Flight Control Computer 2 (FCC-2)
Flight Control Computer 3 (FCC-3)
Flight Control Computer 4 (FCC-4)
VOR/ILS/Marker Beacon 1 (VIM-1)
VOR/ILS/Marker Beacon 2 (VIM-2)
Spoiler Control/Elevator Feel Computer 1 (SEF-1)
Spoiler Control/Elevator Feel Computer 2 (SEF-2)
Inertial Reference Unit 1 (IRU-I)
Inertial Reference Unit 2 (IRU-2)
Inertial Reference Unit 3 (IRU-3)
Inertial Reference Unit 4 (IRU-4)
Air Data Computer 1A (ADC-1A)
Air Data Computer 1B (ADC-1B)
Air Data Computer 2A (ADC-2A)
Air Data Computer 2B (ADC-2B)
Station Keeping Equipment (SKE)
Central Aural Warning (CAW)
Automatic Flight Control Panel (AFCP)
Aircraft Propulsion Data Management Computer 1 (APM-1)
Aircraft Propulsion Data Management Computer 2 (APM-2)
Radar Altimeter 1 (RAD-1)
Radar Altimeter 2 (RAD-2)
Weather Radar Interface Unit (WIU)
Global Positioning System 1 (GPS-1)
Global Positioning System 2 (GPS-2)

70.6.3.1.2 **System Control.**

System control for the Mission Computer (MC) busses is accomplished by the the three mission computers, each of which contains two terminals as indicated in figure 70-39. This architecture provides triply redundant bus control functions, designated as Normal, Primary Backup and Secondary Backup.

70.6.3.1.3 **Bus Controller**

For Mission Bus Ml, terminal MC-1 L is the normal Bus controller, MC-3L is the primary Backup Bus Controller and normally functions as an RT/Monitor. MC-2L is the secondary Backup Bus controller and normally functions as an RT/Monitor.

For Mission Bus M2, terminal MC-2R is the normal Bus controller, MC-3R is the primary Backup and normally functions as an RT/Monitor. MC-1R is the secondary Backup and normally functions as an RT/Monitor.

70.6.3.1.4 **Remote Terminal.**

The C-17 Avionics data bus system interfaces with and provides complete communication with 31 subsystems as listed in section 70.6.3.1.1. All RT's are integral to the subsystem which they serve with the exception of the NBA and WIU. The NBA is a separate interface adapter which converts MIL-STD-1553 data to the format of the standard DME and BDHI instruments. The WIU provides a MIL-STD-1553 interface for the weather radar.

Eight of the Remote Terminals have dual RT interfaces. The WIU and AFC interface to both Mission Computer buses (M1 and M2). APM-1 and APM-2 also interface to the WACS bus. MCK-1 and -2 and CNC-1 and -2 act as RT's on Communications busses C1 and C2 as well as the Mission busses.

70.6.3.2 **Integrated Radio Management (IRMS) Bus.**

70.6.3.2.1 **Bus Architecture.**

The IRMS Bus consists of two essentially independent MIL-STD-1553B dual bus systems with much the same architecture as the Avionics bus. The two busses are designated Communication Bus 1 and 2 (C1 and C2) and are controlled by two Communication Control Units. CCU-1 and CCU-2 each act as Bus controller on one of the Communication busses and Backup Bus Controller on the other. The two Communication busses share a combined total of four bus controllers and eighteen remote terminals identified as follows:

BUS CONTROLLERS

Bus C1 Primary — Communications Control Unit No. 1 (CCU-1)
Bus C1 Backup — Communications Control Unit No. 2 (CCU-2)
Bus C2 Primary — Communications Control Unit No. 2 (CCU-2)
Bus C2 Backup — Communications Control Unit No. 1 (CCU-1)

Intercommunication Set Control 1 (ICSC-1)
Intercommunication Set Control 2 (ICSC-2)
Intercommunication Set Control 3 (ICSC-3)
Intercommunication Set Control 4 (ICSC-4)
Intercommunication Set Control 5 (ICSC-5)
Intercommunication Set Control 6 (ICSC-6)
Intercommunication Set Control 7 (ICSC-7)
Identification Friend or Foe 1 (IFF-1)
Identification Friend or Foe 2 (IFF-2)
UHF Communications No. 1 (UHF-1)
UHF Communications No. 2 (UHF-2)
VHF Communications No. 1 (VHF-1)
VHF Communications No. 2 (VHF-2)
Mission/Communications Keyboard 1 (MCK-1)
Mission/Communications Keyboard 2 (MCK-2)
Mission/Communications Keyboard 3 (MCK-3)
Communications Navigation Control Panel 1 (CNC-1)
Communications Navigation Control Panel 2 (CNC-2)

A Block Diagram of the IRMS bus is shown in figure 70-40. CCU-1 normally acts as bus controller on bus Cl and backup on bus C2. Likewise CCU-2 is primary bus controller on bus C2 and backup on bus Cl.

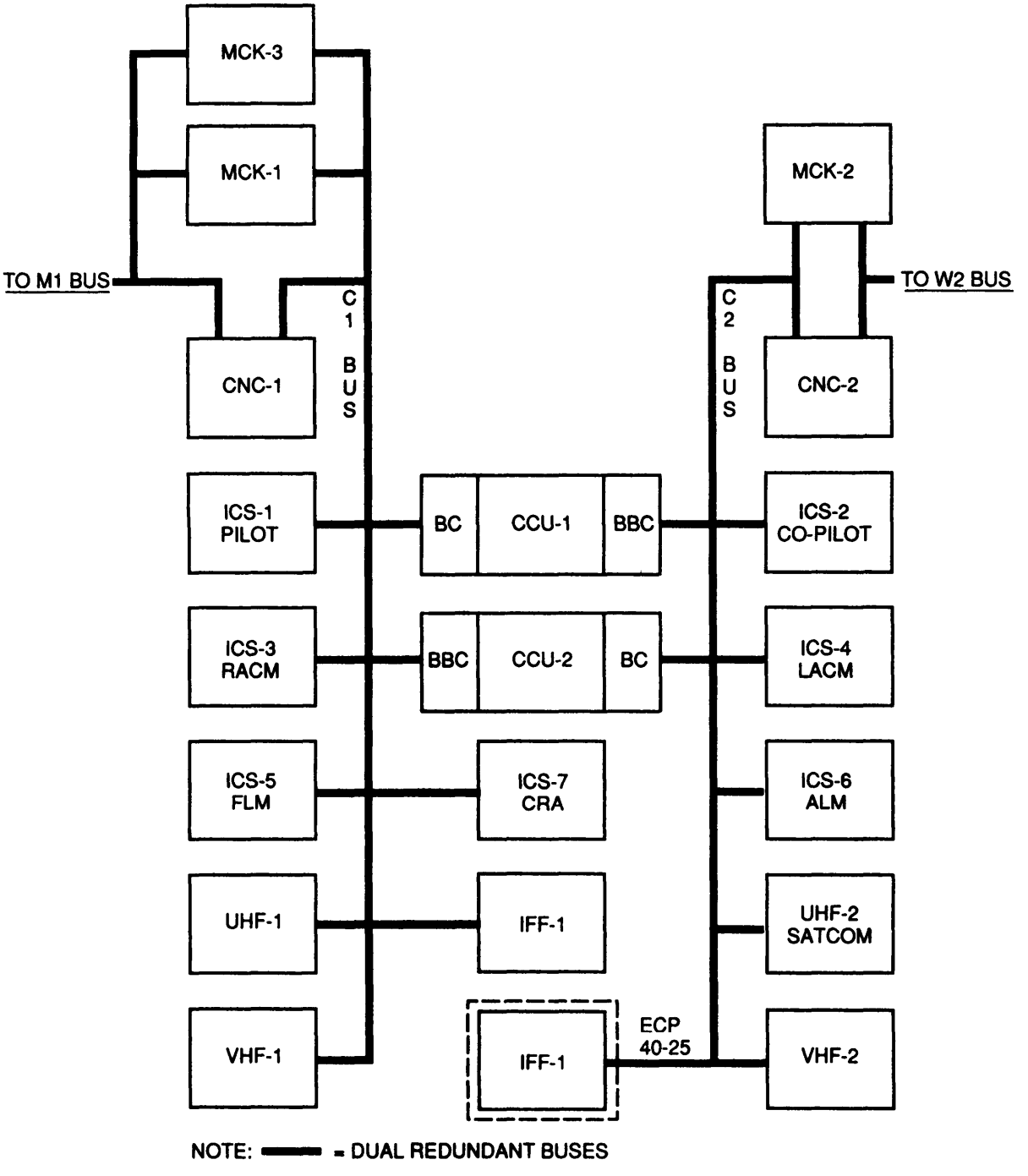


Figure 70-40. C-17A IRMS Data Bus Block Diagram

70.6.3.2.2 **System Control.**

System control for the IRMS Communication busses is accomplished by the the two Communication Control Units (CCU), each of which contains two terminals as indicated in figure 70-40. This architecture provides redundant bus control functions, designated as Primary and Secondary, on each of the two Communication busses.

70.6.3.2.3 **Bus Controller.**

The Bus Controllers provide the bus access and message transfer controls on each data bus and are located within the Communications Control Units. Each CCU provides two independent bus controller functions, one for each Communications bus and an inter-bus data transfer function. Thus, the CCU's provide dual redundant bus control functions for each data bus. The bus controller terminals in the two CCU's that are connected to Communication Bus Cl are identified as CCU-1L and CCU-2L. The bus controller terminals connected to bus C2 are identified as CCU-1 R and CCU-2R. Each CCU has a backup bus controller to provide bus access and message transfer control on each data bus in the event of a failure of the primary bus controller.

70.6.3.2.4 **Remote Terminal.**

Data bus remote terminals built into the individual LRU'S provide the interface functions between the user subsystems and the data busses. Most of the subsystems employ redundant LRU's, with the same configuration connected to Communication busses Cl and C2. Five Remote Terminals on the IRMS bus have dual RT interfaces. MCK-1,-2 and ,-3 and CNC-1 and -2 act as RT's on Mission Computer busses M1 and M2 as well as on the Communication busses.

70.6.3.3 **Warning and Caution System (WACS) Bus.**

70.6.3.3.1 **Bus Architecture.**

A block diagram of the WACS data bus system is shown in figure 70-41. WACS is the only C-17A data bus system which does not contain multiple busses. The WACS bus consists of a single, dual- redundant, MIL-STD-1553B data bus with a primary and backup bus controller and 23 remote terminals identified as follows:

BUS CONTROLLERS

Primary — Warning and Caution Computer 1 (WCC-1)
Backup — Warning and Caution Computer 2 (WCC-2)

REMOTE TERMINALS

Anti-Skid, Braketemp Computer (ABC)
Standard Flight Data Recorder (FDR)
Proximity Interface Unit 1 (PIU-1)
Proximity Interface Unit 2 (PIU-2)
Fuel Quantity Computer (FQC)
Fuel System Module (FSM)
Hydraulic Control Unit 1 (HCU-1)
Hydraulic Control Unit 2 (HCU-2)
Hydraulic System Module (HSM)
Environmental System Module (ESM)
Warning Annunciator Panel (WAP)
On-Board Inert Gas Generating System 1 (OBG-1)
On-Board Inert Gas Generating System 2 (OBG-2)
Aircraft Propulsion Data Management Computer 1 (APM-1)

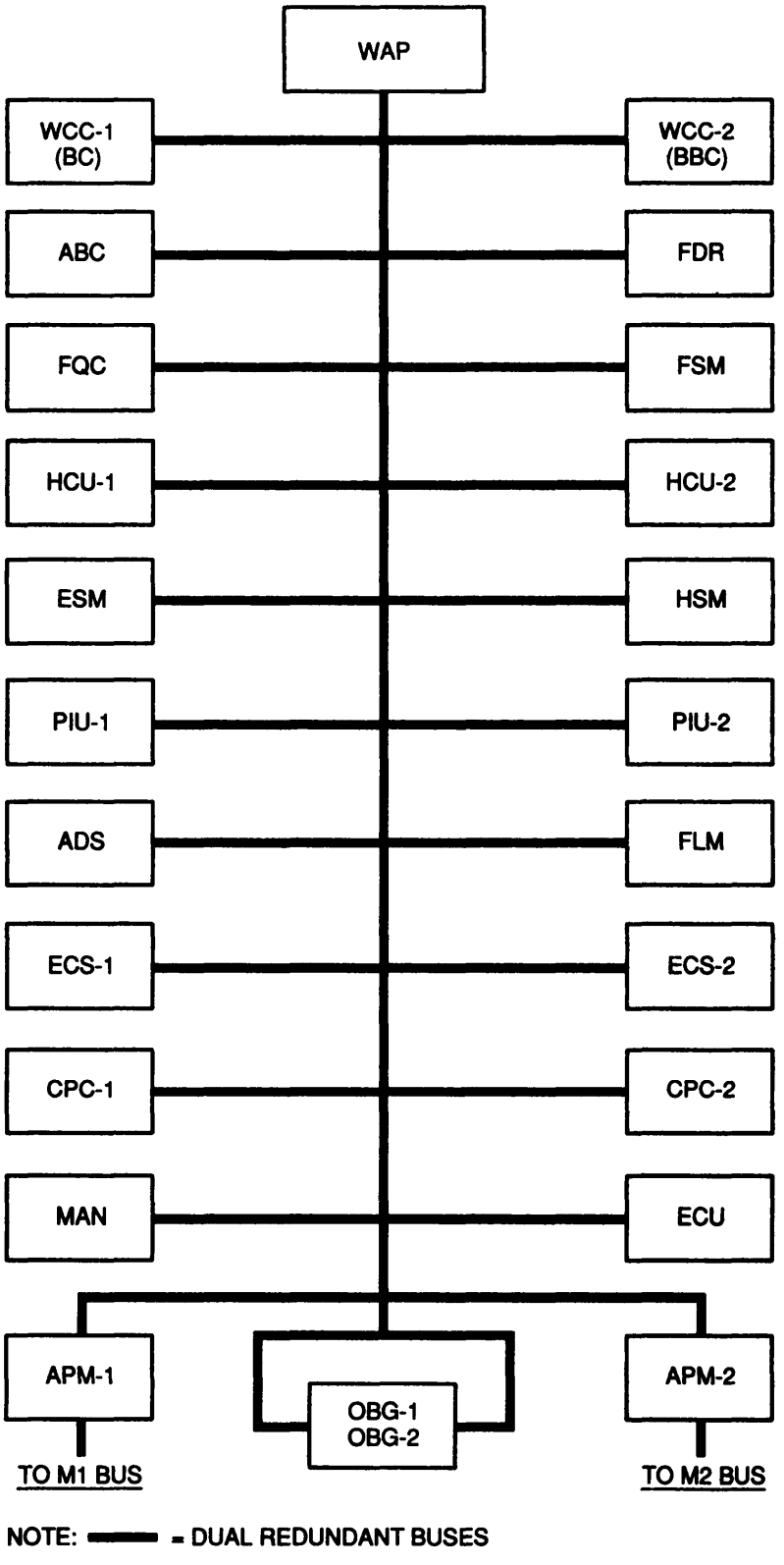


Figure 70-41. C-17A WACS Data Bus Block Diagram

Aircraft Propulsion Data Management Computer 2 (APM-2)
Aerial Delivery System (ADS)
Fomvard Loadmaster Panel (FLM)
Environmental Control System 1 (ECS-1)
Environmental Control System 2 (ECS-2)
Cabin Pressure Controller 1 (CPC-1)
Cabin Pressure Controller 2 (CPC-2)
Manifold Failure Detection (MAN)
Electrical Control Unit (ECU)

70.6.3.3.2 **System Control.**

System control for the Warning and Caution System (WACS) busses is accomplished by the the two Warning and Caution Computers (WCC). Each WCC contains a single MIL-STD-1553B terminal as indicated in figure 70-41. This architecture provides redundant bus control functions, designated as Primary and Secondary, for the WACS bus.

70.6.3.3.3 **Bus Controller.**

The bus controllers provide the bus access and message transfer control on the data bus and are located within the Warning and Caution Computers (WCC). WCC-1 is the primary bus controller and WCC-2 is the backup. The two WCC's thus provide dual redundant bus control functions for the WACS data bus.

70.6.3.3.4 **Remote Terminal.**

A data bus remote terminal is embedded into each of the individual WACS LRU's to provide the interface functions between the user subsystems and the data bus. The RT interfaces with both data bus channels to provide redundant communication paths between a subsystem unit andthedata bus. The overhead Warning Annunciator Panel (WAP) contains two remote terminals, designated as left and right WAP (WAPL and WAPR). The Aircraft Propulsion Data Management Computers, APM-1 and APM-2, are considered a part of the Avionics Bus but also have RT's on the WACS bus (See paragraph 70.6.3.1.1).

70.6.3.4.1 **Flight Control Computer (FCC) Bus.**

The FCC Bus system could be more accurately described as a subset of the Mission Computer Bus, as can be seen in figure 70-42. The FCC bus actually consists of four separate, identical busses, providing full quad redundancy for the critical Flight Control System. Each of the four busses consists of a single bus controller and three remote terminals identified as follows:

Flight Control Computer 1 (FCC-1)
Flight Control Computer 2 (FCC-2)
Flight Control Computer 3 (FCC-3)
Flight Control Computer 4 (FCC-4)

Air Data Computer 1 (ADC-1)
Air Data Computer 2 (ADC-2)
Air Data Computer 3 (ADC-3)
Air Data Computer 4 (ADC-4)

Inertial Reference Unit 1 (INU-1)
Inertial Reference Unit 2 (INU-2)
Inertial Reference Unit 3 (INU-3)
Inertial Reference Unit 4 (INU-4)
Spoiler Control/Elevator Feel Computer 1 (SEF-1)
Spoiler Control/Elevator Feel Computer 2 (SEF-2)
Spoiler Control/Elevator Feel Computer 3 (SEF-3)
Spoiler Control/Elevator Feel Computer 4 (SEF-4)

70.6.3.4.2 **System Control.**

System Control for the Flight Control Computer (FCC) bus system is accomplished by the four Flight Control Computers (FCC). Each FCC contains two MIL-STD-1553B terminals as indicated in figure 70-42. One of the terminals acts as an RT on one of the Mission Busses and the other serves as the Bus Controller for one of the FCC busses. FCC-1 and FCC-2 are RT's on Mission Bus 1 (M-1) while FCC-3 and -4 communicate with the Mission System via M-2.

The four FCC busses operate independently, providing full quad redundancy for the flight control system. Cross-monitoring by a 40 MHz fiber optic data link assures that the same flight data isavailable from each FCC. The Mission Computer automatically selects one FCC from each side as a source for the pilot's and copilot's displays. The pilot and copilot are each provided manual selection for three of the four IRU'S and ADC's. The normal sensor of the opposite crew member cannot be manually selected.

70.6.3.4.3 Bus Controller.

The bus controllers provide the bus access and message transfer control on the data bus and are located within the FCC'S. Each FCC is the sole bus controller for it's bus. There is no provision for redundant bus control.

70.6.3.4.4 Remote Terminal.

A data bus remote terminal is embedded into each of the individual FCC system LRU's to provide the interface functions between the user subsystems and the data bus. The RT interfaces with both data bus channels to provide redundant communication paths between a subsystem unit and the data bus. Each of the user subsystems contains two remote terminals, one on the FCC bus and the other providing communication with one of the Mission Busses. All of the terminals on the FCC bus, including the FCC, are also RT's on one of the Mission busses.

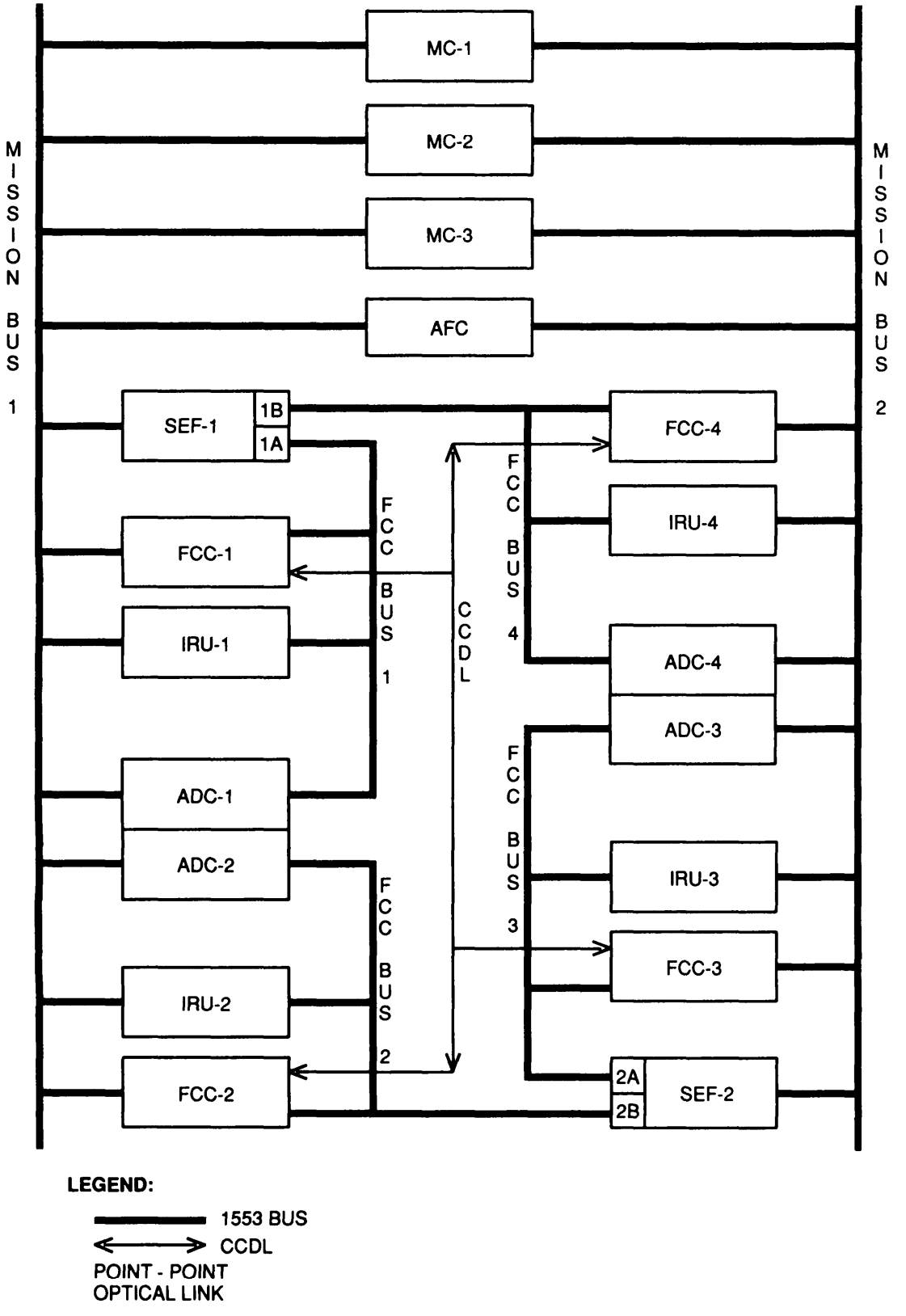


Figure 70-42. C-17A FCC Data Bus Block Diagram

SECTION 70 INDEX

SECTION 80

PARAMETER FORMATS

CONTENTS

FIGURES

TABLES

80. DATA WORD AND MESSAGE FORMAT GUIDELINES

FOREWORD

Section 80 has been updated as a result of Notice 2 approval, suggestions and corrections recommended by users, and anticipation of future applications. Specifically, the following updates have been made.

Two data words have been added tothe Time category - Pulse Repetition Interval (PRI) and Pulse Width. Two vector word formats have been added - one for Asynchronous Message Demand, and one for Asynchronous Action Demand. A table of suggested data word sequencing has been added to the "General Rules for Message Construction" paragraph. Notice 2 considerations have been noted for Command and Status words. The BCH generating polynomial in the Error Protection data word has been corrected. The Broadcast Command Receive bit has been set to zero in the Transmit Status Word. "UTM" designation has been replaced by "MGRS".

Additionally, editorial changes and clarifying notes have been added throughout the section.

80. 1 Introduction

The emphasis in this chapter is the development of data word and message formats for MIL-STD-1553 data bus applications. This chapter is intended as a guide for the designer to identify standard data words and messages for use in avionic systems and subsystems. These standard words and messages, as well as the documentation format for interface control document (ICD) sheets, provide the basis for defining 1553 systems. Also provided in this chapter is the method for developing additional data word formats and messages that may be required by a particular system but are not covered by the formats provided herein. It is essential that any new word formats or message formats that are developed for a 1553 application follow the fundamental guidelines established in this chapter in order to ease future standardization of these words and messages. The standard word formats presented represent a composite result of studies conducted by the U.S. Army, Navy, and Air Force (see References 1, 2 and 3, respectively).

References

1. MIL-STD-1553 Data Word Standardization Technical Report, STR-DD-81273-1, SEMCOR, September 1981, U.S. Army Avionics R&D Activity, Contract No. DAAK80-79-C-0258.

2. AAAS Multiplex Armament Data Word Standardization Study, 4092 TM-81 BASIC-006, SEMCOR, February 1981, Na!val Air Development Center, Contract No. N62269-78-C-0302.

3. MIL-STD-1553 Multiplex Data Bus Word Format Study, Boeing Military Airplane Company, October 1981, USAF/ASD Contract No. F33615-80-C-0124.

In accordance with Public Law 94-168, Metric Conversion Act of 1975, and Department of Defense (DOD) Directive 4120.18, Use of Metric System of Measurement, metric units are preferred for use in new systems. (Reference National Aerospace Standard NAS1OOO1, Preferred Metric Units for Aerospace, which lists the preferred metric units and conversion factors for a number of commonly used quantities in the aerospace industry.) However, when the use of metric units is not practical, the English units presented in this document may be used.

The necessity for standardizing data word and message formats became evident as more and more subsystems provided 1553 interfaces as the basic input and output communication interface. Without coordination of these interfaces, outputs from a subsystem were incompatible with the input requirements of the interfacing subsystem. When new 1553 hardware and systems are designed, the system designer is responsible for identifying the interface requirements of all devices and establishing compatible words and

messages for proper communications. Naturally, this is accomplished during the early system development phases and is then reflected in future procurement specifications for the subsystem elements of the design. This method provides an integrated system that meets all the individual communication requirements. However, as more 1553 systems are developed, this approach may result in subsystems that are incapable of exchanging data because of word and message formatting differences, even though the units meet all the requirements of MIL-STD-1553 and their individual procurement specifications. In this case, t he system designer is faced with thechoiceof using additional processing equipment to translate words and messages from one subsystem to another or modifying the off-the-shelf hardware to achieve integration. Usually the job of data manipulation falls on the bus controller-processor. Messages from each subsystem must be transmitted to the bus controller (RTto bus controller), which constructs new words with the appropriate engineering units, scaling, encoding, bit positions, etc., before retransmission (bus controller to RT) to the subsystem requiring the data. Word order is another message inconsistency that must be resolved. The solution to this problem does not lie in bus controller manipulation or in subsystem modifications; it lies in establishing common usage word formats and common usage output message formats to provide a subsystem designer the information required to build compatible communication interfaces.

This chapter is subdivided to allow easy access when selecting the appropriate word or message format from the standards available. For signals that do not fit the standard word formats available, guidelines are provided for establishing the appropriate word format. Common signal naming practices and an ICD presentation format are provided. Some of the key benefits gained by use of the principles presented in this chapter will be(1) subsystem word format definition, (2) common signal naming practices, and (3) standardization of ICD format across programs. The guidelines required for developing message formats and an ICD presentation format are also provided.

80.2 Word Formats

A word format is the structure, order, and value represented by the bits in a signal data transmission. To properly define a data word format requires knowledge concerning the signal, the 1553 application, and the coding technique used to communicate the information. All of these elements are discussed in the following paragraphs.

The general rules for 1553 word construction (paragraph 80.2.2) apply to all data words whether standard or nonstandard. These rules are to be followed in the development of words that do not fit the formats listed in the standard word tables (paragraph 80.2.5). The procedures on how to construct a data word format described in paragraph 80.2.3 also apply to any data word whether or not it is eventually determined to fit a standard format. Paragraph 80.2.1 describes the standardized ICD presentation format that should be used for all 1553 words.

80.2.1 Interface Control Document Signal Presentation Format

The ICD format required for the documentation of all words in a 1553 system is shown in tables 80-I and 80-II. Presentation formats are provided for single word (table 80-I) and double precision (table 80-II). Signals that require more than two words should use the single word format with the number of words indicated in the REMARKS section (e.g., “3 word quantity-word 1 of 3“) of the word format presentation sheet. The ICD presentation sheet entries are discussed in paragraph 80.2.2.

80.2.2 General Rules for MIL-STD-1553 Word Construction

The general rules for constructing compatible word formats apply to the standard words listed in paragraph 80.2.5 and to those words that do not meet the requirements for the standardized format. The following paragraphs provide generalized rules for establishing the basic word structure.

Table 80-I. Presentation Format, Single Word

DOC. NO. REV.
DATE
SHEET 1 OF

WORD NAME :

WORD ID :
SOURCE(S) :
DEST(S) :
COMP RATE :
XMIT RATE :
SIGNAL TYPE :
UNITS :

MAX VALUE :
MIN VALUE :
RESOLUTION :
ACCURACY :
MSB :
LSB :
FULLSCALE :

FIELD NAME	BIT NO.	DESCRIPTION
	-00-	
	-01-	
	-02-	
	-03-	
	-04-	
	-05-	
	-06-	
	-07-	
	-09-	
	-10-	
	-11-	
	-12-	
	-13-	
	-14-	
	-15-	

REMARKS:

(See notes to tables 80-I and 80-II)

Table 80-11. Presentation Format, Double Precision

DOC. NO. REV.
DATE
SHEET 1 OF

WORD NAME :

WORD ID	:	MAX VALUE	:
SOURCE(S)	:	MIN VALUE	:
DEST(S)	:	RESOLUTION	:
COMP RATE	:	ACCURACY	:
XMIT RATE	:	MSB	:
SIGNAL TYPE	:	LSB	:
UNITS	:	FULLSCALE	:

FIELD NAME	BIT NO.	DESCRIPTION
	MSW -00-	
	-01-	
	-02-	
	-03-	
	-04-	
	-05-	
	-06-	
	-07-	
	-08-	
	-09-	
	-10-	
	-11-	
	-12-	
	-13-	
	-14-	
	-15-	
	LSW -00-	
	-01-	
	-02-	
	-03-	
	-04-	
	-05-	
	-06-	
	-07-	
	-08-	
	-09-	
	-10-	
	-11-	
	-12-	
	-13-	
	-14-	
	-15-	

REMARKS:

(See notes to tables 80-I and 80-II)

Notes to tables 80-I and 80-II:

Tables 80-I and 80-II are the skeleton ICD sheets. Figures 80-I and 80-2 provide the detailed layout for the ICD presentation sheets. The definition of each entry is as follows:

DOC. NO.: The interface control document number.

REV.: The revision symbol for this sheet.

DATE: The calendar date of the latest revision to this sheet.

SHEET 1 OF ## : This sheet count allows multiple sheets.

WORD NAME: The formal name selected for this word as described in paragraph 80.2.4, Naming.

WORD ID: Code identifying the message of which this word is part. The WORD ID is constructed as follows:

XXXXSX-WWSY-W# or XXXXSX-YYYYSY-W#/W#

where:

XXXX = Transmitting terminal name (see table 80-111 for examples). Transmitting terminal has T/R bit= 1.

SX = Transmitting terminal 1553 subaddress from which the word originated.

YYYY = Receiving terminal name (see table 80-III for examples). Receiving terminal has T/R bit = O.

SY = Receiving terminal 1553 subaddress to which the word is addressed.

W# = Word number of single word.

W#/W# = Word numbers of double word.

(XXXXSX-YYYYSY is the message ID).

The rules for WORD ID construction are:

Entries in XXXX and YWY are four characters left-justified with trailing blanks (such as “INS1”, “SMS “, “MC “). In the broadcast mode of operation, WYY is “ALL".

Entries in SX and SY are two numeric characters with a range of 00-31 or the characters BC, M0, or M1. The latter characters are used in conjunction with the bus controller and the transmission of MIL-STD-1553 mode codes. M0 represents the transmission of 00000 in the subaddress/mode field of the MIL-STD-1553 command word; M1 represents the transmissionof11111 in that field. When M0 and M1 are used as either SX or SY, the numeric entry, used in conjunction with the receive/transmit terminal, will indicate the MIL-STD-1553 mode code (the data word count/mode code field of the MIL-STD-1553 command word). For example, the word ID INS 03-BC1 M0-MCCW indicates that a Mode Command Without Data Word, (MCCW), is being commanded by the bus controller (BC1), using 00000 (M0) as the subaddress/mode, to the INS. The mode code being transmitted is Initiate Self Test (03). (See Tables 80-LXVI through 80-LXVIII for the relationship between mode codes and word/message ID formats).

Notes to tables 80-I and 80-II; (Continued)

Entries in W# are two numeric characters with a range of 01-32. The field W#/W# is a five-character field. If the word is single precision, the last three characters will be blank. In the case of command words, this field will contain:

RCW	-	BC-to-RTTransfer
TCW	-	RT-to-BC Transfer
RTCW	-	RT-to-RT Transfer
MCCW	-	Mode Command Without Data Word
MCCDT	-	Mode Command With Data Word (Transmit)
MCCDR	-	Mode Command With Data Word (Receive)
BCCW	-	BC-to-RT Transfer, Broadcast
BCCRT	-	RT-to-RT Transfer, Broadcast
BCMC	-	Mode Command Without Data Word, Broadest
BCMCD	-	Mode Command With Data Word, Broadcast

In the case of status words, this field will contain:

TSW	- Transmit Status Word
RSW	- Receive Status Word

Examples of typical WORD ID's are shown in table 80-IV.

SOURCE(S): Name(s) of the subsystem(s) originating the word, usually abbreviated or an acronym. When a word is modified by a subsystem, that subsystem becomes the originating source. Source information is used to allow tracking of data from the originating source to all destinations.

DEST(S): Name(s) of the subsystem(s) that will receive the word, usually abbreviated or an acronym. Destination information is used to allow tracking of data back to the originating source and to other destinations.

COMP RATE: The rate in times per second (Hz) that the data is computed.

XMIT RATE: The nominal rate in times per second (Hz) that the message is transmitted.

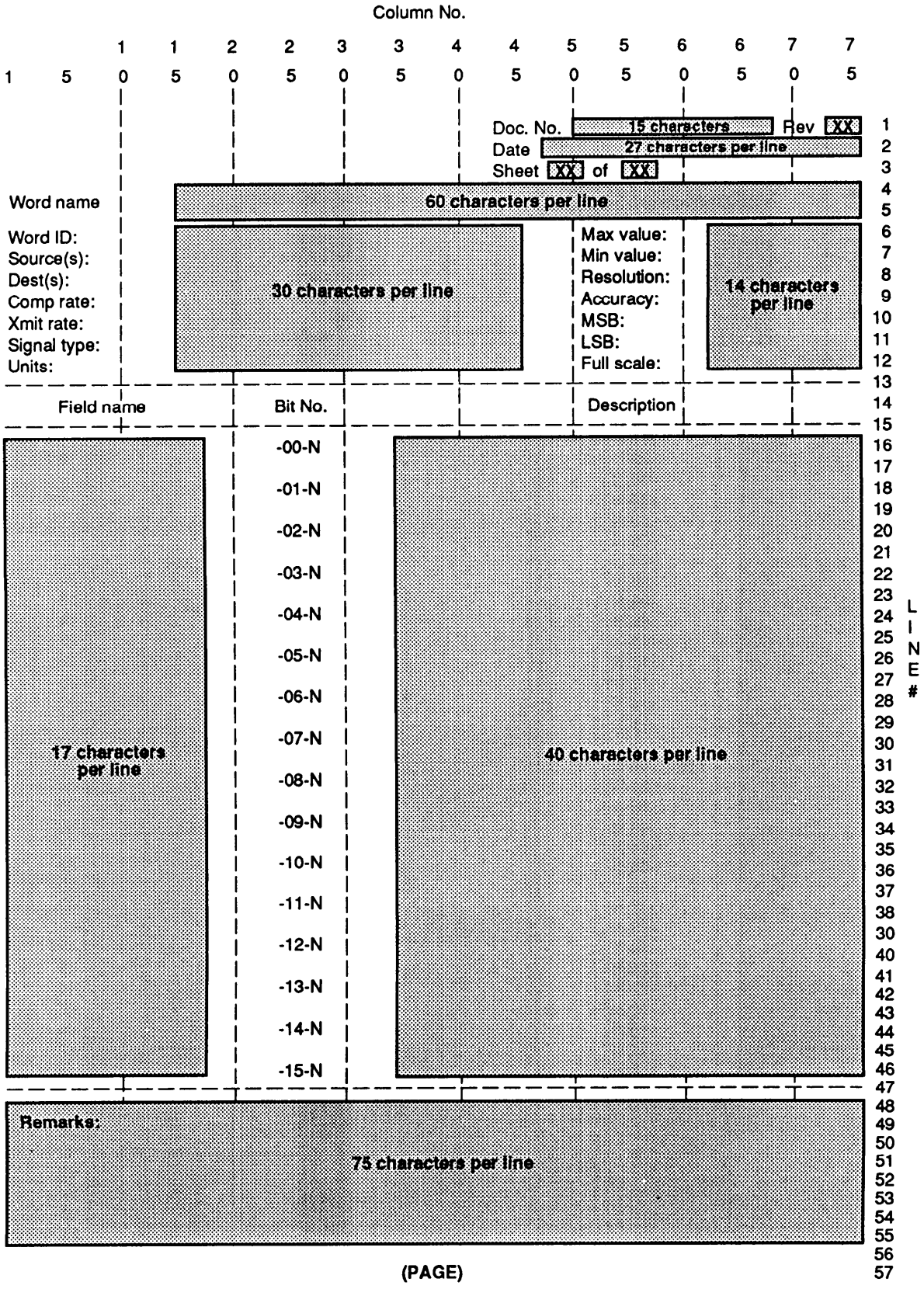


Figure 80-1. ICD Presentation Sheet, Single Word

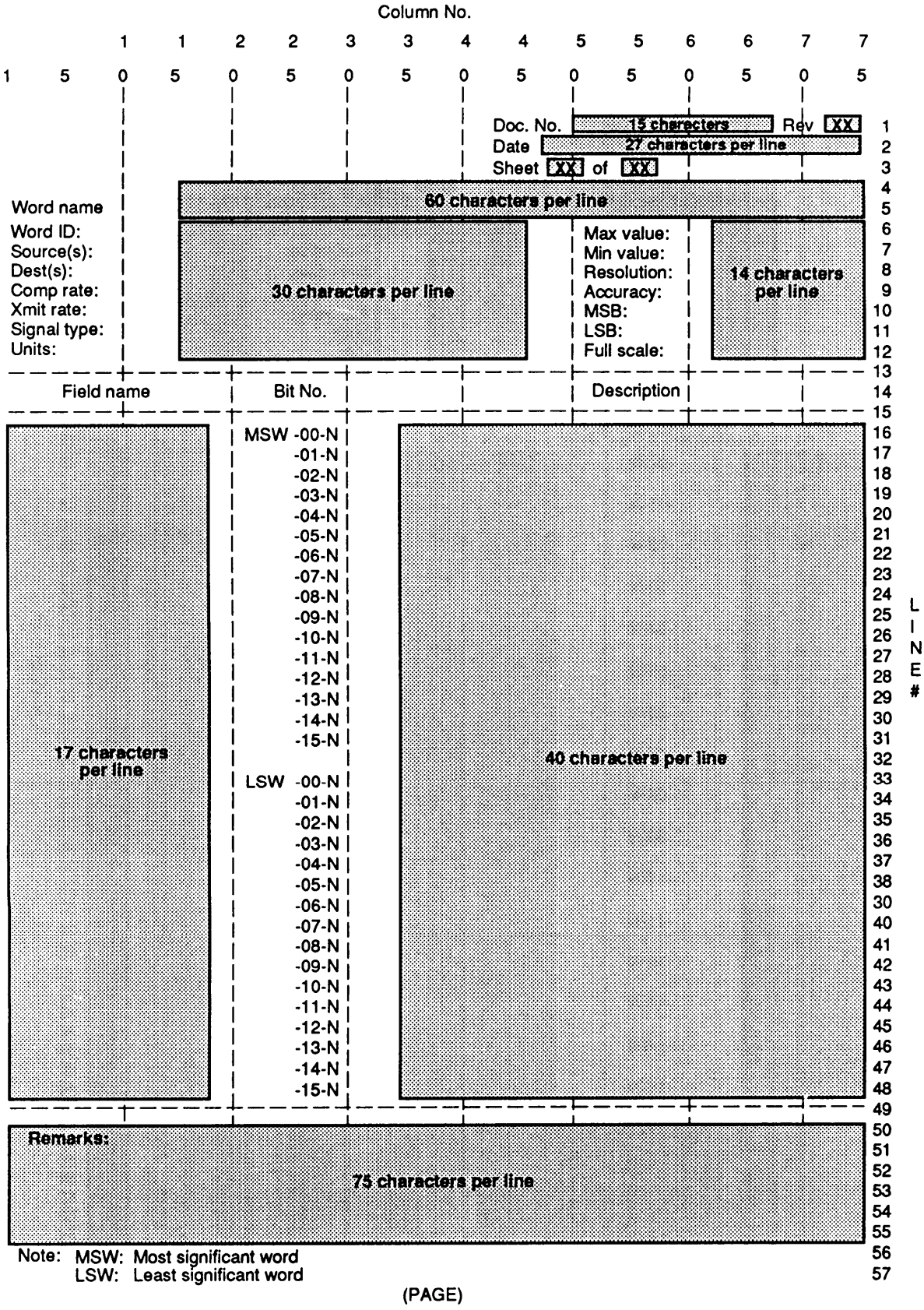


Figure 80-2. ICD Presentation Sheet, Double Precision

Table 80-111. Standard Terminal Acronyms for Use in Word ID's

Acroynm	
ADC	Air Data Computer
ADF	Automatic Direction Finder
ADI	Attitude Direction Indicator
AHRS	Attitude Heading Reference System
AIU	Avionics Interface Unit
ALS	Automatic Landing System
ASI	Airspeed Indicator
ATHS	Airborne Target Handoff System
AUXS	Auxiliary Sensor
BBC	Backup Bus Controller
BC	Bus Controller
BIU	Bus Interface Unit
CAS	Control Actuation System
CDU	Control Display Unit
CNI	Communication, Navigation, Identification
CPU	Central Processing Unit
DL	Data Link
DP	Display Processor
DME	Distance Measuring Equipment
DNC	Doppler Navigation Computer
DNS	Doppler Navigation System
DTU	Data Transfer Unit
DVS	Doppler Velocity Sensor
ECM	Electronic Countermeasures
EHF	Extra High Frequency Radio
FCC	Fire Control Computer
FCS	Fire Control System
FIR	Flight Incident Recorder
FLC	Flight Control
FLI	Forward Looking Infared
GPS	Global Positioning System
GS	Glideslope
HAS	Hover Augmentation System
HF	High Frequency Radio
HMD	Helmet Mounted Display
HSI	Horizontal Situation Indicator
HUD	Head-Up Display
HV	Host Vehicle
ICP	Integrated Control Panel
ICS	Intercommunication System
ICU	Ignition Control Unit
IFF	Identification, Friend or Foe
IL	Instrument Landing System
IMU	Inertial Measurement Unit
INS	Inertial Navigation System
INU	Inertial Navigation Unit
JCU	JTIDS Control Unit

Acronym	
KY	Crypto Unit
LOC	Localizer
MB	Marker Beacon
MC	Mission Computer
MFD	Multi-Function Display
MIU	Missile Interface Unit
MMR	Multi-Mode Receiver
MMS	Mast Mounted Sight
MPD	Multi-Purpose Display
NPU	Navigation Processing Unit
OM	Omega
PCU	Power Control Unit
PLU	PLRS Interface Unit
PNVS	Pilot Night Vision System
RAD	Radar Altimeter
RDR	Radar
RIU	Radar Interface Unit
RTR	Remote Terminal
RTU	Remote Terminal Unit
RWR	Radar Warning Receiver
SAS	Stability Augmentation System
SCU	Signal Converter Unit
SG	Symbol Generator
SHVI	Standard HV Interface
SLU	Stores Interface Unit
SL	Stores Logic
SMS	Stores Management System
SS	Stores Station
SSHV	Slave SHVI
TADS	Target Acquisition Designation System
TCM	TERCOM
TCN	TACAN
TCS	Tactical Camera System
TM	Telemetry
TSC	Time Sync Controller
UHF	Ultra High Frequency Radio
VDI	Vertical Direction Indicator
VHF	Very High Frequency Radio
VOR	VHF Omni-Directional Range Radio
VSI	Vertical Situation Indicator
WCS	Weapon Control System
WIU	Weapon Interface Unit
WXR	Weather Radar

Table 80-IV. Word ID Examples

WORD ID	MIL-STD-1553 TRANSFER TYPE	DESCRIPTION
INS 03-FLIR02-07	RT-to-RT	INS is transmitting word number 07 from subaddress 03 to subaddress 02 of FLIR.
AHRS03-MC BC-07	RT-to-BC	AHRS is transmitting word number 07 from subaddress 03 to the MC (which is the bus controller).
BC1 BC-HUD205-07/08	BC-to-RT	BC1 (the bus controller) is transmitting word number 07 and 08 to subaddress 05 of HUD2.
NPU BC-ALL 04-15	Broadcast	NPU (the bus controller) is transmitting word number 15 to subaddress 04 in the broadcast mode of operation.

Notes to table 80-IV:

SIGNALTYPE : 2's complement-A representation of a signed value where the negative codes are generated by adding one to the complement of the number. The use of 2's complement in a digital computer facilitates the subtraction process.

Unsigned numeric—A binary representation of an unsigned value. The value maybe an integer or may have a fractional component.

Discret-A single binary bit whose state of one or zero has a specified meaning.

Coded-A grouping of bits in which the pattern of ones and zeros has a specified meaning.

Binary Coded Decimal (BCD)—The natural binary coded decimal (NBCD) or four-bit (8421) code is a special BCD form. The NBCD code allows only 10 (O-9) valid states, with the values 10-15 being invalid.

ASCII—A seven-bit binary code representing alpha and numeric characters.

ASCll-8-Extended ASCII using eight bits for additional character representations.

UNITS : The engineering units of the transmitted signal.

Note: Some words may be unitless.

MAX VALUE : The maximum value that the signal, as supplied by the subsystem, can attain. MAX VALUE must be less than or equal to FULLSCALE.*

MIN VALUE	:	The minimum value that the signal, as supplied by the subsystem, can attain.*
RESOLUTION	:	Resolution is defined as the minimum detectable change in value of the signal, as supplied by the subsystem.*
ACCURACY	:	The accuracy of the signal as supplied by the subsystem.*
MSB	:	The value of the most significant bit of the word and/or field.*
LSB	:	The value of the least significant bit of the word and/or field.*
FULLSCALE	:	The maximum value the data field can attain (two times MSB minus LSB).*
FIELD NAME	:	The formal name selected for a signal describing a bit, field, or single or double precision word.
BIT NO	:	BIT NO. is as defined in paragraph 80.2.2.1.
DESCRIPTION	:	A functional description of the signal.
MSW	:	Most significant word of a double precision signal.
LSW	:	Least significant word of a double precision signal.
REMARKS	:	(Optional) Additional comments, if needed, pertaining to the word.
PAGE	:	Page No. of the ICD.

l Set to N/A when data word is divided into coded fields.

80.2.2.1 Data Word/Bit Designation

Figure 80-3 shows the horizontal presentation of the 16-bit data field of the data word defined in MIL-STD-1553. Thedatafield bits are numbered 00through 15, Ieft to right, with bit 00 designated as the most significant bit (MSB) and bit 15 designated as the least significant bit (LSB). In conformance to the requirements of MIL-STD-1553, the most significant bit (bit 00) is transmitted first on the data bus.

The MSB and LSB designations indicated here refer to the relative weighting of the entire 16 bits in a 2's complement representation of signal value. The MSB and LSB designations will also be employed to define the most significant and least significant bits of parameters requiring less than or more than 16 bits. There can also be more than one signal value in a data word, thus requiring multiple MSB'S and LSB's within the data field. Discrete bits and binary codes are also used to represent characters or modes. Throughout this document the term "data word" will be used in reference to this 16-bit data field.

80.2.2.2 Signal Coding and Placement

Several coding techniques are provided because of the variety of signal types that must be accommodated in a data word format. The following are the typical coding conventions and the presentation notations:

a. 2's complement	S (Sign), MSB, LSB, and N (data bits)
b. Unsigned numeric	MSB, LSB, and N (data bits)
c. Discrete bit	D
d. Coded bits	MSB, LSB, and C (data bits)
e. Binary coded decimal (NBCD, 8421)	MSB, LSB, and B (data bits)
f. ASCII alphanumeric codes	MSB, LSB, and A (data bits)
g. Validity bit	v
h. Unused or reserved bits, logic O	0
i. Logic 1	1
j. Floating point	MSB, LSB, Sign, & M (Mantissa) (data bits) MSB, LSB, Sign, & E (Exponent) (data bits)

Figure 80-4 shows some examples of typical word formats employing the above digital representations. The following general rules apply to all word structures:

a. The MSB shall always be transmitted first, in accordance with MIL-STD-1553.

b. All spare or unused bfis shall be transmitted as logic O's, in accordance with MIL-STD-1553.

c. In the event that multiple precision quantities (information accuracy or resolution requiring more than 16 bits) are transmitted, the most significant bits shall retransmitted first, followed by the word(s) containing the less significant bits in descending numerical order, in accordance with MIL-STD-1553.

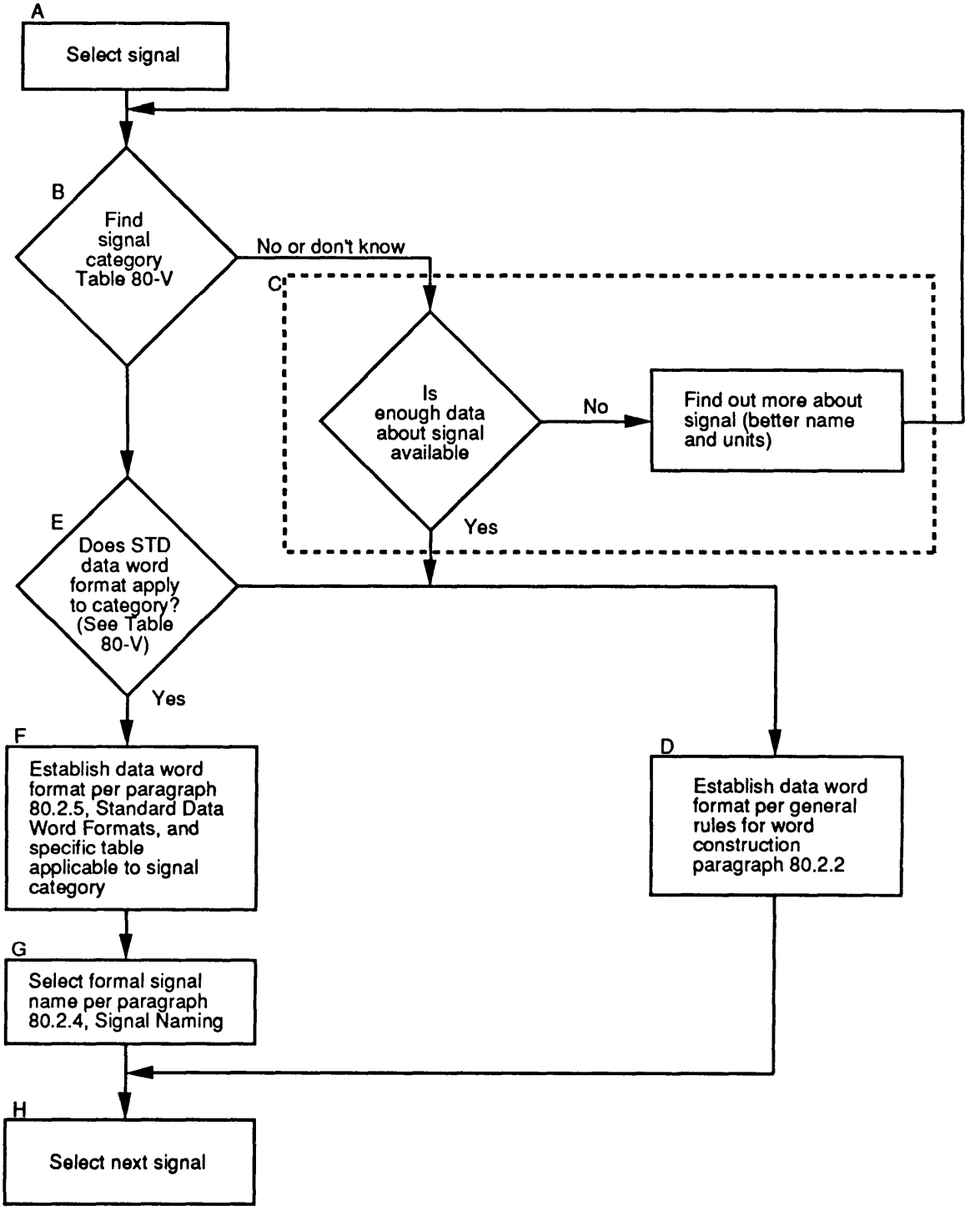


Figure 80-5. Establishing a Data Word Format

b. Refer to table 80-V, Index of Typical Signal Categories, and find the category that applies to the signal. In the example signal, present position latitude, the keyword is latitude. Latitude is an angular measurement; therefore, the signal falls in the "angular" category. Note that table 80-V is divided into categories for signals with engineering units and categories of unitless signals. It will be easier to find the appropriate category if it is known whether the signal is unitless or which units apply. The use of keywords and modifiers associated with each category may aid in identifying the correct category.

   After the signal category is determined, go to Step e.

   If the category cannot be determined or there is uncertainty whether the signal really fits in a given category, go to Step c.

c. If there is still uncertainty about the signal category, get a better definition of the signal. Determine more descriptive or functional details about the signal, including the source, destination, name, and engineering units (if any). Then go back to Step b. Otherwise, go to Step d.

d. If the signal definitely does not fall into any of the listed categories, refer to paragraph 80.2.2, General Rules for MIL-STD-1553 Word Construction, for general guidance in establishing the data word format for this signal.

e. Refer to Table 80-Vl,Standard Data Word Format Index. Using the category identified in Step b (from Table 80-V), select the appropriate units and precision, and note the standard data word format table number. Those formats indicated as double precision maybe used as eithera single or double precision word, based on the requirements of the particular application.

   For the example signal, present position latitude, the correct category is "Angular". In the standard data word format column of the table we find and note for later use the reference to table 80-IX. Find the category of your signal in table 80-VI and note the tables referenced in the standard data word format column.

f. Refer to paragraph 80.2.5, Standard Data Word Formats, and the applicable tables (noted in Step e). Construct the data word format and complete the ICD data sheet(s) for this signal.

g. A necessary part of data word format development is the selection of a formal signal name for each signal. Refer to paragraph 80.2.4, Naming, to select the formal signal name. Proceed to Step h.

h. Select next signal and start the process at Step b.

80.2.4 **Naming**

A necessary part of data word format development is the selection of a formal signal name for each signal. A naming convention will make signals more easily traceable within an integrated system as well as across various systems.

The basic principle for naming signals consistently is placing the most important word (keyword) first, followed by modifiers. The keyword is the word most closely related to the category or engineering units (if any) of the signal. The keyword may be the same as the signal category. Appropriate modifiers should be added as required to create a unique signal name for each data word within the system. For example, "latitude, present position, INS."

Table 80-V presents typical signal names by category. Within each category is a list of keywords associated with that category and some typical modifiers associated with those keywords. This table should be helpful in selecting a formal signal name by using the following procedure:

Table 80-V. Index of Typical Signal Categories (Sheet 1 of 6)

Acceleration Tables 80-VII and 80-VIII		Angular Table 80-1X		Angular Acceleration Table 80-X		Angular Velocity Table 80-XI		ASCII Data Table 80-XII	
Keyword	Typical Modifiers	Keyword	Typical Modifiers	Keyword	Typical Modifiers	Keyword	Typical Modifiers	Keyword	Typical Modifiers
Acceleration	Down East Lateral Longitudinal Normal North Target, X Target, Y Target, Z Turret X Y Z	Angle	AOA (angle-of-attack) AOA, error AOA, true Drift Ground track Ground track, present Pitch Roll Sideslip Steering Tilt Wander	Acceleration	Down East North Pitch Roll Yaw	Gyro bias	Correction X Correction Y Correction Z	Bar	Horizontal Vertical
								Character	Left Middle Right
						Rate	Angular Azimuth Deflection Elevation Pitch Rotation Yaw	Display	Alpha Border Branch Character Control Data Intensity Miscellaneous Numeric Position Radar Symbol Window
		Azimuth	Cross hair Error Platform Relative Rel. to steerpoint Rel. to Nth waypoint Rel. to Nth markpoint Symbol						
								Symbol	Control Identification Internal Reference
		Bearing	(Same as azimuth)						
		Course	Desired Ground track Magnetic, computed Magnetic, inserted						
		Elevation	Bullet Circle Command angle Error LOS (loss-of-signal) Position Reference, aircraft Scale Target						
		Heading	Error Magnetic, inserted Magnetic, present True True, inserted True, present						
		Latitude	Markpoint Nth markpoint Nth waypoint Present pos., inserted Waypoint pos., inserted						
		Longitude	(Same as latitude)						
		Variation	Magnetic, computed Magnetic, inserted						

Table 80-V. Index of Typical Signal Categories (Sheet 2 of 6)

BCD Data Table 80-XIII		Convergence Factor Table 80-XIV		Cosine, Sine Table 80-XV		Counts Tables 80-XVI and 80-XVII	
Keyword	Typical Modifiers	Keyword	Typical Modifiers	Keyword	Typical Modifiers	Keyword	Typical Modifiers
Channel	Select	Convergence factor	Inserted Present, in use	Cosine	Direction a. CXX (ref. platform to earth CXY coordinate system) CXZ	Counts	Track control, RN Track control, n
IFF	Code Control Interrogator				b. DIRXL (ref. A/C body DIRYL coordinate system) DIRZL	Date	Julian Year
ILS	Channel Mode				c. DIRCOSX (same as b) DIRCOSY DIRCOSZ	Frames	Film recording data
Radio	Select Status Test				Heading Pitch Roll	Pulses	Ripple
Receiver	Channel Command Frequency Tune			Sine	Heading Pitch Roll	Revolutions	Revolutions per minute Rotor speed No. n
RF	Channel Disposition Level Transmit					Rounds	Remaining
TACAN	Channel Mode					Words	Instrumentation port data
UHF/VHF	Channel Mode						
VOR	Channel Mode						

Table 80-V. Index of Typical Signal Categories (Sheet 3 of 6)

Data Validity Table 80-XVIII and 80-XIX		Deviation Table 80-XX		Cosine, Sine Table 80-XV		Distance Tables 80-XXI through 80-XXV	
Keyword	Typical Modifiers	Keyword	Typical Modifiers	Keyword	Typical Modifiers	Keyword	Typical Modifiers
Error protection	(None)	Deviation	Glideslope Localizer	Altitude	Above fixpoint Barometric Barometric reference Desired Electronic Altimeter Helo (Helicopter) Inertial Pressure Radar Sonobuoy launch Store System Target	Rate position	Acquisition cursor
Checksum	Bits Word					Separation	Impact
Validity	Bit Data Discrete					Wingspan	(None)
				Azimuth	Cursor Deviation steering Steering dot	X	Cursor connection Cursor total Delta Display delta Display position Display - translate Helo position Helo position at initialization Ownship position Pointer position Position Position, fly-to-point Sonobuoy position Symbol position
				Circle	Display		
				Distance	To Nth waypoint/markpoint To steerpoint	Y	(Same as X)
				Easting	Inserted position Inserted waypoint Nth waypoint/markpoint MGRS Present position MGRS	Z	Cursor total Position
				Elevation	(Same as azimuth)		
				Error	Allowable steering Crosstrack Position east Position north		
				Height	Above target (HAT)		
				Northing	(Same as easting)		
				Range	Aircraft symbol Contact Ground track, incremental Manual Maximum Minimum Pull up Radar Slant TACAN Tactical X, relative target Y, relative target Z, relative target		

Table 80-V. Index of Typical Signal Categories (Sheet 4 of 6)

Flow Tables 80-XXVI and 80-XXVII		Frequency Tables 80-XXVIII through 80-XXX		Mass Tables 80-XXXI and 80-XXXII		MGRS Table 80-XXXIII		Percent Table 80-XXXIV	
Keyword	Typical Modifiers	Keyword	Typical Modifiers	Keyword	Typical Modifiers	Keyword	Typical Modifiers	Keyword	Typical Modifiers
Fuel	(None)	Frequency	ADF-n HF-n UHF-n VHF-n	Mass	Aircraft Fuel Ordnance Payload	MGRS	Area Datum Grid zone Easting Northing Spheroid 100,000 meter Grid square Ellipsoid	Percent	(None)
Oil	(None)								

Table 80-V. Index of Typical Signal Categories (Sheet 5 of 6)

Pressure Tables 80-XXXV and 80-XXXVI		Ratio Table 80-XXXVII		Temperature Table 80-XXXVIII		Time Tables 80-XXXIX through 80-XLIII	
Keyword	Typical Modifiers	Keyword	Typical Modifiers	Keyword	Typical Modifiers	Keyword	Typical Modifiers
Differential	Pressure altitude	Ratio	Air density Pressure	Temperature	Celsius Engine inlet Exhaust gas	Calendar	(None)
Discharge	Compressor turbine				Fuel inlet Outside air	Clock	Kalman
Oil	Engine				Total True freestream air	Time	Align Almanac reference Coordinated universal Greenwich mean Of day Sonobuoy, last correct Sonobuoy launch Symbol Tag
Impact	Indicated						
Static	Indicated					Time to	Destination Go Nth waypoint/markpoint Steerpoint
						Pulse	Width Repetition interval

Table 80-V. Index of Typical Signal Categories (Sheet 6 of 6)

Torque Table 80-XLIV		Vector word Table 80-XLV		Velocity Tables 80-XLVI through 80-L		Voltage Table 80-LI	
Keyword	Typical Modifiers	Keyword	Typical Modifiers	Keyword	Typical Modifiers	Keyword	Typical Modifiers
Engine	(None)	Asynchon-ous	Message demand Action demand	Airspeed	Calibrated Indicated True	Voltage	Display intensity Fore/aft cursor deflection Left/right cursor deflection Stick X deflection Stick Y deflection
Shaft	(None)			Groundspeed	Predicted Present Tail warning system		
				Mach	Number		
				Range rate	None		
				Speed	Bias Desired Ground Helo Helo wind Ownship Symbol True Water		
				Velocity	Correction X Correction Y Doppler drift Doppler heading Doppler vertical Down Drift East Heading North Vertical Wind X X, relative target Y Y, relative target Z Z, relative target		

Table 80-VI. Standard Data Word Format Index (Sheet 1 of 2)

Category	Units	Word(s)/ Precision	Table No.
Acceleration	Metres/Second/Second	Double	80-VII
	Feet/Second/Second	Single	80-VIII
Angular	Semicircles	Double	80-IX
Angular Acceleration	Semicircles/Second/Second	Single	80-X
Angular Velocity	Semicircles/Second	Double	80-XI
ASCII Data	Unitless (Character)	One	80-XII
BCD Data	Unitless (Channel Select)	One	80-XIII
Convergence Factor	Unitless	Single	80-XIV
Cosine/Sine	Unitless	Double	80-XV
Counts	Unitless (Signed)	Single	80-XVI
	Unitless (Unsigned)	Single	80-XVII
Data Validity	Unitless (Checksum)	Single	80-XVIII
	Unitless (Error Protection)	One	80-XIX
Deviation	Difference in Depth of Modulation (DDM)	Single	80-XX
Distance	Metres	Double	80-XXI
	Feet	Double	80-XXII
	Kilometres	Double	80-XXIII
	Nautical Miles (Low Range)	Single	80-XXIV
	Nautical Miles (High Range)	Double	80-XXIV
Flow	Kilograms/Hour (Low Range)	Single	80-XXVI
	Kilograms/Minute (High Range)	Single	80-XXVII
Frequency	Hertz	Four	80-XXVIII
	Kilohertz (ADF)	One	80-XXIX
	Megahertz (VHF/UHF)	One	80-XXX
Mass	Kilograms (Low Range)	Single	80-XXXI
	Kilograms (High Range)	Single	80-XXXII
MGRS	Unitless	Five	80-XXXIII
Percent	Unitless	Single	80-XXXIV
Pressure	Kilopascals	Double	80-XXXV
	Inches of Mercury	Single	80-XXXVI

Table 80-VI. Standard Data Word Format Index (Sheet 2 of 2)

Category	Units	Word(s)/ Precision	Table No.
Ratio	Unitless	Single	80-XXXVII
Temperature	Celsius	Single	80-XXXVIII
Time	Month, Day, Hour, Minute, Second	Three	80-XXXIX
	Microseconds (Time Tag)	Double	80-XL
	Seconds (Time To)	Single	80-XLI
	Microseconds (PRI)	Single	80-XLII
	Nanoseconds (Pulse Width)	Single	80-XLIII
Torque	Newton-Metres	Double	80-XLIV
Vector Word	Unitless	Single	80-XLV
Velocity	Metres/Second	Double	80-XLVI
	Feet/Second	Double	80-XLVII
	Kilometres/Hour	Single	80-XLVIII
	Knots	Single	80-XLIX
	Mach Number	Single	80-L
Voltage	volts	Double	80-LI

a. Find the appropriate category for your signal. For our example signal, present position latitude, the category is “Angular”.

b. Determine if your signal’s keyword is listed. For the example signal, present position latitude, the keyword is “latitude”.

c. If your signal’s keyword is not listed under the appropriate category, consider using the category name as your signal’s keyword. If the category name is an inappropriate keyword for your signal, choose the most meaningful word in the name as the keyword.

d. Define your signal’s formal name by placing the keyword first, followed by the remaining words (modifiers). Table 80-V also lists some typical modifiers for common keywords. The formal name for our example signal would therefore be ”latitude, present position.”

e. Return to paragraph 80.2.3 to complete data word format definition.

80.2.5 Standard Data Word Formats

This paragraph presents the standard data word formats, and provides the user guidance necessary to fit real-life signals into the standard data word formats. An example signal is used to illustrate the application of the standard data word formats to real-life signals. The derivation of the example data word is presented in the following paragraphs, and the completed data word format is presented in figure 80-6. Figure 80-7 depicts the standard vehicle fixed-axis coordinate system. Other coordinate systems referenced in the ICD should be similarly illustrated.

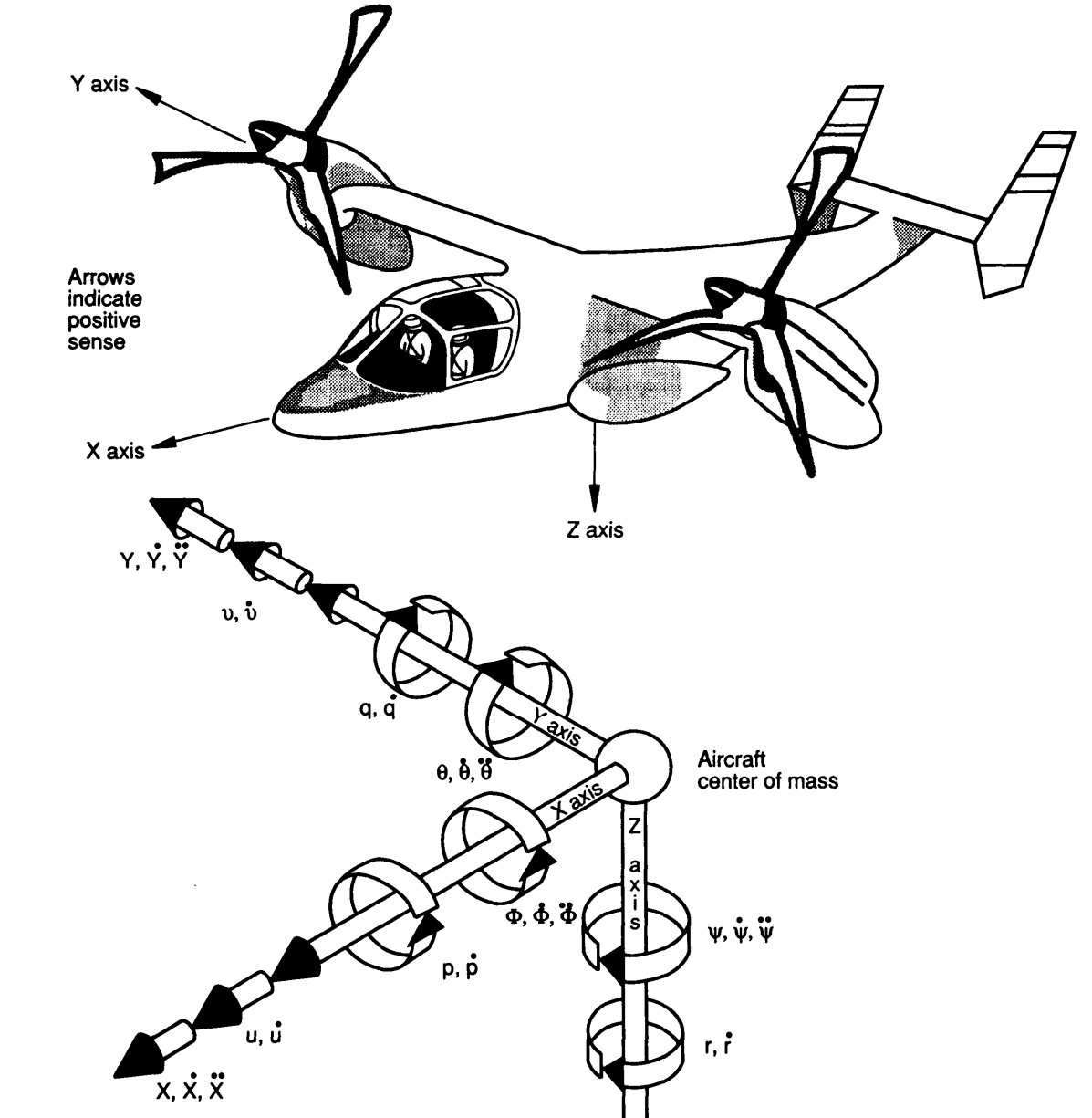
DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME: Latitude, Present Position, INS

WORD ID	: INS 03-FCC 12-04/05	MAX VALUE	: 0.5
SOURCE(S)	: INS	MIN VALUE	: -0.5
DEST(S)	: FCC	RESOLUTION	: 0.0000000038
COMP RATE	: 8	ACCURACY	: 0.0000000152
XMIT RATE	: 8	MSB	: 0.5
SIGNAL TYPE	: 2's complement	LSB	: 0.0000000005
UNITS	: Semicircle	FULLSCALE	: 1

FIELD NAME	BIT NO.	DESCRIPTION
Latitude	MSW-00-N	Sign
	-01-N	MSB
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	
	LSW -00-N	
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	RESOLUTION :0.0000000038
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: Positive Sense: Plus is North
* -Application Dependent



	Velocities	Position/ angle	Acceleration
Forward	$\dot{X}$, u	X	$\ddot{X}$, $\dot{u}$
Side	$\dot{Y}$, υ	Y	$\ddot{Y}$, $\dot{\upsilon}$
Vertical	$\dot{Z}$, w	Z	$\ddot{Z}$, $\dot{w}$
Roll	p, $\dot{\Phi}$	Φ	$\dot{p}$, $\ddot{\Phi}$
Pitch	q, $\dot{\theta}$	θ	$\dot{q}$, $\ddot{\theta}$
Yaw	r, $\dot{\psi}$	ψ	$\dot{r}$, $\ddot{\psi}$

Figure 80-7. Vehicle Fixed-Axis Coordinate System

Table 80-VI is an index that keys the user into the various standard data word formats. The standard data word formats are presented in tables 80-VII through 80-LI. Having established the category of your signal (by following the steps outlined in paragraph 80.2.3), refer to the appropriate standard data word format(s), as indexed in table 80-VI, and to the following example for guidance.

An effective means of guiding the user in establishing data word formats for his signals is by example. We have been using atypical signal, "latitude, present position," as our example. The data word format for this signal is derived as follows. It is necessary to have certain information about the signal before the data word format can be defined. For signals that have engineering units, the minimum necessary information is as follows:

a. The formal word name (established in paragraph 80.2.4)

b. The engineering units

c. The range (maximum and minimum) of signal value

d. The accuracy required

The following information is used in our example:

WORD NAME : LATITUDE
UNITS : DEGREES
RANGE : ±9O DEGREES (POSITIVE IS NORTH)
ACCURACY : 0.00000273 DEGREES

Refer to the index in table 80-VI. We established that the category of our example signal is "angular." The index refers us to table 80-IX for angular category, double precision. Proceed as follows to decide whether data word will be single or double precision:

a. Is RANGE of signal covered by MAX VALUE and MIN VALUE of standard data word format? If not, define data word format for the signal by using the General Rules for Word Construction, paragraph 80.2.2, and the standard data word formats as examples.

   The RANGE of our signal is ±9O DEGREES. We see that the UNITS of the standard data word format are SEMICIRCLES (1 semicircle = 1 pi radian), so we must convert all signal parameters from DEGREES to SEMICIRCLES. To convert, divide DEGREES by 180. The signal RANGE (±90 DEGREES) becomes ±0.5 SEMICIRCLES, and is within the MAX VALUE (+1) and MIN VALUE (-1) of the standard format.

b. Can the required signal ACCURACY be transmitted using the single precision standard format? If yes, proceed; if no, can double precision standard format accommodate ACCURACY? If yes, proceed; if no, refer to paragraph 80.2.2, General Rules for MIL-STD-1553 Word Construction, and define data word format for the signal using the standard data word formats as examples.

   The example signal's required ACCURACY is 0.00000273 DEGREES, or, after conversion, 0.0000000152 SEMICIRCLES. The LSB value of the first word of the standard format is 2^{-15} (i.e., 0.0000305176) SEMICIRCLES. The format with accuracy of 0.0000305176 cannot accommodate the 0.0000000152 accuracy required. The LSB value of the double precision standard format is 2^{-31} (i.e., 0.000000000466) SEMICIRCLES, which is sufficient to accommodate the 0.0000000152 signal accuracy.

By the preceding steps it was determined that the appropriate standard data word format for the example signal is Table 80-IX, for angular category, double precision. Now use a blank ICD presentation format sheet (see Tables 80-I and 80-II for single and double precision formats, respectively) as a worksheet and to

document the data word format that will be derived. We need to use the ICD format of table 80-II because our example data word will be double precision. The completed ICD presentation for our example signal's data word format is shown in figure 80-6. The derivation of each entry which is not application dependent is as follows:

a. DOC. NO. : Application dependent.

b. REV. : Application dependent.

c. DATE : Application dependent.

d. SHEET 1 OF ## : 1.

e. WORD NAME : LATITUDE, PRESENT POSITION, INS (formal signal name, selected in paragraph 80.2.4).

f. WORD ID : INS 03-FCC 12-04/05

g. SOURCE(S) : INS (source of example signal).

h. DEST(S) : FCC (destination of example signal).

i. COMP RATE : 8 Hertz.

j. XMIT RATE : 8 Hertz.

k. SIGNAL TYPE : The encoding format of the digital data is 2's complement notation, as specified in the standard format.

l. UNITS : Semicircles (as specified in standard data word format).

m. MAX VALUE : The maximum value of our signal is +0.5 semicircles (converted from +90 degrees)

n. MIN VALUE : The minimum value of our signal is -0.5 semicircles (converted from -90 degrees)

o. RESOLUTION : 0.0000000038 semicircles (determination of RESOLUTION is application dependent).

p. ACCURACY : 0.0000000152 semicircles (the signal accuracy).

q. MSB : 0.5 semicircles (MSB value as specified in standard data word format).

r. LSB : 0.0000000005 semicircles (LSB value as specified in standard data word format).

s. FULLSCALE : 1 semicircle (as specified in standard data word format).

t. FIELD NAME : Latitude (application dependent).

u. DESCRIPTION : Application dependent.

v. MSW : This defines the bit assignments for the first data word. This is a signed quantity; therefore, BIT-00 is the Sign. BIT-01 is the MSB (MSB of data is transmitted first per MIL-STD-1553B). BIT-02 through BIT-15 are data bits.

w. LSW : This defines the bit assignments for the second dataword. BIT-00 through BIT-09 are data bits. BIT-15 is the LSB. BIT-11 through BIT-15 are not used.

x. REMARKS : POSITIVE SENSE: PLUS IS NORTH (statement that data is transmitted as plus equals north latitude).

y. PAGE NO. : Application dependent.

(This page intentionally left blank.)

Table 80-VII. Acceleration Category, Metres/Second/Second, Double Precision

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Acceleration

WORD ID	: *	MAX VALUE	:
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 512
SIGNAL TYPE	: 2's complement	LSB	: 0.0000004768
UNITS	: Metres/Second/Second	FULLSCALE	: 1,024

FIELD NAME		BIT NO.	DESCRIPTION
Acceleration	MSW	-00-S	Sign
		-01-N	MSB
		-02-N	
		-03-N	
		-04-N	
		-05-N	
		-06-N	
		-07-N	
		-08-N	
		-09-N	
		-10-N	
		-11-N	
		-12-N	
		-13-N	
		-14-N	
		-15-N	Notes 1, 2
	LSW	-00-N	
		-01-N	
		-02-N	
		-03-N	
		-04-N	
		-05-N	
		-06-N	
		-07-N	
		-08-N	
		-09-N	
		-10-N	
		-11-N	
		-12-N	
		-13-N	
		-14-N	
		-15-N	LSB

REMARKS: * - Application Dependent

Note 1: If the resolution requirement for a particular application is coarser than or equal to 0.03125, the designer should use only one word.

Note 2: Coordinate system should be referenced.

Table 80-VIII Acceleration Category, Feet/Second/Second

DOC. NO.* REV.*
DATE *
SHEET 1 OF 1

WORD NAME : Acceleration

WORD ID	: *	MAX VALUE	: *
SOURCES(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 512
SIGNAL TYPE	: 2's complement	LSB	: 0.03125
UNITS	: Feet/Second/Second	FULLSCALE	: 1,024

FIELD NAME	BIT NO.	DESCRIPTION
Acceleration	-00-S	Sign
	-01-N	MSB
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	Note 1
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: * - Application Dependent

Note 1: Coordinate system should be referenced.

Table 80-IX. Angular Category, Semicircles, Double Precision

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Angle

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 0.5
SIGNAL TYP E	: 2's complement	LSB	: 0.0000000005
UNITS	: Semicircles	FULLSCALE	: 1

FIELD NAME	BIT NO.	DESCRIPTION
Angle	MSW -00-S	Sign
	-01-N	MSB
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	Notes 1,2
	LSW -00-N	
	-01-N	
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: Semicircle = 1 pi radian * - Application Dependent
Note 1: If the resolution requirement for a particular application is coarser than or equal to 0.0000305176, the designer should use only one word.
Note 2: Coordinate system should be referenced.

Table 80-X. Angular Acceleration Category, Semicircles/Second/Second

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Angular Acceleration

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 4
SIGNAL TYPE	: 2's complement	LSB	: 0.0002441406
UNITS	: Semicircles/Second/Second	FULLSCALE	: 8

FIELD NAME	BIT NO.	DESCRIPTION
Angular Acceleration	-00-S	Sign
	-01-N	MSB
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	Note 1
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: Semicircle = 1 pi radian
* - Application Dependent

Note 1: Coordinate system should be referenced.

Table 80-XI. Angular Velocity Category, Semicircles/Second, Double Precision

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Angular Velocity

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 2
SIGNAL TYPE	: 2's complement	LSB	: 0.0000000018
UNITS	: Semicircles/Second	FULLSCALE	: 4

FIELD NAME		BIT NO.	DESCRIPTION
Angular Velocity	MSW	-00-S	Sign
		-01-N	MSB
		-02-N	
		-03-N	
		-04-N	
		-05-N	
		-06-N	
		-07-N	
		-08-N	
		-09-N	
		-10-N	
		-11-N	
		-12-N	
		-13-N	
		-14-N	
		-15-N	Notes 1, 2
	LSW	-00-N	
		-01-N	
		-02-N	
		-03-N	
		-04-N	
		-05-N	
		-06-N	
		-07-N	
		-08-N	
		-09-N	
		-10-N	
		-11-N	
		-12-N	
		-13-N	
		-14-N	
		-15-N	LSB

REMARKS: Semicircle = 1 pi radian * - Application Dependent

Note 1: If the resolution requirement for a particular application is coarser than or equal to 0.0001220703, the designer should use only one word.

Note 2: Coordinate system should be referenced.

Table 80-XII. ASCII Data Category (Character)

DOC. NO. * REV.*
DATE *
SHEET 1 OF 1

WORD NAME : Character

WORD ID	: *	MAX VALUE	: N/A
SOURCE(S)	: *	MIN VALUE	: N/A
DEST(S)	: *	RESOLUTION	: N/A
COMP RATE	: *	ACCURACY	: N/A
XMIT RATE	: *	MSB	: N/A
SIGNAL TYPE	: ASCII	LSB	: N/A
UNITS	: N/A	FULLSCALE	: N/A

FIELD NAME	BIT NO.	DESCRIPTION
Character N	-00-A MSB	
	-01 -A	
	-02-A	
	-03-A	Note 1
	-04-A	
	-05-A	
	-06-A	
	-07-A LSB	
Character N + 1	-08-A MSB	
	-09-A	
	-1O-A	
	-11-A	Note 1
	-12-A	
	-13-A	
	-14-A	
	-15-A LSB	

REMARKS: * - Application Dependent

Note 1: In standard 7-bit ASCII the first bit of each character field (MSB) shall be set to logic zero (0), and the 7-bit ASCII code shall occupy the remaining seven bits of the field.

Table 80-XIII. BCD Data Category (Channel Select)

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Channel Select

WORD ID	: *	MAX VALUE	: N/A
SOURCE(S)	: *	MIN VALUE	: N/A
DEST(S)	: *	RESOLUTION	: N/A
COMP RATE	: *	ACCURACY	: N/A
XMIT RATE	: *	MSB	: N/A
SIGNAL IVPE	: NBCD	LSB	: N/A
UNITS	: N/A	FULLSCALE	: N/A

FIELD NAME	BIT NO.	DESCRIPTION
Channel Select Thousands digit	-00-B MSB	
	-01-B	MAX VALUE = 9 MIN VALUE = 0
	-02-B	
	-03-B LSB	
Channel Select Hundreds Digit	-04-B MSB	
	-05-B	MAX VALUE = 9 MIN VALUE = 0
	-06-B	
	-07-B LSB	
Channel Select Tens digit	-08-B MSB	
	-09-B	MAX VALUE = 9 MIN VALUE = 0
	-10-B	
	-11-B LSB	
Channel Select Ones digit	-12-B MSB	
	-13-B	MAX VALUE = 9 MIN VALUE = 0
	-14-B	
	-15-B LSB	

REMARKS: * - Application Dependent

Table 80-XIV. Convergence Factor Categoy

DOC. No. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Convergence Factor

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 1
SIGNAL TYPE	: Unsigned Numeric	LSB	: 0.0000305176
UNITS	: N/A	FULLSCALE	: 2

FIELD NAME	BIT NO.	DESCRIPTION
Convergence Factor	-00-N MSB	
	-01-N	
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N LSB	

REMARKS: * - Application Dependent

Table 80-XV. Cosine/Sine Category, Double Precision

DOC. NO.* REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Cosine/Sine

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 0.5
SIGNAL TYPE	: 2's complement	LSB	:.0000000005
UNITS	: N/A	FULLSCALE	: 1

FIELD NAME	BIT NO.	DESCRIPTION
Cosine/Sine	MSW -00-S	Sign
	-01-N	MSB
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	Note 1, 2
	LSW -00-N	
	-01 -N	
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: * - Application Dependent

Note 1: If the resolution requirement for a particular application is coarser than or equal to 0.0000305176, the designer should use only one word.

Note 2: Coordinate system should be referenced.

Table 80-XVI. Counts Category (Signed)

DOC. NO. * REV.*
DATE *
SHEET 1 OF 1

WORD NAME : Counts

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
SMIT RATE	: *	MSB	: 16,384
SIGNAL TYPE	: 2's complement	LSB	: 1
UNITS	: *	FULLSCALE	: 32,767

FIELD NAME	BIT NO.	DESCRIPTION
Counts	-00-S	Sign
	-01-N	MSB
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: * - Application Dependent

Table 80-XVII. Counts Category (Unsigned)

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Counts

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 32,768
SIGNAL TYPE	: Unsigned Numeric	LSB	: 1
UNITS	: *	FULLSCALE	: 65,535

FIELD NAME	BIT NO.	DESCRIPTION
Counts	-00-N	MSB
	-01-N	
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-1O-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: * - Application Dependent

Table 80-XVIII. Data Validity Category (Checksum)

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Checksum

WORD ID	: *	MAX VALUE	: N/A
SOURCE(S)	: *		: N/A
DEST(S)	: *	RESOLUTION	: N/A
COMP RATE	: *	ACCURACY	: N/A
XMIT RATE	: *	MSB	: N/A
SIGNAL TYPE	: Unsigned Numeric	LSB	: N/A
UNITS	: N/A	FULLSCALE	: N/A

FIELD NAME	BIT NO.	DESCRIPTION
Checksum	-00-N	MSB
	-01-N	
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	Note 1
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: * - Application Dependent
Note 1: The checksum word consists of the arithmetic sum, without regard to overflows, of a selected group of data words. More than one checksum word maybe used, if required.

Table 80-XIX. Data Validity Category (Error Protection)

DOC. NO. * REV.*
DATE *
SHEET 1 OF 2

WORD NAME : Error Protection

WORD ID	: *	MAX VALUE	: N/A
SOURCE(S)	: *	MIN VALUE	: N/A
DEST(S)	: *	RESOLUTION	: N/A
COMP RATE	: *	ACCURACY	: N/A
XMIT RATE	: *	MSB	: N/A
SIGNAL TYPE	: Coded (BCH 31, 16, 3)	LSB	: N/A
UNITS	: N/A	FULLSCALE	: N/A

FIELD NAME	BIT NO.	DESCRIPTION
Error Protection Word	-00-C	MSB
	-01-C	
	-02-C	
	-03-C	
	-04-C	
	-05-C	
	-06-C	
	-07-C	Notes 1,2,3,4
	-08-C	
	-09-C	
	-10-C	
	-11-C	
	-12-C	
	-13-C	
	-14-C	LSB
	-15-0	

REMARKS: * - Application Dependent

Table 80-XIX. Data Validity Category (Error Protection) (Continued)

DOC. NO. * REV.*
DATE *
SHEET 2 OF 2

WORD NAME: Error Protection

Note 1: Other methods of error protection (detection and correction) are available for use. The use of other methods of error protection may cause system integration problems. First, certain error protection methods, such as CRC, may be susceptible to single point failures or other reliability problems. Secondly, a multiplicity of encoding standards will unnecessarily complicate the encoder/decoder function. Therefore, the use of BCH (31, 16, 3) is recommended for error protection.

Note 2: Number of errors required to be detected/corrected is application dependent.

Note 3: The BCH generating polynomial is:

$$G(X)=X^{15}+X^{11}+X^{10}+X^{9}+X^{8}+X^{7}+X^{5}+X^{3}+X^{2}+X+1,$$

where X^{15} indicates the MSB of the 16-bit data word field. BCH (31,16, 3) indicates a 31 -bit field, with 16 information bits and 15 check bits, which provide for error correction of 3 bits.

Note 4: The Error Protection Word shall immediately follow the data word to be protected. If multiword parameters are to be protected, the Error Protection Word will follow contiguously each 16-bit protected data word (e.g., Protected Data Word 1, Error Protection Word 1; Protected Data Word 2, Error Protection Word 2; etc.).

Table 80-XX. Deviation Category, DDM

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Deviation

WORD ID	: *	MAX VALUE	: Note 1
SOURCE(S)	: *	MIN VALUE	: Note 1
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 0.5
SIGNAL TYPE	: 2's complement	LSB	: 0.0000305176
UNITS	: DDM	FULLSCALE	: 1

FIELD NAME	BIT NO.	DESCRIPTION
Deviation	-00-S	Sign
	-01-N	MSB
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	Note 2
	-08-N	
	-09-N	
	-1O-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: DDM = Difference in Depth of Modulation

*-Application Dependent

Note 1: Range for localizer signals is ±0.4 DDM. Range for glideslope deviation is ±0.8 DDM.

Note 2: Positive values of localizer data indicate a fly-right command. Positive values of glideslope data indicate a fly-down command.

Table 80-XXI. Distance Category, Metres, Double Precision

DOC. NO * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Distance

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCCURACY	: *
XMIT RATE	: *	MSB	: 16,384
SIGNAL TYPE	: 2's complement	LSB	: 0.0000152588
UNITS	: Metres	FULLSCALE	: 32,768

FIELD NAME	BIT NO.		DESCRIPTION
Distance	MSW	-00-S	Sign
		-01-N	MSB
		-02-N	
		-03-N	
		-04-N	
		-05-N	
		-06-N	
		-07-N	
		-08-N	
		-09-N	
		-10-N	
		-11-N	
		-12-N	
		-13-N	
		-14-N	
		-15-N	Notes 1,2
	LSW	-00-N	
		-01-N	
		-02-N	
		-03-N	
		-04-N	
		-05-N	
		-06-N	
		-07-N	
		-08-N	
		-09-N	
		-10-N	
		-11-N	
		-12-N	
		-13-N	
		-14-N	
		-15-N	LSB

REMARKS: * - Application Dependent
Note 1: If the resolution requirement for a particular application is coarser than or equal to 1, the designer should use only one word.
Note 2: Coordinate system should be referenced.

Table 80-XXII. Distance Category, Feet, Double Precision

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Distance

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	:16,777,216
SIGNAL TYPE	: 2's complement	LSB	: 0.015625
UNITS	: Feet	FULLSCALE	:33,554,432

FIELD NAME		BIT NO.	DESCRIPTION
Distance	MSW	-00-S	Sign
		-01-N	MSB
		-02-N	
		-03-N	
		-04-N	
		-05-N	
		-06-N	
		-07-N	
		-08-N	
		-09-N	
		-10-N	
		-11-N	
		-12-N	
		-13-N	
		-14-N	
		-15-N	Notes 1, 2
	LSW	-00-N	
		-01-N	
		-02-N	
		-03-N	
		-04-N	
		-05-N	
		-06-N	
		-07-N	
		-08-N	
		-09-N	
		-10-N	
		-11-N	
		-12-N	
		-13-N	
		-14-N	
		-15-N	LSB

REMARKS: * - Application Dependent

Note 1: If the resolution requirement for a particular application is coarser than or equal to 1,024, the designer should use only one word.

Note 2: Coordinate system should be referenced.

Table 80-XX/11. Distrance Category, Kilometers, Double Precision

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Distance

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 16,384
SIGNAL TYPE	: 2's complement	LSB	: 0.000015258
UNITS	: Kilometres	FULLSCALE	: 32,768

FIELD NAME		BIT NO.	DESCRIPTION
Distance	MSW	-00-S	Sign
		-01-N	MSB
		-02-N	
		-03-N	
		-04-N	
		-05-N	
		-06-N	
		-07-N	
		-08-N	
		-09-N	
		-10-N	
		-11-N	
		-12-N	
		-13-N	
		-14-N	
		-15-N	Notes 1,2
	LSW	-00-N	
		-01-N	
		-02-N	
		-03-N	
		-04-N	
		-05-N	
		-06-N	
		-07-N	
		-08-N	
		-09-N	
		-1O-N	
		-11-N	
		-12-N	
		-13-N	
		-14-N	
		-15-N	LSB

REMARKS: * - Application Dependent
Note 1 If the resolution requirement for a particular application is coarser than or equal to 1, the designer should use only one word.
Note 2: Coordinate system should be referenced.

Table 80-XXIV. Distance Category, Nautical Miles (Low Range)

DOC. No. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Distance

WORDID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	:	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 256
SIGNAL TYPE	: 2's complement	LSB	: 0.015625
UNITS	: Nautical Miles	FULLSCALE	: 512

FIELD NAME	BIT NO.	DESCRIPTION
Distance	-00-S	Sign
	-01-N	MSB
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: * - Application Dependent

Table 80-XXV. Distance Category, Nautical Miles (High Range), Double Precision

DOC. NO. * REV.*
DATE *
SHEET 1 OF 1

WORD NAME : Distance

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 4,096
SIGNAL TYPE	: 2's complement	LSB	:0.0000038147
UNITS	: Nautical Miles	FULLSCALE	: 8,192

FIELD NAME		BIT NO.	DESCRIPTION
Distance	MSW	-00-S	Sign
		-01-N	MSB
		-02-N	
		-03-N	
		-04-N	
		-05-N	
		-06-N	
		-07-N	
		-08-N	
		-09-N	
		-10-N	
		-11-N	
		-12-N	
		-13-N	
		-14-N	
		-15-N	Note 1
	LSW	-00-N	
		-01-N	
		-02-N	
		-03-N	
		-04-N	
		-05-N	
		-06-N	
		-07-N	
		-08-N	
		-09-N	
		-10-N	
		-11-N	
		-12-N	
		-13-N	
		-14-N	
		-15-N	LSB

REMARKS: * - Application Dependent
Note 1: If the resolution requirement for a particular application is coarser than or equal to 0.25, the designer should use only one word.

Table 80-XXVI. Flow Category, Kilogram/Hour (Low Range)

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Flow

WORDID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	:
XMIT RATE	:	MSB	: 32,768
SIGNAL TYPE	: 2's complement	LSB	: 2
UNITS	: Kilograms/Hour	FULLSCALE	: 65,534

FIELD NAME	BIT NO.	DESCRIPTION
Flow	-00-S	Sign
	-01-N	MSB
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: * - Application Dependent

Table 80-XXVII. Flow Category, Kilograms/Minute (High Range)

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Flow

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 32,768
SIGNAL TYPE	: 2's complement	LSB	: 2
UNITS	: Kilograms/Minute	FULLSCALE	: 65,534

FIELD NAME	BIT NO.	DESCRIPTION
Flow	-00-S	Sign
	-01-N	MSB
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: * - Application Dependent

Table 80-XXVIII. Frequency Category, Hertz (Four Words)

DOC. NO. * REV. *
DATE *
SHEET 1 OF 4

WORD NAME : Frequency

WORD ID	: *	MAX VALUE	: N/A
SOURCE(S)	: *	MIN VALUE	: N/A
DEST(S)	: *	RESOLUTION	: N/A
COMP RATE	: *	ACCURACY	: N/A
XMIT RATE	:	MSB	: N/A
SiGNAL TYPE	: NBCD	LSB	: N/A
UNITS	: Hertz	FULLSCLE	: N/A

FIELD NAME	BIT NO.	DESCRIPTION
Frequency (1,000 GHz)	-00-B	MSB
	-01-B	
		LSB = 1 X 10^{12} Hz (1,000 GHz)
	-02-B	
	-03-B	LSB
Frequency (100 GHz)	-04-B	MSB
	-05-B	
		LSB= 1 X 10^{11} Hz (100 GHz)
	-06-B	
	-07-B	LSB
Frequency (10 GHz)	-08-B	MSB
	-09-B	
		LSB = 1 X 10^{10} Hz (10 GHz)
	-10-B	
	-11-B	LSB
Frequency (1 GHz)	-12-B	MSB
	-13-B	
		LSB = 1 X 10^{9} Hz (1 GHz)
	-14-B	
	-15-B	LSB

REMARKS: Four-word quantity-word 1 of 4. Any contiguous grouping (e.g., 1,2) can be used to create a frequency data block.
* - Application Dependent

Table 80-XXVIII. Frequency Category, Hertz (Four Words) (Continued)

DOC. NO. * REV. *
DATE *
SHEET 2 OF 4

WORD NAME : Frequency

WORD ID	: *	MAX VALUE	: N/A
SOURCE(S)	: *	MIN VALUE	: N/A
DEST(S)	: *	RESOLUTION	: N/A
COMP RATE	: *	ACCURACY	: N/A
XMIT RATE	: *	MSB	: N/A
SIGNAL TYPE	: NBCD	LSB	: N/A
UNITS	: Hertz	FULLSCLE	: N/A

FIELD NAME	BIT NO.	DESCRIPTION
Frequency (100 MHz)	-00-B	MSB
	-01-B	LSB = 1 X 10^8 Hz (100 MHz)
	-02-B	
	-03-B	LSB
Frequency (10 MHz)	-04-B	MSB
	-05-B	LSB = 1 X 10^7 Hz(10 MHz)
	-06-B	
	-07-B	LSB
Frequency (1 MHz)	-08-B	MSB
	-09-B	LSB = 1 X 10^6 Hz (1 MHz)
	-10-B	
	-11-B	LSB
Frequency (100 kHz)	-12-B	MSB
	-13-B	LSB = 1 X 10^5 Hz (100 kHz)
	-14-B	
	-15-B	LSB

REMARKS: Four-word quantity-word 2 of 4. Any contiguous grouping (e.g., 1, 2) can be used to create a frequency data block.
* - Application Dependent

Table 80-XXVIII. Frequency Category, Hertz (Four Words) (Continued)

DOC. NO. * REV. *
DATE *
SHEET 3 OF 4

WORD NAME : Frequency

WORD ID	: *	MAX VALUE	: N/A
SOURCE(S)	: *	MIN VALUE	: N/A
DEST(S)	: *	RESOLUTION	: N/A
COMP RATE	: *	ACCURACY	: N/A
XMIT RATE	: *	MSB	: N/A
SIGNAL TYPE	: NBCD	LSB	: N/A
UNITS	: Hertz	FULLSCALE	: N/A

FIELD NAME	BIT NO.	DESCRIPTION
Frequency (10 kHz)	-00-B	MSB
	-01-B	
	-02-B	LSB = 1 X 10^4 Hz (10 kHz)
	-03-B	LSB
Frequency (1 kHz)	-04-B	MSB
	-05-B	
	-06-B	LSB = 1 X 10^3 Hz (10 kHz)
	-07-B	LSB
Frequency (100 Hz)	-08-B	MSB
	-09-B	
	-10-B	LSB = 1 X 10^2 Hz (100 Hz)
	-11-B	LSB
Frequency (10 Hz)	-12-B	MSB
	-13-B	
	-14-B	LSB = 10 Hz
	-15-B	LSB

REMARKS: Four-word quantity-word 3 of 4. Any contiguous grouping (e.g., 1,2) can be used to create a frequency data block.
l - Application Dependent

Table 80-XXVIII. Frequency Category, Hertz (Four Words) (Continued)

DOC. NO. * REV.*l
DATE *
SHEET 4 OF 4

WORD NAME : Frequency

WORD ID : *
SOURCE(S) : *
DEST(S) : *
COMP RATE : *
XMIT RATE : *
SIGNAL TYPE : NBCD
UNITS : Hertz

MAX VALUE : N/A
MIN VALUE : N/A
RESOLUTION : N/A
ACCURACY : N/A
MSB : N/A
LSB : N/A
FULLSCALE : N/A

FIELD NAME	BIT NO.	DESCRIPTION
Frequency (1 Hz)	-00-B	MSB
	-01-B	
	-02-B	LSB = 1 Hz
	-03-B	LSB
Frequency (0.1 Hz)	-04-B	MSB
	-05-B	
	-06-B	LSB = 1 X 10^{-1} Hz (0.1 Hz)
	-07-B	LSB
Frequency (0.01 Hz)	-08-B	MSB
	-09-B	
	-10-B	LSB = 1 X 10^{-2} Hz (0.01 Hz)
	-11-B	LSB
Frequency (0.001 Hz)	-12-B	MSB
	-13-B	
	-14-B	LSB = 1 X 10^{-3} Hz (0.001 Hz)
	-15-B	LSB

REMARKS: Four-word quantity-word 4 of 4. Any contiguous grouping (e.g., 1, 2) can be used to create a frequency data block.
* - Application Dependent

Table 80-XXIX. Frequency Category, Kilohertz (ADF)

DOC. No. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : ADF, Low Frequency

WORDID	: *	MAX VALUE	: N/A
SOURCE(S)	: *	MIN VALUE	: N/A
DEST(S)	: *	RESOLUTION	: N/A
COMP RATE	: *	ACCURACY	: N/A
XMIT RATE	: *	MSB	: N/A
SIGNAL TYPE	: Coded, NBCD, Discrete	LSB	: N/A
UNITS	: Kilohertz	FULLSCALE	: N/A

FIELD NAME	BIT NO.	DESCRIPTION	
Thousands digit	-00-C	MSB — 1 = 2000.0 kHz	
	-01-C	LSB — 1 = 1000.0 kHz	
Hundreds digit	-02-B	MSB — 1 = 800.0 kHz	
	-03-B	1 = 400.0 kHz	Note 1
	-04-B	1 = 200.0 kHz	
	-05-B	LSB — 1 = 100.0 kHz	
Tens digit	-06-B	MSB — 1 = 80.20 kHz	
	-07-B	1 = 40.0 kHz	Note 1
	-08-B	1 = 20.0 kHz	
	-09-B	LSB — 1 = 10.0 kHz	
Ones digit	-1O-B	MSB — 1 = 8.0 kHz	
	-11-B	1 = 4.0 kHz	Note 1
	-12-B	1 = 2.0 kHz	
	-13-B	LSB — 1 = 1.0 kHz	
Tenths digit	-14-D	1 = 0.5 kHz	
	-15-0	Not used	

REMARKS: * - Application Dependent

Note 1: Valid range 0000-1001 (binary).

Table 80-XXX. Frequency Category, Megahertz (VHF/UHF)

Doc. No. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : VHF/UHF Frequency

WORD ID	: *	MAX VALUE	: N/A
SOURCE(S)	: *	MIN VALUE	: N/A
DEST(S)	: *	RESOLUTION	: N/A
COMP RATE	: *	ACCURACY	: N/A
XMIT RATE	:	MSB	: N/A
SIGNAL TYPE	: Coded, NBCD	LSB	: N/A
UNITS	: Megahertz	FULLSCALE	: N/A

FIELD NAME	BIT NO.	DESCRIPTION	
Hundreds digit	-00-C	MSB — 1 = 200.0 MHz	
	-01-C	LSB — 1 = 100.0 MHz	
Tens digit	-02-B	MSB — 1 = 80.0 MHz	
	-03-B	1 = 40.0 MHz	Note 1
	-04-B	1 = 20.0 MHz	
	-05-B	LSB — 1 = 10.0 MHz	
Ones digit	-06-B	MSB — 1 = 8.0 MHz	
	-07-B	1 = 4.0 MHz	Note 1
	-08-B	1 = 2.0 MHz	
	-09-B	LSB — 1 = 1.0 MHz	
Tenths digit	-10-B	MSB — 1 = 0.8 MHz	
	-11-B	1 = 0.4 MHz	Note 1
	-12-B	1 = 0.2 MHz	
	-13-B	LSB — 1 = 0.1 MHz	
Hundredths digit	-14-C	MSB — 1 = 0.050 MHz	
	-15-C	LSB — 1 = 0.025 MHz	

REMARKS: * - Application Dependent

Note 1: Valid range 0000-1001 (binary).

Table 80-XXXI. Mass Category, Kilograms (Low Range)

DOC. NO.* REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Mass

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	:
XMIT RATE	:	MSB	: 2,048
SIGNAL TYPE	: 2's complement	LSB	: 0.125
UNITS	: Kilograms	FULLSCALE	: 4,096

FIELD NAME	BIT NO.	DESCRIPTION
Mass	-00-S	Sign
	-01-N	MSB
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: * - Application Dependent

Table 80-XXXII. Mass Category, Kilograms (High Range)

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Mass

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	:
XMIT RATE	:	MSB	: 262,144
SIGNAL TYPE	: 2's complement	LSB	: 16
UNITS	: Kilogram	FULLSCALE	; 524,272

FIELD NAME	BIT NO.	DESCRIPTION
Mass	-00-S	Sign
	-01-N	MSB
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: * - Application Dependent

Table 80-XXXIII. MGRS Category (Five Words)

DOC. NO. * REV.*
DATE *
SHEET 1 OF 7

WORD NAME : MGRS

WORD ID	: *	MAX VALUE	: N/A
SOURCE(S)	: *	MIN VALUE	: N/A
DEST(S)	: *	RESOLUTION	: N/A
COMP RATE	: *	ACCURACY	: N/A
XMIT RATE	: *	MSB	: N/A
SIGNAL TYPE	: Coded, ASCII	LSB	: N/A
UNITS	: N/A	FULLSCALE	: N/A

FIELD NAME	BIT NO.	DESCRIPTION
Ellipsoid/Datum	-00-C	MSB
	-01-C	Most Significant Character
	-02-C	Notes 1,3
	-03-C	LSB
Ellipsoid/Datum	-04-C	MSB
	-05-C	Least Significant Character
	-06-C	Notes 2,3
	-07-C	LSB
MGRS Grid Zone	-08-A	MSB
	-09-A	
	-10-A	
	-11-A	Column Number
	-12-A	Most Significant Digit
	-13-A	Note 3
	-14-A	
	-15-A	LSB

REMARKS: Five-word quantity-word 1 of 5. * - Application Dependent
Note 1: Hexadecimal values 0 through 9 are valid.
Note 2: Hexadecimal values 0 through F are valid.
Note 3: Column Number range: 1 to 60 (decimal).

Table 80-XXXIII. MGRS Category (Five Words) (Continued)

WORD NAME : MGRS
Note 3:

Ellipsoid	Hex Code	Datum
International	30	Local Astro
	00	Camp Area Astro
	01	European
	02	Geodetic Datum 1949
	03	Herat North
	04	Hjorsey 1955
	05	Hu-tzu-shan
	06	Maui
	07	Oahu
	08	Kauai
	09	Qornoq
	0A	Provisional South American 1956
	0B	Corrego Alegre
	0C	Campo Inchauspe
	0D	Chua Astro
	0E	Yacare
	0F	Tanerarive Absv. 1925
Clarke 1866	31	Local Astro
	10	Guam 1963
	11	Luzon
	12	CONUS
	13	Alaska and Canada
	14	Luzon Special
Clarke 1880	32	Local Astro
	20	Adindan
	21	Arc 1950
	22	Ghana
	23	Liberia 1964
	24	Merchich
	25	Nigeria
	26	Sierra Leone 1960
	27	Voirol
Everest	33	Local Astro
	3A	Indian
	3B	Timbalai
	3C	Indian Special

Table 80-XXXIII. MGRS Category (Five Words) (Continued)

DOC. NO. * REV. *
DATE *
SHEET 3 OF 7

WORD NAME : MGRS

Note 3 (continued):

Ellipsoid	Hex Code	Datum
Bessel	34	Local Astro
	40	Bukit Rimpah
	42	Djakarta
	43	G. Segara
	44	G. Serindung
	45	Montjong Lowe
	46	Tokyo
	47	Tokyo Special
Australian National	35	Local Astro
	50	Australian Geodetic
Airy	36	Local Astro
	60	Ordinance Survey of Great Britain 1936
Hough	37	Local Astro
South America	38	Local Astro
Modified Everest	39	Local Astro
	90	Kertau (Malayan Revised Triangulation)
WGS-72	41	Local Astro
	4A	WGS-72 Special

Table 80-XXXIII. MGRS Category (Five Words) (Continued)

DOC. NO. * REV.*
DATE *
SHEET 4 OF 7

WORD NAME : MGRS

WORD ID	:	*	MAX VALUE	: N/A
SOURCE(S)	:	*	MIN VALUE	: N/A
DEST(S)	:	*	RESOLUTION	: N/A
COMP RATE	:	*	ACCURACY	: N/A
XMIT RATE	:		MSB	: N/A
SIGNAL TYPE	:	ASCII	LSB	: N/A
UNITS	:	NIA	FULLSCALE	: N/A

FIELD NAME	BIT NO.	DESCRIPTION
MGRS Grid Zone	-00-A	MSB
	-01-A	
	-02-A	
	-03-A	Column Number
	-04-A	Least Significant Digit Note 1
	-05-A	
	-06-A	
	-07-A	LSB
MGRS Grid Zone	-08-A	MSB
	-09-A	
	-10-A	
	-11-A	Row Letter
	-12-A	
	-13-A	
	-14-A	
	-15-A	LSB

REMARKS: Five-word quantity-word 2 of 5.
* - Application Dependent
Note 1: Column Number range: 1 to 60 (decimal).

Table 80-XXXIII. MGRS Category (Five Words) (Continued)

DOC. NO. * REV. *
DATE *
SHEET 5 OF 7

WORD NAME : MGRS

WORD ID	: *	MAX VALUE	: N/A
SOURCE(S)	: *	MIN VALUE	: N/A
DEST(S)	: *	RESOLUTION	: N/A
COMP RATE	: *	ACCURACY	: N/A
XMIT RATE	: *	MSB	: N/A
SIGNAL TYPE	: ASCII	LSB	: N/A
UNITS	: N/A	FULLSCALE	: N/A

FIELD NAME	BIT NO.	DESCRIPTION
MGRS Grid Square	-00-A	MSB
	-01-A	
	-02-A	
	-03-A	Column Letter Most Significant Character
	-04-A	
	-05-A	
	-06-A	
	-07-A	LSB
MGRS Grid Square	-08-A	MSB
	-09-A	
	-10-A	
	-11-A	Row Letter Least Significant Character
	-12-A	
	-13-A	
	-14-A	
	-15-A	LSB

REMARKS: Five-word quantity-word 3 of 5.
* -Application Dependent

Table 80-XXXIII. MGRS Category (Five Words) (Continued)

DOC. NO. * REV. *
DATE *
SHEET 6 OF 7

WORD NAME : MGRS

WORD ID	: *	MAX VALUE	: 99,998
SOURCE(S)	: *	MIN VALUE	: 0
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	:	MSB	: 65,536
SIGNAL TYPE	: Unsigned Numeric	LSB	: 2
UNITS	: Metres	FULLSCALE	: 131,070

FIELD NAME	BIT NO.	DESCRIPTION
MGRS Easting	-00-N	MSB
	-01-N	
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: Five-word quantity-word 4 of 5.
* - Application Dependent

DOC. NO. * REV. *
DATE *
SHEET 7 OF 7

WORD NAME : MGRS

WORD ID : *
SOURCE(S) : *
DEST(S) : *
COMP RATE : *
XMIT RATE : *
SIGNAL TYPE : Unsigned Numeric
UNITS : Metres

MAX VALUE : 99,998
MIN VALUE : 0
RESOLUTION : *
ACCURACY : *
MSB : 65,536
LSB : 2
FULLSCALE : 131,070

FIELD NAME	BIT NO.	DESCRIPTION
MGRS Northing	-00-N	MSB
	-01-N	
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: Five-word quantity-word 5 of 5.
* - Application Dependent

Table 80-XXXIV. Percent Category

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Percent

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	:
XMIT RATE	:	MSB	: 128
SIGNAL TYPE	: 2's complement	LSB	: 0.0078125
UNITS	: N/A	FULLSCALE	: 256

FIELD NAME	BIT NO.	DESCRIPTION
Percent	-00-S	Sign
	-01-N	MSB
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-1O-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: * - Application Dependent

Table 80-XXXV. Pressure Category, Kilopascals, Double Precision

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Pressure

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 16,384
SiGNAL TYPE	: 2's complement	LSB	:0.0000152588
UNITS	: Kilopascals	FULLSCALE	: 32,768

FIELD NAME	BIT NO.	DESCRIPTION
Pressure	MSW-00-S	Sign
	-01-N	MSB
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	Note 1
	LSW -00-N	
	-01-N	
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: * - Application Dependent

Note 1: If the resolution requirement for a particular application is coarser than or equal to 1, the designer should use only one word.

Table 80-XXXVI. Pressure Category, Inches of Mercury

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Pressure

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 64
SIGNAL TYPE	: 2's complement	LSB	:0.00390625
UNITS	: Inches of Mercury	FULLSCALE	: 128

FIELD NAME	BIT NO.	DESCRIPTION
Pressure	-00-S	Sign
	-01-N	MSB
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: * - Application Dependent

Table 80-XXVII. Ratio Category

DOC. NO. *
REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Ratio

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	:
XMIT RATE	:	MSB	: 1
SIGNAL TYPE	: Unsigned Numeric	LSB	: 0.0000305176
UNITS	: N/A	FULLSCALE	: 2

FIELD NAME	BIT NO.	DESCRIPTION
Ratio	-00-N	MSB
	-01-N	
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: * - Application Dependent

Table 80-XXXVIII. Temperature Category, Degrees Celcius

DOC. NO. *
DATE *
REV. *

WORD NAME : Temperature
SHEET 1 OF 1

WORD NAME : *
SOURCE(S) : *
DEST(S) : *
COMP RATE : *
XMIT RATE : *
SIGNAL TYPE : 2's complement
UNITS : Degrees Celsius

MAX VALUE : *
MIN VALUE : *
RESOLUTION : *
ACCURACY : *
MSB : 1,024
LSB : 0.0625
FULLSCALE : 2,046

FIELD NAME	BIT NO.	DESCRIPTION
Temperature	-00-S	Sign
	-01-N	MSB
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-I5-N	LSB

REMARKS: * - Application Dependent

Table 80-XXXIX. Time Category (Three Words)

DOC. NO. * REV. *
DATE *
SHEET 1 OF 3

WORD NAME : Month/Day (Calendar)

WORD ID : *
SOURCE(S) : *
DEST(S) : *
COMP RATE : *
XMIT RATE : *
SIGNAL TYPE : NBCD
UNITS : N/A

MAX VALUE : N/A
MIN VALUE : N/A
RESOLUTION : N/A
ACCURACY : N/A
MSB : N/A
LSB : N/A
FULLSCALE : N/A

FIELD NAME	BIT NO.	DESCRIPTION
Month, Tens digit	-00-0	MSB
	-01-0	MAX VALUE = 1
	-02-0	MIN VALUE = 0 Note 1
	-03-B	LSB
Month, Ones digit	-04-B	MSB
	-05-B	MAX VALUE = 9
	-06-B	MIN VALUE = 0 Note 1
	-07-B	LSB
Day, Tens digit	-08-0	MSB
	-09-0	MAX VALUE = 3
	-10-B	MIN VALUE = 0 Note 2
	-11-B	LSB
Day, Ones digit	-12-B	MSB
	-13-B	MAX VALUE = 9
	-14-B	MIN VALUE = 0 Note 2
	-15-B	LSB

REMARKS: Three-word quantity-word 1 of 3. Any contiguous grouping (e.g., 1,2) can be used to create a time data block. * - Application Dependent
Note 1: Valid range 0-12 (decimal).0 = Unused field; 1 = January, etc.
Note 2: Valid range 0-31 (decimal). 0 = Unused field.

Table 80-XXXIX. Time Category (Three Words) (Continued)

DOC. NO. * REV. *
DATE *
SHEET 2 OF 3

WORD NAME : Hour/Minute

WORD ID	: *	MAX VALUE	: N/A
SOURCE(S)	: *	MIN VALUE	: N/A
DEST(S)	: *	RESOLUTION	: N/A
COMP RATE	: *	ACCURACY	: N/A
XMIT RATE	:	MSB	: N/A
SIGNAL TYPE	: NBCD	LSB	: N/A
UNITS	: N/A	FULLSCALE	: N/A

FIELD NAME	BIT NO.	DESCRIPTION
Hour, Tens digit	-00-0	MSB
	-01-0	MAX VALUE = 2
	-02-B	MIN VALUE = 0 Note 3
	-03-B	LSB
Hour, Ones digit	-04-B	MSB
	-05-B	MAX VALUE = 9
	-06-B	MIN VALUE = 0 Note 3
	-07-B	LSB
Minute, Tens digit	-08-0	MSB
	-09-B	MAX VALUE = 5
	-10-B	MIN VALUE = 0 Note 4
	-11-B	LSB
Minute, Ones digit	-12-B	MSB
	-13-B	MAX VALUE = 9
	-14-B	MIN VALUE = 0 Note 4
	-15-B	LSB

REMARKS: Three-word quantity-word 2 of 3. Any contiguous grouping (e.g., 1,2) can be used to create a time data block. * - Application Dependent
Note 3: Valid range 0-23 (decimal).
Note 4: Valid range 0-59 (decimal).

Table 80-XXXIX. Time Category (Three Words) (Continued)

DOC. NO. * REV. *
DATE *
SHEET 3 OF 3

WORD NAME : Second

WORD ID	: *	MAX VALUE	: N/A
SOURCE(S)	: *	MIN VALUE	: N/A
DEST(S)	: *	RESOLUTION	: N/A
COMP RATE	: *	ACCURACY	: N/A
XMIT RATE	: *	MSB	: N/A
SIGNAL TYPE	: NBCD	LSB	: N/A
UNITS	: N/A	FULLSCALE	: N/A

FIELD NAME	BIT NO.	DESCRIPTION
Second, Tens digit	-00-0	MSB
	-01-B	MAX VALUE = 5
		MIN VALUE = 0
	-02-B	Note 5
	-03-B	LSB
Second, Ones digit	-04-B	MSB
	-05-B	MAX VALUE = 9
		MIN VALUE = 0
	-06-B	Note 5
	-07-B	LSB
Second, Tenths digit	-08-B	MSB
	-09-B	MAX VALUE = 9
		MIN VALUE = 0
	-1O-B	Note 5
	-11-B	LSB
Second, Hundredths digit	-12-B	MSB
	-13-B	MAX VALUE = 9
		MIN VALUE = 0
	-14-B	Note 5
	-15-B	LSB

REMARKS: Three-word quantity-word 3 of 3. Any contiguous grouping (e.g., 1,2) can be used to create a time data block. * - Application Dependent
Note 5: Valid range 0.00-59.99 (decimal).

Table 80-XL. Time Category (Time Tag), Microseconds, Double Precision

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Time Tag

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 2,097,152
SIGNAL TYPE	: Unsigned Numeric	LSB	: 0.0009766
UNITS	: Microseconds	FULLSCALE	: 4,194,304

FIELD NAME		BIT NO.	DESCRIPTION
Time Tag	MSW	-00-N	MSB
		-01-N	
		-02-N	
		-03-N	
		-04-N	
		-05-N	
		-06-N	
		-07-N	
		-08-N	
		-09-N	
		-10-N	
		-11-N	
		-12-N	
		-13-N	
		-14-N	
		-15-N	Note 1
	LSW	-00-N	
		-01-N	
		-02-N	
		-03-N	
		-04-N	
		-05-N	
		-06-N	
		-07-N	
		-08-N	
		-09-N	
		-1O-N	
		-11-N	
		-12-N	
		-13-N	
		-14-N	
		-15-N	LSB

REMARKS: * - Application Dependent
Note 1: If the resolution requirement for a particular application is coarser than or equal to 64, the designer should use only one word.

Table 80-XLI. Time Category (Time To), Seconds

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORDNAME : Time To

WORD ID	: *		MAX VALUE :	*
SOURCE(S)	: *		MIN VALUE :	*
DEST(S)	: *		RESOLUTION :	*
COMP RTE	: *		ACCURACY :	
XMIT RATE	:		MSB :	32,768
SIGNAL TYPE	: Unsigned Numeric		LSB :	1
UNITS	: Seconds		FULLSCALE :	65,535

FIELD NAME	BIT NO.	DESCRIPTION
Time to Go	-00-N	MSB
	-01-N	
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-1O-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: * - Application Dependent

Table 80-XLII. Time Category, Pulse Repetition Interval

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Pulse Repetition Interval (PRI)

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 16,384
SIGNAL TYPE	: Unsigned Numeric	LSB	: 0.5
UNITS	: Microseconds	FULLSCALE	: 32,768

FIELD NAME	BIT NO.	DESCRIPTION
Pulse Repetition Interval	-00-N	MSB
	-01 -N	
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: * - Application Dependent.

Table 80-XLIII. Time Category, Pulse Width

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Pulse Width

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 1,638,400
SIGNAL TYPE	: Unsigned Numeric	LSB	: 50
UNITS	: Nanoseconds	FULLSCALE	: 3,276,750

FIELD NAME	BIT NO.	DESCRIPTION
Pulse Width	-00-N	MSB
	-01-N	
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-1O-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: * - Application Dependent.

Table 80-XLIV. Torque Category, Newton-Metres, Double Precision

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Torque

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 16,384
SIGNAL TYPE	: 2's complement	LSB	: .0000152588
UNITS	: Newton-Metres	FULLSCALE	: 32,768

FIELD NAME	BIT NO.	DESCRIPTION
Torque	MSW -00-S	Sign
	-01-N	MSB
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	Note 1
	LSW -00-N	
	-01-N	
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: * - Application Dependent
Note 1: If the resolution requirement for a particular application is coarser than or equal to 1, the designer should use only one word.

Table 80-XLVa. Vector Word Category

DOC. NO. * REV. *
DATE *
SHEET 1 OF 2

WORD NAME : Vector Word (Asynchronous Message Demand)

WORDID	: ******-****BC-01	MAX VALUE	: N/A
SOURCE(S)	: *	MIN VALUE	: N/A
DEST(S)	: *	RESOLUTION	: N/A
COMP RATE	: N/A	ACCURACY	: N/A
XMIT RATE	: *	MSB	: N/A
SIGNAL TYPE	: Discrete, Coded	LSB	: N/A
UNITS	: N/A	FULLSCALE	: N/A

FIELD NAME	BIT NO.	DESCRIPTION
Format Flag	-00-0	Always set to zero
Reserved	-01-0	MSB
	-02-0	Always set to 0000
	-03-0	
	-04-0	LSB
T/R	-05-D	0 = receive, 1 = transmit
Subaddress/Mode	-06-C	MSB
	-07-C	00001 to 11110 = Subaddress of transmit or receive terminal*
	-08-C	00000 or 11111 = Decode contents of mode code field as five-bit mode code
	-09-C	
	-10-C	LSB
Data Word Count/ Mode Code	-11-C	MSB
	-12-C	Number of words to be transmitted or received, Note 1 *
	-13-C	Legal range 00000-11111 00000 indicates 32 data words
	-14-C	MIL-STD-1553 mode code legal values, Note 2
	-15-C	LSB

REMARKS: * - Application Dependent
This data word is to be used in conjunction with a Transmit Vector Word Mode Code.
Note 1: For RT-to-RT messages, the word count must be identical in the command word for both the transmit and receive terminals.

Table 80-XLVa. Vector Word Category (Continued)

DOC. NO. * REV. *
DATE *
SHEET 2 OF 2

WORD NAME: Vector Word (Asynchronous Message Demand)

Note 2: 00000- Dynamic Bus Control
00001- Synchronize
00010- Transmit Status Word
00011- Initiate Self-Test
00100- Transmitter Shutdown
00101- Override Transmitter Shutdown
00110- Inhibit Terminal Flag Bit
00111- Override Inhibit Terminal Flag Bit
01000- Reset Remote Terminal
10000- Transmit Vector Word
10001- Synchronize
10010- Transmit Last Command Word
10011- Transmit BIT Word
10100- Selected Transmitter Shutdown
10101- Override Selected Transmitter Shutdown

Table 80-XLVb. Vector Word Category

DOC. NO.* REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Vector Word (Asynchronous Action Demand)

WORD ID : ******-****BC-01
SOURCE(S) : *
DEST(S) : *
COMP RATE : N/A
XMIT RATE : *
SIGNAL TYPE : Discrete, Coded
UNITS : N/A

MAX VALUE : N/A
MIN VALVE : N/A
RESOLUTION : N/A
ACCURACY : N/A
MSB : N/A
LSB : N/A
FULLSCALE : N/A

FIELD NAME	BIT NO.	DESCRIPTION
Format Flag	-00-1	Always set to logic one
Notification Flag	-01-C	User defined
	-02-C	User defined
	-03-C	User defined
	-04-C	User defined
	-05-C	User defined
	-06-C	User defined
	-07-C	User defined
	-08-C	User defined
	-09-C	User defined
	-10-C	User defined
	-11-C	User defined
	-12-C	User defined
	-13-C	User defined
	-14-C	User defined
	-15-C	User defined

REMARKS: * - Application Dependent

Table 80-XLVI. Velocity Category, Metres/Second, Double Precision

DOC. NO. * REV.*
DATE *
SHEET 1 OF 1

WORD NAME : Velocity

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 4,096
SIGNAL TYPE	: 2's complement	LSB	:0.0000038147
UNITS	: Metres/Second	FULLSCALE	: 8,192

FIELD NAME	BIT NO.	DESCRIPTION
Velocity	MSW -00-S	Sign
	-01-N	MSB
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	Notes 1,2
	LSW -00-N	
	-01-N	
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: * - Application Dependent
Note 1: If the resolution requirement for a particular application is coarser than or equal to 0.25, the designer should use only one word.
Note 2: Coordinate system should be referenced.

Table 80-XLVII. Velocity Category, Feet/Second, Double Precision

DOC. NO. * REV. *
DATE*
SHEET 1 OF 1

WORD NAME : Velocity

WORDID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 4,096
SIGNAL TYPE	: 2's complement	LSB	:.0000038147
UNITS	: Feet/Second	FULLSCALE	: 8,192

FIELD NAME	BIT NO.	DESCRIPTION
Velocity	MSW -00-S	Sign
	-01-N	MSB
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	Notes 1,2
	LSW -00-N	
	-01-N	
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: * - Application Dependent
Note 1: If the resolution requirement for a particular application is coarser than or equal to 0.25, the designer should use only one word.
Note 2: Coordinate system should be referenced.

Table 80-XLVIII. Velocity Category, Kilometres/Hour

DOC. No. * REV. *
DATE*
SHEET 1 OF 1

WORD NAME : Velocity

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 1,024
SIGNAL TYPE	: 2's complement	LSB	: 0.0625
UNITS	: Kilometres/Hour	FULLSCALE	: 2,048

FIELD NAME	BIT NO.	DESCRIPTION
Velocity	-00-S	Sign
	-01-N	MSB
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	Note 1
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: * - Application Dependent

Note 1: Coordinate system should be referenced.

Table 80-XLIX. Velocity Category, Knots

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Velocity

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 2,048
SIGNAL TYPE	: 2's complement	LSB	: 0.125
UNITS	: Knots	FULLSCALE	: 4,096

FIELD NAME	BIT NO.	DESCRIPTION
Velocity	-00-S	Sign
	-01-N	MSB
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	Note 1
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: * - Application Dependent

Note 1: Coordinate system should be referenced.

Table 80-L. Velocity Category, Mach

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Velocity

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 16
SIGNAL TYPE	: 2's complement	LSB	: 0.0009765625
UNITS	: Mach Number	FULL SCALE	: 32

FIELD NAME	BIT NO.	DESCRIPTION
Velocity	-00-S	Sign
	-01-N	MSB
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: * - Application Dependent

Table 80-LI. Voltage Category, Volts, Double Precision

DOC. NO.* REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Voltage

WORD ID	: *	MAX VALUE	: *
SOURCE(S)	: *	MIN VALUE	: *
DEST(S)	: *	RESOLUTION	: *
COMP RATE	: *	ACCURACY	: *
XMIT RATE	: *	MSB	: 256
SIGNAL TYPE	: 2's complement	LSB	:0.0000002384
UNITS	: volts	FULLSCALE	: 512

FIELD NAME	BIT NO.	DESCRIPTION
Voltage	MSW -00-S	Sign
	-01-N	MSB
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11 -N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	Note 1
	LSW -00-N	
	-01-N	
	-02-N	
	-03-N	
	-04-N	
	-05-N	
	-06-N	
	-07-N	
	-08-N	
	-09-N	
	-10-N	
	-11-N	
	-12-N	
	-13-N	
	-14-N	
	-15-N	LSB

REMARKS: * - Application Dependent

Note 1: If the resolution requirement for a particular application is coarser than or equal to 0.015625, the designer should use only one word.

80.3 MESSAGE FORMATS

Message is defined in MIL-STD-1553B as the transmission of a command word, status word, and data words if they are specified. For the RT-to-RT transmission, the message definition is expanded to include the two command words, the two status words, and the data words. In this handbook, a message is defined to be the data words (1-32) that are part of the information transfer format. The information transfer format is defined the same as the 1553B message definition. For purposes of the discussion to follow, message format is defined to mean the order and content of the data words within the information transfer formats shown in figures 6 and 7 of MIL-STD-1553B.

The general rules for message construction and standard Interface Control Document (ICD) message formats are included in this section.

80.3.1 Interface Control Document Message Presentation Format

The ICD format required for the documentation of all messages in a 1553 system is shown in tables 80-LIII through 80-LXII. Figure 80-8 provides the detailed layout for a typical message ICD presentation sheet. Figure 80-9 provides an example of a completed message ICD presentation sheet. Presentation formats are provided for the following 1553 transfer types:

a. BC-to-RT Transfer
b. RT-to-BC Transfer
c. RT-to-RT Transfer
d. Mode Command Without Data Word
e. Mode Command With Data Word (Transmit)
h. Mode Command With Data Word (Receive)
g. BC-to-RT Transfer, Broadcast
h. RT-to-RT Transfer, Broadcast
i. Mode Command Without Data Word, Broadcast
j. Mode Command With Data Word, Broadcast

Tables 80-LIII through 80-LXII are the skeleton ICD sheets. The definition of each entry is as follows:

DOC. NO. : The interface control document number.

REV. : The revision symbol for this sheet.

DATE : The calendar date of the latest revision to this sheet.

SHEET 1 OF # : This page count allows multiple pages, for extensive REMARKS.

MESSAGE NAME : The formal name selected for this message-A name that is to be used in this and other documents.

MESSAGE ID : Code identifying the message. The MESSAGE ID is a subset of the WORD ID and is constructed as follows:

XXXXSX-YYYYSY

where:

XXXX = Transmitting terminal name (see Table 80-III for examples).

SX = Transmitting terminal 1553 subaddress from which the word originated.

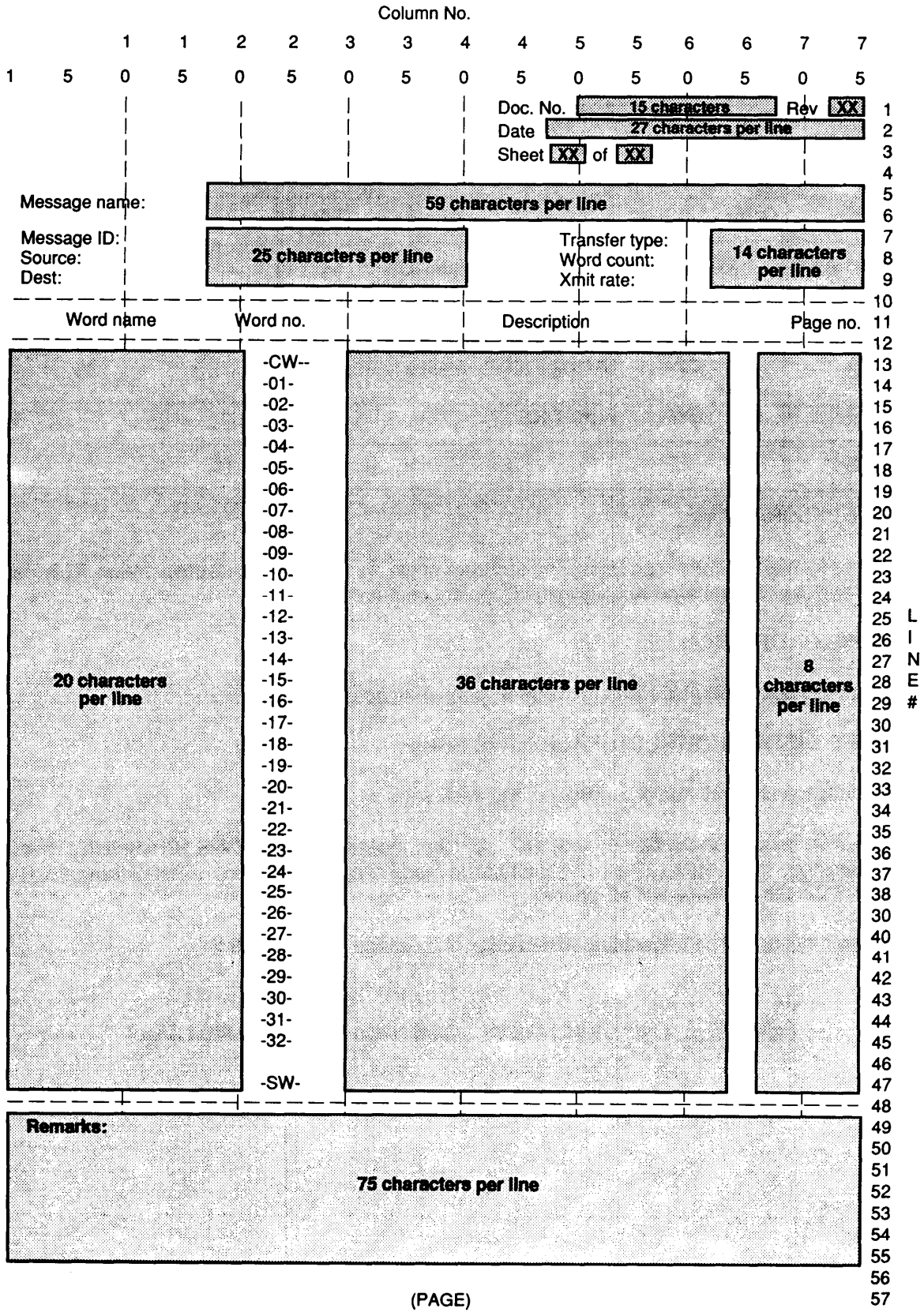


Figure 80-8. Message Format ICD Presentation Sheet

DOC. NO. STR-DD-82009-2 REV. 0
DATE January 1982
SHEET 1 OF 1

MESSAGE NAME: Manual Groundspeed and Track Angle

MESSAGE ID : HV BC-DNS 22
SOURCE : BC
DEST : DNS
TRANSFER TYPE : BC-to-RT
WORD COUNT : 2
XMIT RATE :

WORD NAME	WORD NO.	DESCRIPTION	PAGE NO.
Receive Command Word	-CW-	To DNS subaddress 22	33
Groundspeed	-01-	HV groundspeed along HV track angle	34
Track Angle	-02-	HV track angle relative to true North	35
Receive Status Word	-SW-	From DNS	36

REMARKS:

MESSAGE DESCRIPTION:

Provides for manual entry of groundspeed and track angle in the backup mode of operation. This manual entry replaces remembered velocity in the Doppler computations.

TRANSMISSION CRITERIA:

Transmitted upon operator action in the backup mode of operation.

MESSAGE FUNCTIONAL/STRUCTURAL RELATIONSHIP:

This message shall provide groundspeed and track angle of the vehicle.

The system must be in the backup mode of operation (message HV BC-DNS 16) when this message is transmitted. If the ASN-137 is not in the backup mode of operation upon receipt of message HV BC-DNS 22, the message will be ignored.

NOTE: This function will be negated upon reception of message HV BC-DNS 21.

Figure 80-9. Example of a Completed Message ICD Presentation Sheet

YYYY = Receiving terminal name (see table 80-III for examples).

SY = Receiving terminal 1553 subaddress to which the word is addressed.

The rules for MESSAGE ID construction are:

Entries in XXXX and YYYY are four characters left-justified with trailing blanks (such as “INSI”, “SMS”, “MC”). In the broadcast mode of operation, YYYY is “ALL”.

Entries in SX and SY are two numeric characters with a range of 00-31 or the characters M0 or M1. The latter characters are used in conjunction with the bus controller and the transmission of MIL-STD-1553 mode codes. M0 represents the transmission of 00000 in the subaddress/mode field of the MIL-STD-1553 command word; M1 represents the transmission of 11111 in that field. When M0 and M1 are used as either SX or SY, the numeric entry, used in conjunction with the receive/transmit terminal, will indicate the MIL-STD-1553 mode code (the data word count/mode code field of the MIL-STD-1553 command word). For example, the message ID INS 03-BC1 M0 indicates that a Mode Command Without Data Word, is being commanded by the bus controller (BC1), using 00000 (M0) as the subaddress/mode, to the INS. The mode code being commanded is Initiate Self Test (03).

SOURCE : Name of the subsystem originating the message, usually abbreviated or an acronym. When a message is modified by a subsystem, that subsystem becomes the originating source. Source information is used to allow tracking of data from the originating source to all destinations.

DEST : Name of the subsystem that will receive the message, usually abbreviated or an acronym. Destination information is used to allow tracking of data back to the originating source and to other destinations.

TRANSFER TYPE : BC-to-RT Transfer
RT-to-BC Transfer
RT-to-RT Transfer
Mode Command Without Data Word
Mode Command With Data Word (Transmit)
Mode Command With Data Word (Receive)
BC-to-RT Transfer, Broadcast
RT-to-RT Transfer, Broadcast
Mode Command Without Data Word, Broadcast
Mode Command With Data Word, Broadcast

WORD COUNT : The number of data words transmitted in this message.

XMIT RATE : The rate in times per second (Hz) that the message is transmitted.

WORD NAME : The formal name selected for this word as described in paragraph 80.2.4, Naming.

WORD NO. : Placement of the word within the message.

DESCRIPTION : A functional description of the word.

PAGE NO. : Page location of word presentation format.

REMARKS : Additional comments, i.e., Message Description, Transmission Criteria, and Message Functional/Structural Relationship (See figure 80-9).

PAGE : Page No. of the ICD.

80.3.2 General Rules for Message Construction

The following is a list of general rules for message construction developed from the message format analysis, common usage, and good engineering practice.

a. Multiple messages from a subsystem containing the same data words should have those data words in the same order.

b. Shorter messages, which contain some of the data words found in a longer message, should be a subset of the longer message with the same data word positions.

c. A header word maybe provided as the first word of the message. The header may contain message tag and subsystem mode information, including GO/NO-GO indications.

d. A validity word(s) maybe provided to indicate the validity of specific data words within a message. A validity word(s) should be positioned preceding all data words validated.

e. If used, the word sequence within a message should be as follows:

   (1) Header Word

   (2) Validity Word

   (3) Time Tag Word (defined in paragraph 80.2.5)

   (4) Other data words as required.

f. Use standard data words, defined in paragraph 80.2.5.

g. When initially assigning words to messages, leave space for later expansion. In other words, do not assign all 32 word spaces in the beginning. A recommended maximum number of words to be assigned initially is 28.

h. When assigning words to messages, do not program in spare or reserved words.

i. Data word sequences such as those shown in table 80-LII are recommended when developing messages. Sine and cosine of directional parameters should follow the same sequence.

Table 80-LII. Recommended Data Word Sequences for Message Development

Word Number (N]		
N	N + 1	N + 2
Wind Speed	Wind Direction	
Distance	Bearing	Time to Go
Velocity X	Velocity Y	Velocity Z
Direction I	Direction J	Direction K
Pitch	Roll	Yaw
Longitudinal Velocity	Lateral Velocity	Normal Velocity
Longitudinal Acceleration	Lateral Acceleration	Normal Acceleration
North	East	Down
Heading	Pitch	Roll

(This page left intentionally blank.)

Table 80-LIII. BC-to-RT Transfer, Standard Message Format

DOC. NO. * REV. *
DATE *
SHEET 1 OF *

MESSAGE NAME : BC-to-RT Transfer

MESSAGE ID : *
SOURCE : *
DEST : *

TRANSFER TYPE : BC-to-RT
WORD COUNT : *
XMIT RATE : *

WORD NAME	WORD NO.	DESCRIPTION	PAGE NO.
	-CW-		
	-01-		
	-02-		
	-03-		
	-04-		
	-05-		
	-06-		
	-07-		
	-08-		
	-09-		
	-10-		
	-11-		
	-12-		
	-13-		
	-14-		
	-15-		
	-16-		
	-17-		
	-18-		
	-19-		
	-20-		
	-21-		
	-22-		
	-23-		
	-24-		
	-25-		
	-26-		
	-27-		
	-28-		
	-29-		
	-30-		
	-31-		
	-32-		
	-SW-		

REMARKS: * - Application Dependent

Table 80-LIV. RT-to-BC Transfer, Standard Message Format

DOC. NO. * REV. *
DATE *
SHEET 1 OF *

MESSAGE NAME : RT-to-BC Transfer

MESSAGE ID : *
SOURCE : *
DEST : *

TRANSFER WPE : RT-to-BC
WORD COUNT : *
XMIT RATE : *

WORD NAME	WORD NO.	DESCRIPTION	PAGE NO.
	-C W-		
	-SW-		
	-01-		
	-02-		
	-03-		
	-04-		
	-05-		
	-06-		
	-07-		
	-08-		
	-09-		
	-10-		
	-11-		
	-12-		
	-13-		
	-14-		
	-15-		
	-16-		
	-17-		
	-18-		
	-19-		
	-20-		
	-21-		
	-22-		
	-23-		
	-24-		
	-25-		
	-26-		
	-27-		
	-28-		
	-29-		
	-30-		
	-31-		
	-32-		

REMARKS: * - Application Dependent

Table 80-LV. RT-to-RT Transfer, Standard Message Format

DOC. NO. * REV. *
DATE *
SHEET 1 OF *

MESSAGE NAME : RT-to-RT Transfer

MESSAGE ID : *
SOURCE : *
DEST : *

TRANSFER TYPE : RT-to-RT
WORD COUNT : *
XMIT RATE : *

WORD NAME	WORD NO.	DESCRIPTION	PAGE NO.
	-CW-		
	-CW-		
	-SW-		
	-01-		
	-02-		
	-03-		
	-04-		
	-05-		
	-06-		
	-07-		
	-08-		
	-09-		
	-10-		
	-11-		
	-12-		
	-13-		
	-14-		
	-15-		
	-16-		
	-17-		
	-18-		
	-19-		
	-20-		
	-21-		
	-22-		
	-23-		
	-24-		
	-25-		
	-26-		
	-27-		
	-28-		
	-29-		
	-30-		
	-31-		
	-32-		
	-SW-		

REMARKS: * - Application Dependent

Table 80-LVI. Mode Command Without Data Word, Standard Message Format

DOC. NO. * REV. *
DATE *
SHEET 1 OF *

MESSAGE NAME : Mode Command Without Data Word

MESSAGE ID : *
SOURCE : *
DEST : *
TRANSFER TYPE : Mode Command
WORD COUNT : *
XMIT RATE : *

WORD NAME	WORD NO.	DESCRIPTION	PAGE NO.
	-CW-		
	-SW-		

REMARKS: * - Application Dependent

Table 80-LVII. Mode Command With Data Word (Transmit), Standard Messsage Forma

DOC. NO. REV.
DATE
SHEET 1 OF

MESSAGE NAM Mode Command With Data Word (Transmit

MESSAGE I
SOURC
DES
TRANSFER TYP Mode Comman
WORD COUN
XMIT RAT

WORD NAM	WORD NO	DESCRIPTIO	PAGE NO
	-CW		
	-SW		
	-01		

REMARKS: * - Application Dependen

Table 80-LVIII. Mode Command With Data Word (Receive), Standard Message Format

DOC. NO. * REV. *
DATE *
SHEET 1 OF *

MESSAGE NAME : Mode Command With Data Word (Receive)

MESSAGE ID : *
SOURCE : *
DEST : *

TRANSFER TYPE : Mode Command
WORD COUNT : *
XMIT RATE : *

WORD NAME	WORD NO.	DESCRIPTION	PAGE NO.
	-CW-		
	-01-		
	-SW-		

REMARKS: * - Application Dependent

Table 80-LIX. BC-to-RT Transfer, Broadcast, Standard Message Format

DOC. NO.* REV. *
DATE *
SHEET 1 OF *

MESSAGE NAME : BC-to-RT Transfer, Broadcast

MESSAGE ID : *
SOURCE : *
DEST : *

TRANSFER TYPE : Broadcast
WORD COUNT : *
XMIT RATE : *

WORD NAME	WORD NO.	DESCRIPTION	PAGE NO.
	-CW-		
	-01-		
	-02-		
	-03-		
	-04-		
	-05-		
	-06-		
	-07-		
	-08-		
	-09-		
	-10-		
	-11-		
	-12-		
	-13-		
	-14-		
	-15-		
	-16-		
	-17-		
	-18-		
	-19-		
	-20-		
	-21-		
	-22-		
	-23-		
	-24-		
	-25-		
	-26-		
	-27-		
	-28-		
	-29-		
	-30-		
	-31-		
	-32-		

REMARKS: * - Application Dependent

Table 80-LX. RT-to-RT Transfer, Broadcast, Standard Message Format

DOC. NO. * REV. *
DATE *
SHEET 1 OF *

MESSAGE NAME : RT-to-RT Transfer, Broadcast

MESSAGE ID	: *	TRANSFER TYPE :	Broadcast
SOURCE	: *	WORD COUN :	*
DEST	:	XMITRATE :	*

WORD NAME	WORD NO.	DESCRIPTION	PAGE NO.
	-CW-		
	-CW-		
	-SW-		
	-01-		
	-02-		
	-03-		
	-04-		
	-05-		
	-06-		
	-07-		
	-08-		
	-09-		
	-10-		
	-11-		
	-12-		
	-13-		
	-14-		
	-15-		
	-16-		
	-17-		
	-18-		
	-19-		
	-20-		
	-21-		
	-22-		
	-23-		
	-24-		
	-25-		
	-26-		
	-27-		
	-28-		
	-29-		
	-30-		
	-31-		
	-32-		

REMARKS: * - Application Dependent

Table 80-LXI. Mode Command Without Data Word, Broadcast, Standard Message Format

DOC. NO. * REV. *
DATE *
SHEET 1 OF *

MESSAGE NAME : Mode Command Without Data Word, Broadcast

MESSAGE ID	: *	TRANSFER TYPE	: Broadcast
SOURCE	: *	WORD COUNT	: *
DEST	: *	XMIT RATE	: *

WORD NAME	WORD NO.	DESCRIPTION	PAGE NO.
	-CW-		

REMARKS: * - Application Dependent

Table 80-LXII. Mode Command With Data Word, Broadcast, Standard Message Forma

DOC. NO. REV.
DATE
SHEET 1 OF

MESSAGE NAME: Mode Command With Data Word, Broadcas

MESSAGE I		TRANSFER TYP	Broadcas
SOURC		WORD COUN	
DES		XMIT RAT	

WORD NAM	WORD NO	DESCRIPTION	PAGE NO
	-CW -01		

REMARKS: * - Application Dependen

80.3.3 Command and Status Word ICD Presentation Format

Command and status word ICD presentation formats are shown in tables 80-LXIII through 80-LXXII and tables 80-LXXIII and 80-LXXIV, respectively. These formats, based on the data word ICD presentation formats of Tables 80-I and 80-II, are included to provide consistency and completeness in the ICD process.

A command word ICD presentation format is provided for each MIL-STD-1553 information type:

BC-to-RT Transfer
RT-to-BC Transfer
RT-to-RT Transfer
Mode Command Without Data Word
Mode Command With Data Word (Transmit)
Mode Command With Data Word (Receive)
BC-to-RT Transfer, Broadcast
RT-to-RT Transfer, Broadcast
Mode Command Without Data Word, Broadcast
Mode Command With Data Word, Broadcast

Two status word presentation formats are provided: Transmit status word and Receive status word. The two formats provide a means of distinguishing uniquely between the two status words in an RT-to-RT transfer through the use of the message ID.

(This page left intentionally blank.)

Table 80-LXIII. BC-to-RT Transfer, Standard Command Word Format

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : BC-to-RT Transfer

WORD ID : **** BC-******-RCW
XMIT RATE : *
SIGNAL TYPE : Command Word

FIELD NAME	BIT NO.		DESCRIPTION
Remote Terminal Address	-00-C	MSB	Address of receive terminal,* Legal addresses 00000-11110
	-01-C		
	-02-C		
	-03-C		
	-04-C	LSB	
T/R	-05-0		0 indicates receive
Subaddress	-06-C	MSB	Subaddress of receive terminal, * Legal subaddresses 00001-11110
	-07-C		
	-08-C		
	-09-C		
	-10-C	LSB	
Data Word Count	-11-C	MSB	Number of words to be received, * Legal range 00000-11111 00000 indicates 32 words
	-12-C		
	-13-C		
	-14-C		
	-15-C	LSB	

REMARKS: * - Application Dependent

Table 80-LXIV. RT-to-BC Transfer, Standard Command Word Format

DOC. NO.* REV. *
DATE *
SHEET 1 OF 1

WORD NAME : RT-to-BC Transfer

WORD ID : ******-**** BC-TCW
XMIT RATE : *
SIGNAL TYPE : Command Word

FIELD NAME	BIT NO.		DESCRIPTION
Remote Terminal Address	-00-C	MSB	Address of transmit terminal, * Legal addresses 00000-11110
	-01-C		
	-02-C		
	-03-C		
	-04-C	LSB	
T/R	-05-1		1 indicates transmit
Subaddress	-06-C	MSB	Subaddress of transmit terminal, * Legal subaddresses 00001-11110
	-07-C		
	-08-C		
	-09-C		
	-10-C	LSB	
Data Word Count	-11-C	MSB	Number of words to be transmitted, * Legal range 00000-11111 00000 indicates 32 words
	-12-C		
	-13-C		
	-14-C		
	-15-C	LSB	

REMARKS: * - Application Dependent

Table 80-LXV. RT-to-RT Transfer, Standard Command Word Format

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : RT-to-RT Transfer

WORD ID : ******-******-RTCW
XMIT RATE : *
SIGNAL TYPE : Command Word

FIELD NAME	BIT NO.		DESCRIPTION
Remote Terminal Address	MSW -00-C	MSB	
	-01-C		Address of receive terminal, *
	-02-C		Legal addresses 00000-11110
	-03-C		
	-04-C	LSB	
T/R	-05-0		0 indicates receive
Subaddress	-06-C	MSB	
	-07-C		Subaddress of receive terminal, *
	-08-C		Legal subaddresses 00001-11110
	-09-C		
	-10-C	LSB	
Data Word Count	-11-C	MSB	Number of words to be received,
	-12-C		Note 1, *
	-13-C		Legal range 00000-11111
	-14-C		00000 indicates 32 words
	-15-C	LSB	
Remote Terminal Address	LSW -00-C	MSB	
	-01-C		Address of transmit terminal, *
	-02-C		Legal addresses 00000-11110
	-03-C		
	-04-C	LSB	
T/R	-05-1		1 indicates transmit
Subaddress	-06-C	MSB	
	-07-C		Subaddress of transmit terminal, *
	-08-C		Legal subaddresses 00001-11110
	-09-C		
	-10-C	LSB	
Data Word Count	-11-C	MSB	Number of words to be transmitted,
	-12-C		Note 1,*
	-13-C		Legal range 00000-11111
	-14-C		00000 indicates 32 words
	-15-C	LSB	

REMARKS: * - Application Dependent

Note 1: Data word count fields must be identical.

Table 80-LXVI. Mode Command Without Data Word, Standard Command Word Format

DOC. NO. * REV. *
DATE *
SHEET 1 OF 2

WORD NAME : Mode Command Without Data Word

WORD ID : ******-****M*-MCCW
XMIT RATE : *
SIGNAL TYPE : Command Word

FIELD NAME	BIT NO.	DESCRIPTION
Remote Terminal Address	-00-C	MSB
	-01-C	Address of transmit terminal, *
	-02-C	Legal addresses 00000-11110
	-03-C	
	-04-C	LSB
T/R	-05-1	1 indicates transmit
Mode	-06-C	MSB
	-07-C	Indicates the contents of the mode code field are to be decoded as a five-bit mode code.
	-08-C	Legal values 00000, 11111, Note 1
	-09-C	
	-10-C	LSB
Mode Code	-11-C	MSB
	-12-C	MIL-STD-1553B mode code
	-13-C	Legal values, Note 2
	-14-C	
	-15-C	LSB

REMARKS: * - Application Dependent

Note 1: Code 00000 should not be used for any system that uses the status word's instrumentation bit (bit 06).

Table 80-LXVI. Mode Command Without Data Word, Standard Command Word Format (Continued)

DOC. NO. * REV. *
DATE *
SHEET 2 OF 2

WORD NAME : Mode Command Without Data Word

Note 2: Refer to Notice 2 (if applicable) for required mode codes

00000- Dynamic Bus Control
00001- Synchronize
00010- Transmit Status Word
00011- Initiate Self Test
00100- Transmitter Shutdown
00101- Override Transmitter Shutdown
00110- Inhibit Terminal Flag Bit
00111- Override Inhibit Terminal Flag Bit
01000- Reset Remote Terminal

Table 80-LXVII. Mode Command With Data Word (Transmit), Standard Command Word Format

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Mode Command With Data Word (Transmit)
WORD ID : *****-****M*-MCCDT
XMIT RATE : *
SIGNAL IYPE : Command Word

FIELD NAME	BIT NO.		DESCRIPTION
Remote Terminal Address	-00-C	MSB	Address of transmit terminal, l Legal addresses 00000-11110
	-01-C		
	-02-C		
	-03-C		
	-04-C	LSB	
T/R	-05-1		1 indicates transmit
Mode	-06-C	MSB	Indicates the contents of the mode code field are to be decoded as a five-bit mode code. Legal values 00000,11111, Note 1
	-07-C		
	-08-C		
	-09-C		
	-10-C	LSB	
Mode Code	-11-C	MSB	MIL-STD-1553B mode code Legal values, Note 2, l
	-12-C		
	-13-C		
	-14-C		
	-15-C	LSB	

REMARKS: * - Application Dependent

Note 1: Code 00000 should not be used for any system that uses the status word's instrumentation bit (bit 06).

Note 2: 10000- Transmit Vector Word
10010- Transmit Last Command
10011- Transmit BIT Word

Table 80-LXVIII. Mode Command With Data Word (Receive), Standard Command Word Format

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Mode Command With Data Word (Receive)

WORD ID : **** M*-******-MCCDR
XMIT RATE : *
SIGNAL TYPE : Command Word

FIELD NAME	BIT NO.		DESCRIPTION
Remote Terminal Address	-00-C	MSB	
	-01-C		Address of receive terminal, *
	-02-C		Legal addresses 00000-11110
	-03-C		
	-04-C	LSB	
T/R	-05-0		0 indicates receive
Mode	-06-C	MSB	
	-07-C		Indicates the contents of the mode code field are to be decoded as
	-08-C		a five-bit mode code.
	-09-C		Legal values 00000, 11111, Note 1
	-10-C	LSB	
Mode Code	-11-C	MSB	
	-12-C		MIL-STD-1553B mode code
	-13-C		Legal values, Note 2, *
	-14-C		
	-15-C	LSB	

REMARKS: * - Application Dependent

Note 1: Code 00000 should not be used for any system that uses the status word's instrumentation bit (bit 06).
Note 2: 10001- Synchronize
10100- Selected Transmitter Shutdown
10101- Override Selected Transmitter Shutdown

Table 80-LXIX. BC-to-RT Transfer, Broadcast, Standard Command Word Format

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : BC-to-RT Transfer, Broadcast

WORD ID : ****BC-ALL**-BCCW
XMIT RATE : *
SIGNAL TYPE : Command Word

FIELD NAME	BIT NO.		DESCRIPTION
Remote Terminal Address	-00-1	MSB	
	-01-1		
	-02-1		11111 indicates broadcast
	-03-1		
	-04-1	LSB	
T/R	-05-0		0 indicates receive
Subaddress	-06-C	MSB	
	-07-C		Subaddress of receive terminals, *
	-08-C		Legal subaddresses 00001-11110
	-09-C		
	-10-C	LSB	
Data Word Count	-11-C	MSB	
	-12-C		Number of words to be received, *
	-13-C		Legal range 00000-11111
	-14-C		00000 indicates 32 words
	-15-C	LSB	

REMARKS: * - Application Dependent

Table 80-LXX. RT-to-RT Transfer, Broadcast, Standard Command Word Format

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : RT-to-RT Transfer, Broadcast

WORD ID : ******-ALL**-BCCRT
XMIT RATE : *
SIGNAL TYPE : Command Word

FIELD NAME		BIT NO.		DESCRIPTION
Remote Terminal Address	MSW	-00-1	MSB	
		-01-1		
		-02-1		11111 indicates broadcast
		-03-1		
		-04-1	LSB	
T/R		-05-0		0 indicates receive
Subaddress		-06-C	MSB	
		-07-C		Subaddress of receive terminals, *
		-08-C		Legal subaddresses 00001-11110
		-09-C		
		-10-C	LSB	
Data Word Count		-11-C	MSB	Number of words to be received,
		-12-C		Note 1, *
		-13-C		Legal range 00000-11111
		-14-C		00000 indicates 32 words
		-15-C	LSB	
Remote Terminal Address	LSW	-00-C	MSB	
		-01-C		Address of transmit terminal, *
		-02-C		Legal addresses 00000-11110
		-03-C		
		-04-C	LSB	
T/R		-05-1		1 indicates transmit
Subaddress		-06-C	MSB	
		-07-C		Subaddress of transmit terminal, *
		-08-C		Legal subaddresses 00001-11110
		-09-C		
		-10-C	LSB	
Data Word Count		-11-C	MSB	Number of words to be transmitted, -
		-12-C		Note 1,*
		-13-C		Legal range 00000-11111
		-14-C		00000 indicates 32 words
		-15-C	LSB	

REMARKS: * - Application Dependent

Note 1: Data word count fields must be identical.

Table 80-LXXI. Mode Command Without Data Word, Broadcast, Standard Command Word Format

DOC. NO. * REV. *
DATE *
SHEET 1 OF 2

WORD NAME : Mode Command Without Data Word, Broadcast

WORD ID : ALL**BCM*-BCMC
XMIT RATE : *
SIGNAL TYPE : Command Word

FIELD NAME	BIT NO.		DESCRIPTION
Remote Terminal Address	-00-1	MSB	
	-01-1		
	-02-1		11111 indicates broadcast
	-03-1		
	-04-1	LSB	
T/R	-05-1		1 indicates transmit
Mode	-06-C	MSB	
	-07-C		Indicates the contents of the mode code field are to be decoded as a five-bit mode code. Legal values 00000,11111, Note 1
	-08-C		
	-09-C		
	-10-C	LSB	
Mode Code	-11-C	MSB	
	-12-C		MIL-STD-15536 mode code, * Legal values, Note 2
	-13-C		
	-14-C		
	-15-C	LSB	

REMARKS: * - Application Dependent

Note 1: Code 00000 should not be used for any system that uses the status word's instrumentation bit (bit 06).

Table 80-LXXI. Mode Command Without Data Word, Broadcast, Standard Command Word Format (Continued)

DOC. NO. * REV. *
DATE *
SHEET 2 OF 2

WORD NAME : Mode Command Without Data Word, Broadcast

Note 2: Refer to Notice 2 (if applicable) for required mode codes

00001- Synchronize
00011- Initiate Self Test
00100- Transmitter Shutdown
00101- Override Transmitter Shutdown
00110- Inhibit Terminal Flag Bit
00111- Override Inhibit Terminal Flag Bit
01000- Reset Remote Terminal

Table 80-LXXII. Mode Command With Data Word, Broadcast, Standard Command Word Format

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Mode Command With Data Word, Broadcast

WORD ID : BC M*-ALL**-BCMCD
XMIT RATE : *
SIGNAL TYPE : Command Word

FIELD NAME	BIT NO.	DESCRIPTION
Remote Terminal Address	-00-1	MSB
	-01-1	
	-02-1	11111 indicates broadcast
	-03-1	
	-04-1	LSB
T/R	-05-0	0 indicates receive
Mode	-06-C	MSB
	-07-C	Indicates the contents of the mode code field are to be decoded as a five-bit mode code.
	-08-C	Legal values 00000, 11111, Note 1
	-09-C	
	-10-C	LSB
Mode Code	-11-C	MSB
	-12-C	MIL-STD-15536 mode code, * Legal values, Note 2
	-13-C	
	-14-C	
	-15-C	LSB

REMARKS: * - Application Dependent

Note 1: Code 00000 should not be used for any system that uses the status word's instrumentation bit (bit 06).
Note 2: 10001- Synchronize
10100- Selected Transmitter Shutdown
10101- Override Selected Transmitter Shutdown

Table 80-LXXIII. Receive, Standard Status Word Format

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NAME : Status Word, Receive

WORD ID : ******-******-RSW
XMIT RATE : *
SIGNAL TYPE : Status Word

FIELD NAME	BIT NO.	DESCRIPTION
Remote Terminal Address	-00-C MSB	Address of receive terminal, * Legal addresses 00000-11111 11111 indicates broadcast
	-01-C	
	-02-C	
	-03-C	
	-04-C LSB	
Message Error	-05-D	1 indicates message error
Instrumentation	-06-0	Always set to zero
Service Request	-07-D	1 indicates service requested, Note 1
Reserved	-08-0 MSB	Always set to 000
	-09-0	
	-10-0 LSB	
Broadcast Command Received	-11-D	1 indicates preceding valid command word was a broadcast command, Notes 1 & 2
Busy	-12-D	1 indicates subsystem is busy, Note 1
Subsystem Flag	-13-D	1 indicates a subsystem fault condition, Note 1
Dynamic Bus Cont. Acceptance	-14-D	1 indicates acceptance of control, Note 1
Terminal Flag	-1 5-D	1 indicates a terminal fault condition, Note 1

REMARKS: * - Application Dependent

Note 1: Set to zero if not implemented. Refer to Notice 2 (if applicable) for required status bits.
Note 2: This bit can only be set to logic one in a Transmit Last Command Word mode code or Transmit Status Word mode code.

Table 80-LXXIV. Transmit, Standard Status Word Format

DOC. NO. * REV. *
DATE *
SHEET 1 OF 1

WORD NBAME: Status Word, Transmit

WORD ID : ******-******-TSW
XMIT RATE : *
SIGNAL TYPE : Status Word

FIELD NAME	BIT NO.	DESCRIPTION
Remote Terminal Address	-00-C	MSB
	-01-C	Address of transmit terminal, *
	-02-C	Legal addresses 00000-11110
	-03-C	
	-04-C	LSB
Message Error	-05-D	1 indicates message error
Instrumentation	-06-0	Always set to zero
Service Request	-07-D	1 indicates service requested, Note 1
Reserved	-08-0	MSB
	-09-0	Always set to 000
	-10-0	LSB
Broadcast Command Received	-11-0	Always set to zero.
Busy	-12-D	1 indicates subsystem is busy, Note 1
Subsystem Flag	-13-D	1 indicates a subsystem fault condition, Note 1
Dynamic Bus Cont. Acceptance	-14-D	1 indicates acceptance of control, Note 1
Terminal Flag	-15-D	1 indicates a terminal fautt condition, Note 1

REMARKS: * - Application Dependent

Note 1: Set to zero if not implemented. Refer to Notice 2 (if applicable) for required status bits.

SECTION 80 INDEX

SECTION 90

COMPARISON OF MIL-STD-1553B VERSIONS AND NOTICES

CONTENTS

FIGURES

TABLES

90. COMPARISON OF MIL-STD-1553 VERSIONS AND NOTICES

This section compares the versions and notices of MIL-STD-1553A, MIL-STD-1553B, Notice 1 to MIL-STD-1553B, and Notice 2 to MIL-STD-1553B MIL-STD-1553. Table 90-I presents the 1553 requirement for each of the versions. The far right column, "Note," refers to the numbers of the text notes, which are detailed discussions of the differences among applicable versions of the 1553 requirements. Table 90-I is a complete list of the differences.

Table 90-II then lists several practical and important problem areas associated with integrating a terminal designed using one version of 1553 into a system designed using another version of 1553. This table also refers to the numbers of the text notes in section 90.

Note 1. Starting with 1553A, interface electronics components previously known as a multiplex terminal unit (MTU) and a subsystem interface unit (SSIU) were no longer defined separately. They were combined into a single component called a remote terminal (RT).

Note 2. In 1553A, the list of documents that forma part of the standard changed as follows:

a. MIL-STD-442 (Aerospace Telemetry Standards) was deleted.

b. MIL-STD-462 (Electromagnetic Interference Characteristics, Measurement of) was added.

Note 3. In 1553B, the list of documents that forma part of the standard changed as follows:

a. MIL-STD-461 (Electromagnetic Interference Characteristics, Requirements for Equipment) was deleted.

b. MIL-STD-462 (Electromagnetic Interference Characteristics, Measurement of) was deleted.

Note 4. In 1553B, several revised and new definitions were introduced and were presented in a different order.

Note 5. Starting with 1553A, a remote terminal (RT) may exist as a separate line replaceable unit (LRU) or be contained (i.e., embedded) within a subsystem.

Note 6. In 1553B, the definition of remote terminal (RT) was simplified and clarified to include all terminals not operating as the bus controller (BC) or as a (newly defined) bus monitor (BM).

Note 7. The idea of dynamic bus allocation was introduced in 1553A, renamed dynamic bus control (but not substantially changed) in 1553B.

Note 8. A word was defined in 1553A as a sequence of 16 bits plus sync and parity (for a total of 20 bits). Three types of words were specified: command, status, and data.

Note 9. A message was defined in 1553A as a transmission of words on the data bus cable. Three types of messages were defined:

a. Controller to terminal.

b. Terminal to controller.

c. Terminal to terminal.

In 1553B, the three types of messages were renamed as:

a. Bus controller (BC) to remote terminal (RT).

Table 90-I. Comparison of Data Bus Requirements (Sheet 1 of 3)

Requirements	1553A	1553B	Notice 1	Notice 2	Notes
Transmission bit rate:	1 Mbit/sec	1 Mbit/sec	1 Mbit/sec		
Short term stability	0.001%	0.01%	0.01% or 0.001%		22
Long term	0.01%	0.1%	0.1% or 0.01%		22
Mode code indicator:	00000	00000/11111	00000/11111	00000/11111	16,25,26
T/R bit for mode codes:	Not specified	No data word = 1 Data word: 1=transmit, 0=receive			
Assigned mode codes:					32
00000	Dynamic bus allocation	Dynamic bus control	Not allowed	Not allowed for AF	7,27,28
00001	Not specified	Synchronize			
00010	Not specified	Transmit status word		Required	28
00011	Not specified	Initiate self test		Additional reqmts	33
00100	Not specified	Transmitter shutdown		Required	
00101	Not specified	Override shutdown		Required	
00110	Not specified	Inhibit terminal flag bit	Not allowed	Allowed	27
00111	Not specified	Override inhibit	Not allowed	Allowed	27
01000	Not specified	Reset remote terminal		Required	28,33
01100	Not specified	Reserved			
01101	Not specified	Reserved			
01110	Not specified	Reserved			
01111	Not specified	Reserved			
10000	Not specified	Transmit vector word			
10001	Not specified	Synchronize			
10010	Not specified	Transmit last command			
10011	Not specified	Transmit bit word			
10100	Not specified	Selected transmitter shutdown	Not allowed	Allowed	27,28
10101	Not specified	Override shutdown	Not allowed	Allowed	27,28
Status word bit definitions:					40/41
Bit 9	Message error	Message error		Required	34,35,36,37,39,41,73,90
Bit 10	Status codes	Instrumentation		Always zero	34,35,38,39
Bit 11	Status codes	Service request		Optional	34,35,38,39
Bit 12	Status codes	Reserved		Always zero	34,35,38,39
Bit 13	Status codes	Reserved		Always zero	34,35,38,39
Bit 14	Status codes	Reserved		Always zero	34,35,38,39
Bit 15	Status codes	Broadcast command		If broadcast used	34,35,38,39,41,89
Bit 16	Status codes	Busy			34,35,38,39,41
Bit 17	Status codes	Subsystem flag		If have BIT	34,35,38,39,41,89
Bit 18	Status codes	Dynamic bus control acpt.		If DBC used	34,35,38,39,41,89
Bit 19	Terminal flag	Terminal flag		If have self test	34,35,38,39,41,89
Message formats:					20,42
RT to controller	Yes	Yes		Required	9,42
Controller to RT	Yes	Yes		Required	9,42
RT to RT	Yes	Yes		Required	9,42,43,51
Mode command without data	No	Yes		Required	42,44
Broadcast	No	Yes	Not allowed	Restricted	15,29,42,44
Intermessage gap time	Not specified	4 microseconds			45
Response time	2 to 5 microseconds	4 to 12 microseconds	May use max. 7 microseconds		46,47
No response time out	Not specified	14 microseconds			48
Word validation	Yes	Yes			71

Note:
T/R Transmit/receive

Table 90-I. Comparison of Data Bus Requirements (Sheet 2 of 3)

Requirements	1553A	1553B	Notice 1	Notice 2	Notes
Transmission continuity	Yes	Yes			73
Fail safe	660 microseconds	800 microseconds			74
Superseding valid command	Yes	Yes			84
Invalid data rejection	Yes	Yes			
Parity	Odd	Odd			40
Cable:					
Twists	12 twists/ft	4 twists/ft			55
Shield coverage	80%	75%	Minimum 90.0%	Minimum 90.0%	80,82,83
Characteristic impedance (Z_0)	70±10% (1 MHz)	70-85 (1 MHz)	70 - 85 (1 MHz)	70 - 85 (1 MHz)	51,56,81
Attenuation	1 dB/100 ft (1 MHz)	1.5 dB/100 ft (1 MHz)			52,57
Length	300 ft	Not specified			50
Capacitance	30 pF/ft	30 pF/ft			
Stub failure bus impedance	1.5 Z_0	1.5 Z_0			
Termination	Characteristic impedance	Characteristic impedance 2%			59
Connector	Specified	Not specified			60
RTs with transformer coupled stubs:				Use specified	62
Stub length	20 ft	20 ft			59
Stub input voltage	Not specified	1 - 14 V			67
Isolation resistor	0.75 Z_0 ± 5%	0.75 Z_0 ± 2%			63
Transformer open circuit input impedance	Not specified	3000 (75 KHz to 1 MHz)			
Cable coupling	Shielded coupler box	Minimum 75%	Minimum 90%	Minimum 75% (360)	82
Transformer turns-ratio	Not specified	1:1.41 ± 3%			87
Transformer waveform integrity:	Not specified				65
Droop group		20%			65
Overload and ringing	Not specified	1V peak			65
Transformer common mode rejection	Not specified	45 dB at 1 MHz			
Output waveform requirements:	Trapezoid	Trapezoid			
Output level	6 - 20 Vp-p	18 - 27 Vp-p			64
Output level with 1 RT fault	4.5 - 15 Vp-p	Not specified			
Max zero crossing deviation	25 ns	25 ns			
Rise or fall time	100 ns	100-300 ns			65
Max distortion	Not specified	900 mV (p, 1 to 1)			65
Output noise	10 mVp-p	14 mV RMS			66
Output symmetry	Not specified	500 mVp-p after 2.5s			
Input waveform requirements:		Square to sine wave			67
Input level	1 - 20 Vp-p (1 to1)	0.86 - 14 Vp-p (1 to1)			
Common mode rejection at RT	Not specified	10V (1 to g) (DC to 2 MHz)			

Table 90-I. Comparison of Data Bus Requirements (Sheet 3 of 3)

Requirements	1553A	1553B	Notice 1	Notice 2	Notes
Input waveform requirements: (Continued)					
Max zero crossing deviation	Not specified	150 ns			
Common mode rejection at bus	10V (1 to g) (DC to 2 MHz)	Not specified			
No response input level	Not specified	0 - 0.2 Vp-p			
Input impedance	2000	1000			70
Noise rejection (specified conditions)	1 error in 500 words	1 error in 10^7 words			68,75
Message rejection (specified conditions)	1 error in 10 messages	Not specified			68
RTs with direct coupled stubs:			Not allowed AF	Use specified	
Stub length	1 ft	1 ft			
Stub input voltage requirements	1 - 20 Vp-p	1.4 - 20 Vp-p			67
Isolation resistor	0.75 Zo ± 5%	55 ± 2%			63
Cable coupling	Shielded coupler box	Minimum 75%			
Output waveform requirements:	Trapezoid	Trapezoid			
Output level	6 - 20Vp-p (1 to 1)	6 - 9 V			64
Output level with 1 RT fault	4.5-15Vp-p	Not specified			
Max. zero crossing deviation	25 ns	25 ns			
Rise or fall time	100 ns	100 - 300 ns			65
Max. distortion	Not specified	300 mV (peak, 1 to 1)			65
Output noise	10 mVp-p	5 mV RMS			66,86
Output symmetry	Not specified	180 mVp-p after 2.5 µs			
Input waveform requirements:	Square to sine wave	Square to sine wave			67
Input level	1-20Vp-p (1 to 1)	1.2 - 20Vp-p (1 to 1)			
Common mode rejection	10V (1 to g)(DC to 2 MHz)	10V (1 to g)(DC to 2 MHz)			
Max. zero crossing deviation	Not specified	150 ns			
No response input level	Not specified	0.28V			
Input impedance	2000	2000			70
Noise rejection (specified conditions)	1 error in 500 words	1 error in 10^7 words			68,75
Message rejection (specified conditions)	1 error in 10 messages	Not specified			68
Dual redundant bus	Not specified	Optional	Required	Required	14
Electrical insulation	Not specified	45 dB			
Unique address for RTs	Yes	Yes		Implementation	30
Data wrap-around	No	No	No	Required	31
RT to RT validation	Nc	No	No	Required	49
Connector polarity	No	No	No	Specified	85
Power on/off noise	No	No	No	Specified	86

Table 90-//. Major Considerations of 1553 Versions

System / Terminal	1553A	1553B	1553B Notice 1	1553B Notice 2
1553A		Coupling ratio 87 Status word 35, 36 Mode code indicator 25, 26 Message error bit 90	Coupling ratio 87 Status word 25, 36 Mode code indicator 25, 26 Message error bit 90	Coupling ratio 87 Status word 35, 36 Mode code indicator 25, 26 Message error bit 90
1553B	Response time 46 Coupling ratio 87		Bus controller 88 RTs with only direct coupled stubs not allowed	Bus controller 88
1553B Notice 1	Intermessage gap 45 Response time 46, 47 Coupling ratio 87	Mode codes 27 Bus controller 88		Bus controller 88
1553B Notice 2	Intermessage gap 45 Response time 46, 47 Coupling ratio 87 RT-RT validation 49	Mode codes 28, 33 Bus controller 88 Status word, 89	Bus controller 88 Status word, 89	

Numbers in the cells are notes in this section.

b. RT to BC.

c. RT to RT.

Both 1553A and 1553B referred to a single message as the transmission of a command word, a status word, and data words. However, 1553B went on to specify the inclusion of two command words, two status words, and data words in the case of an RT to RT transmission.

Note 10. In 1553B, subsystem was defined as the device or functional unit receiving data transfer service from the data bus. This term was not previously defined.

Note 11. A data bus was defined initially in 1553A as a single, twisted, shielded pair cable. In 1553B, the definition was expanded to include all the hardware required to provide a single data path between the bus controller and all the associated remote terminals (RT) (i.e., twisted, shielded pair cables, isolation resistors, transformers, etc.).

Note 12. In 1553B, a terminal was defined as the electronic module necessary to allow the data bus to interface with the subsystem and the subsystem with the data bus. This term was not previously defined. Also, 1553B allowed terminals to exist as separate LRUS or to be contained within subsystems.

Note 13. Acontroller was defined initially in 1553A as a unit, either programmable or controlled by a processor, that serves the function of commanding, scanning, and monitoring bus traffic. In 1553B, parts of the function were allocated to two types of components, the bus controller (BC) and the bus monitor (BM). In 1553B, a BC was defined as the terminal assigned the task of initiating (i.e., commanding) information transfers on the data bus. However, to perform this task, a BC needs also to scan and monitor the bus traffic, including RT-to-BC and RT-to-RT messages. Therefore, the function of a 1553B BC is fully equivalent to that of a 1553A controller. (In fact, the terms “controller” and “bus controller” were used interchangeably in the text of 1553A.) In 1553B, a BM is defined as the terminal assigned the task of receiving bus traffic and extracting selected information to be used at a later time; this is equivalent to the scanning and monitoring part of the 1553A controller function.

Note 14. In 1553B a redundant data bus was defined as the use of more than one data bus to provide more than one data path among subsystems. This term was not previously defined.

Note 15. In 1553B, broadcast was defined as operation of a data bus system such that information transmitted by the BC or an RT is addressed to more than one of the RTs connected to the data bus. This term was not previously defined.

Note 16. In 1553B, mode code was defined as a means by which the BC can communicate with hardware related to the multiplex bus to assist in managing the information flow. This term was not previously defined.

Note 17. Several paragraphs were added, changed, and renumbered in the requirements section of 1553B compared to 1553A. The information in section 4, "Requirements," of 1553A was divided into two sections in 1553B: section 4, "General requirements," and section 5, "Detail requirements," to comply with the format established for military standards. However, only general requirements are contained in 1553B; section 5 is labeled "not applicable."

Note 18. In 1553B, it was specified that all of the general requirements shall be valid over the environmental conditions in which the multiplex data bus system is required to operate.

Note 19. In 1553B, the reference to the electromagnetic compatibility (EMC) requirements of MIL-E-6051 was moved to paragraph 4.5.1.5.3, and the reference to the electromagnetic interference (EMI) requirements of MIL-STD-461 was deleted.

Note 20. In 1553B, the preliminary identification of the three modes of information transfer, and the reference to their description in subsequent paragraphs, were deleted. This information is contained in 4.3.3.6, "Message formats," in 1553B.

Note 21. Permission for bit packing of multiple quantities in a single data word was introduced in 1553B.

Note 22. The long- and short-term stability of the individual clocks used to transmit encoded data have been relaxed in 1553B. The order of magnitude reduction in transmission bit rate stability allows for selecting multiplex bus interface clocks that can meet the long shelf life requirements of some weapons. Notice 1 suggests that avionics designed for Air Force applications may be required to interface with existing avionic systems that were designed per 1553A, so the stability in this version should be used. There is no problem in using the tighter stability specified in 1553A.

Note 23. In 1553A, a total word size (including the sync waveform and the parity bit) of 20 bit times was specified.

Note 24. In 1553A, two separate graphs were added to figure 2 of 1553A to represent the 1 -MHz clock and nonreturn-to-zero (NRZ) data.

Note 25. In 1553A, the optional use of the code 00000 in the subaddress/mode field of the command word was allowed to signify that the contents of the data word count field are to be decoded as a five-bit mode command (also known as mode code). The mode code of 00000 in the word count field was reserved for dynamic bus allocation (Interchanged to dynamic bus control in 1553B) when used with this option. The data word count field was renamed the data word count/mode code field in 1553B to reflect this option.

Note 26. In 1553A, it specified that all zeros (00000) be used in the subaddress/mode field of the command word for mode codes. In 1553B it was specified that all 0's (00000) or all 1's (11111) be used. Notice 1 suggests that the capability to respond to both all 0's (00000) and all 1's (11111) be used. Notice 2 requires that a BC be capable of issuing, and an RT be capable of responding, to both subaddress/mode codes 00000 and 11111. The same notice further specified that the subaddress/mode codes 00000 and 11111 will not convey different information.

The number of assigned (i.e., not reserved) mode codes was increased to 32 to standardize the means by

which information transfers on the data bus would be controlled. If a 1553A remote terminal (RT) is used on a 1553B system, the bus controller (BC) software would have to be modified to either not send the mode codes to that RT or use the mode codes in the way that particular RT implemented them.

Note 27. Notice 1 to 1553B prohibited the transmission of five of the 32 assigned mode codes by bus controllers (BC), but allowed their implementation in remote terminals (RT), in Air Force avionic applications. The five prohibited mode codes correspond to the following functions:

a. Dynamic bus control.

b. Inhibit terminal flag bit.

c. Override inhibit terminal flag bit.

d. Selected terminal shutdown.

e. Override selected terminal shutdown.

Note 28. Notice 2 to 1553B required that remote terminals (RT) implement the mode codes for the following four functions as a minimum:

a. Transmit status word.

b. Transmitter shutdown.

c. Override transmitter shutdown.

d. Reset remote terminal.

The same notice required that bus controllers (BC) have the capability to implement all of the 32 mode codes defined in 1553B but (reiterating part of the mode code restriction from Notice 1) specified that, for Air Force applications, the mode code for dynamic bus control shall never be issued by the BC.

Note 29. In 1553B, 11111 (decimal address 31) was established as the broadcast address. Notice 1 prohibited the transmission of the broadcast command. Notice 2 limited the transmission of broadcast commands to the mode codes allowed in table 90-111.

Note 30. Notice 2 to 1553B established specific requirements for remote terminal (RT) addresses, including the requirement that all RTs be capable of being assigned any unique address from decimal address 0 (00000) through decimal address 30 (11110), established through an external connector.

Note 31. Notice 2 to 1553B identified 11110 (decimal address 30) as the desired wraparound receive and transmit subaddress.

Note 32. In 1553B, the procedures were defined and certain restrictions were established for use of the assigned optional mode codes (see list in table I of 1553B).

Note 33. Notice 2 to 1553B provided more detailed requirements for use of the optional initiate self-test and reset remote terminal mode codes for which the general procedures were initially defined in 1553B. The remote terminal (RT) is to reset within 5.0 ms and complete the self-test function within 100.0 ms.

Note 34. In 1553A, the names of some fields of the status word were changed as follows:

Table 90-III. MIL-STD-1553B, Notice 1, and Notice 2 Mode Codes

T/R BIT	1553B mode code	Function	Data word	Broadcast allowed	Notice 1 prohibits use	Notice 2 requires use
1	00000	Dynamic bus control	No	No	Yes	No
1	00001	Synchronize	No	Yes	No	No
1	00010	Transmit status word	No	No	No	Yes
1	00011	Initiate self-test	No	Yes	No	No
1	00100	Transmitter shutdown	No	Yes	No	Yes
1	00101	Override transmitter shutdown	No	Yes	No	Yes
1	00110	Inhibit terminal flag bit	No	Yes	Yes	No
1	00111	Override inhibit termimal flag	No	Yes	Yes	No
1	01000	Reset remote terminal	No	Yes	No	Yes
1	10000	Transmit vector word	Yes	No	No	No
0	10001	Synchronize	Yes	Yes	No	No
1	10010	Transmit last command	Yes	No	No	No
1	10011	Transmit BIT word	Yes	No	No	No
0	10100	Selected transmitter shutdown	Yes	Yes	Yes	No
0	10101	Override selected shutdown	Yes	Yes	Yes	No

Bit Times	Old (1553) Field Name	New (1553A) Field Name
9	Parity error (P/E)	Message error (ME)
10-18	MTU failure code	Status code
19	SSIU status indicator	Terminal flag bit

Note 35. The use of a status word is required by the standard. However, 1553B defines procedures for the use of bit times 9 through 19 in the status word, while 1553A only defines the message error and terminal flag bits and bits 10 through 18 for user-defined status codes. The purpose of defining the bits in the status word is to maintain commonality among terminals. If a 1553A terminal is used on a 1553B bus, the bus controller (BC) software may have to be modified to handle the different information conveyed by the status word bits. Notice 2 specifies which bits are to be used.

Note 36. In 1553A, additional criteria were specified to be used by a remote terminal (RT) to test the validity of incoming signals. In addition to the simple parity check that was previously required by 1553, 1553A required each word to begin with a valid sync field, to have all bits in a valid Manchester II code, and to have 16 bits plus parity in the information field. To reflect the expanded validation criteria, 1553A renamed the field at bit time 9 in the status word to “message error (ME).”

Note 37. In 1553B, it was required that the message error bit be used to indicate that a data word received from the bus controller (BC) has failed to pass the remote terminal (RT) validity tests (as previously specified in 1553A) or has failed to meet either of the newly specified conditions of transmission continuity and terminal

address validity. In 1553B, it was also specifically required that all RTs implement the message error bit, and this requirement was reiterated by Notice 2 to 1553B.

Note 38. The nine bits comprising the status codes plus the single terminal flag bit (bit times 10 to 19, inclusive) of the 1553A status word are roughly equivalent to the 10 status bits (also bit times 10 through 19) of the 1553 status word. The main difference is in the meaning of the last bit in this group (i.e., the terminal flag bit).

Note 39. In 1553B, the procedures for use of bit times 9 through 19 in the status word were defined.

Note 40. In 1553B, the wording describing the position of the parity bit in the status word was changed from 'the last bit" to "the least significant bit." This does not represent an actual change in the format of the status word because the least significant bit is the last bit (see 4.3.2 of 1553B).

Note 41. In 1553B, the status word reset requirement was introduced.

Note 42. In 1553B, the illustration of message formats was expanded from one figure to two figures, including the new broadcast information format. In 1553B, it was also stipulated that no message formats, other than those defined in 1553B, shall be used on the bus. More specific requirements for nonbroadcast message formats were provided in Notice 2 to 1553B. Notice 2 also required the implementation of RT-to-BC, BC-to-RT, and RT-to-RT data transfers, plus certain mode codes without data words.

Note 43. In 1553B, the description of RT-to-RT transfers was clarified.

Note 44. In 1553B, several paragraphs detailing use of mode commands and the optional broadcast command were added. More information on use of the broadcast command was provided in 1553B in appendix 10.6. Also see Note 25.

Note 45. In 1553B, the response time requirements were expanded by specifying a minimum intermessage gap time of 4.0 μs. The purpose was to clearly identify that the bus controller (BC) shall not transmit contiguous messages (must have a gap) and that the maximum response time does not apply to gaps between messages. The BC may issue messages with a gap time greater than 4 μs. If a 1553B remote terminal (RT) is designed to check for this gap, then there would be a problem using it with a 1553A BC with a gap less than 4 μs.

Note 46. In 1553B, the response time changed from 2.0 to 5.0 μs (1553A) to 4.0 to 12.0 ps (1553B) and identified the point of measurement to establish the time. The measurement technique was undefined in 1553A and, because it is difficult to determine precisely when the multiplex line is quiet, the measurement was specified to be from the previous midbit (zero) crossing to the next midbit crossing. Remote terminals (RT) with a 2.0-to 5.0- μs response time (1553A) will work in a system that requires a 4.0- to 12.0- μs response time (1553B). A 1553B RT, however, will not work in a system that requires a 2.0-to5.0- μs response time (1553A). This presents a problem when a new subsystem built to 1553B is to be used in a 1553A system. For this reason, Notice 1 suggests that the designer use the response time of 1553A.

Note 47. Notice 1 to 1553B suggested that "the designer may wish . . ." to restrict the maximum response time to 7.0 μs.

Note 48. In 1553B, the minimum time that a bus controller (BC) shall wait before concluding that the remote terminal (RT) is not going to respond as requested was clarified.

Note 49. Notice 2 to 1553B defined additional criteria for RT-to-RT message validation, requiring the receiving RT to count the message as invalid if the first data word is received after 57.0 ±3.0 μs

It is also recommended that the receiving RT of an RT to RT transfer verify the proper occurrence of the transmit command word and status word as specified in 4.3.3.6.3 of 1553.

Note 50. In 1553A, the maximum allowable wire-to-wire distributed capacitance of the two-conductor, twisted, shielded, jacketed cable (i.e., the data bus) was reduced from 50 to 30.0 pF/ft. In 1553A, the following requirements were also added:

a. That the cable be formed with not less than one twist per inch.

b. That the cable shield provide a minimum of 80% coverage.

Note 51. In 1553A, the required characteristic impedance of the data bus was changed from "between 64 ohms and 85 ohms at a frequency of 1.0 MHz" to "70 ohms ± 10% (i.e., between 63 ohms and 77 ohms) at a sinusoidal frequency of 1.0 MHz." Minor variations from the specified cable impedance do not significantly affect the system performance; however, a lower impedance could cause a change in waveform characteristics and amplitude.

Note 52. In 1553A, the distinction was removed between systems with cable lengths of less than 100 ft (where the cable loss specified by 1553 was 2dB/100 ft or less) and systems with cable lengths of greater than 100 ft (where the cable loss specified by 1553 was 1 dB/100 ft or less). The cable loss as specified by 1553A became 1 dB/100 ft or less, regardless of cable length.

Note 53. In 1553A, the requirement was removed that the lengths of redundant cables carrying redundant data be within 25% of each other. In 1553B, the reference to cable length was removed entirely, effectively eliminating the maximum cable length limitation of 300 ft that was previously specified by both 1553 and 1553A.

Note 54. In 1553B, the current version of most of the transmission line requirements (previously contained in paragraph 4.2.4 of 1553 and 1553A) was provided in new paragraph 4.5.1, "Data bus characteristics."

Note 55. In 1553B, the minimum required number of twists per foot of cable was decreased from twelve to four and defined a twist as a 360-degree rotation of the wire pairs. In 1553B, the required coverage by the cable shield was also reduced from 80% to 75%. The characteristics of the twisted, shielded pair cable have been relaxed in 1553B to allow selection of cable types from a variety of manufacturers. It has shown that minor variations from the specified cable characteristics do not significantly affect system performance.

Note 56. In 1553B, the specified characteristic impedance of the data bus were raised from "70 ohms ± 10%" to a "nominal characteristic impedance . . . within the range of 70.0 ohms to 85.0 ohms" at a sinusoidal frequency of 1.0 MHz.

Note 57. In 15536, the specific cable loss limit was relaxed from 1 dB/100 ft or less to 1.5 dB/100 ft or less.

Note 58. The requirements contained in 1553 for termination of the cable shield to air vehicle ground, and for insulation resistance, were not carried over to 1553A or 1553B.

Note 59. In 1553B, a ±2.0% tolerance was added to the cable termination resistance and it was specified in terms of the cable nominal characteristic impedance. In addition, whereas both 1553 and 1553A proscribed the use of cable stubs more than 20 ft long, 1553B allowed (but still discouraged) it.

Note 60. In 1553A, specific hardware requirements were introduced (covering the shielded coupler box, connector plug, and connector receptacle) for all connections to the data bus. These requirements were not carried over to 1553B.

Note 61. The electromagnetic compatibility (EMC) requirements of MIL-E-6051 were referenced in 1553, 1553A, and 1553B. These requirements were applied to "all elements of the data bus" in 4.1 of 1553 and 1553A, and they were applied to "wiring and cabling" in 4.2.4.7 of 1553A and in 4.5.1.5.3 of 1553B.

Note 62. The "coupling-transformer" mentioned in the description of the terminal-to-bus interface configuration in 4.2.5.1 of 1553, was renamed "DC isolation/coupling transformer" in 4.2.5.1 of 1553A. It was changed back to "coupling transformer" in 4.5.1.5.1.1 of 1553B.

The differences in cable coupling requirements between 1553A and 1553B can be seen by comparing figures 90-1 and 90-2. The major differences in requirements are the placement of the isolation resistors for the direct-coupled (short-stub) connection and the characterization of the coupling transformer in the transformer-coupled (long-stub) connection. With the isolation resistors located in the terminal for the direct-coupled case, a separate coupler box is not needed as long as a reliable shielded splice can be maintained.

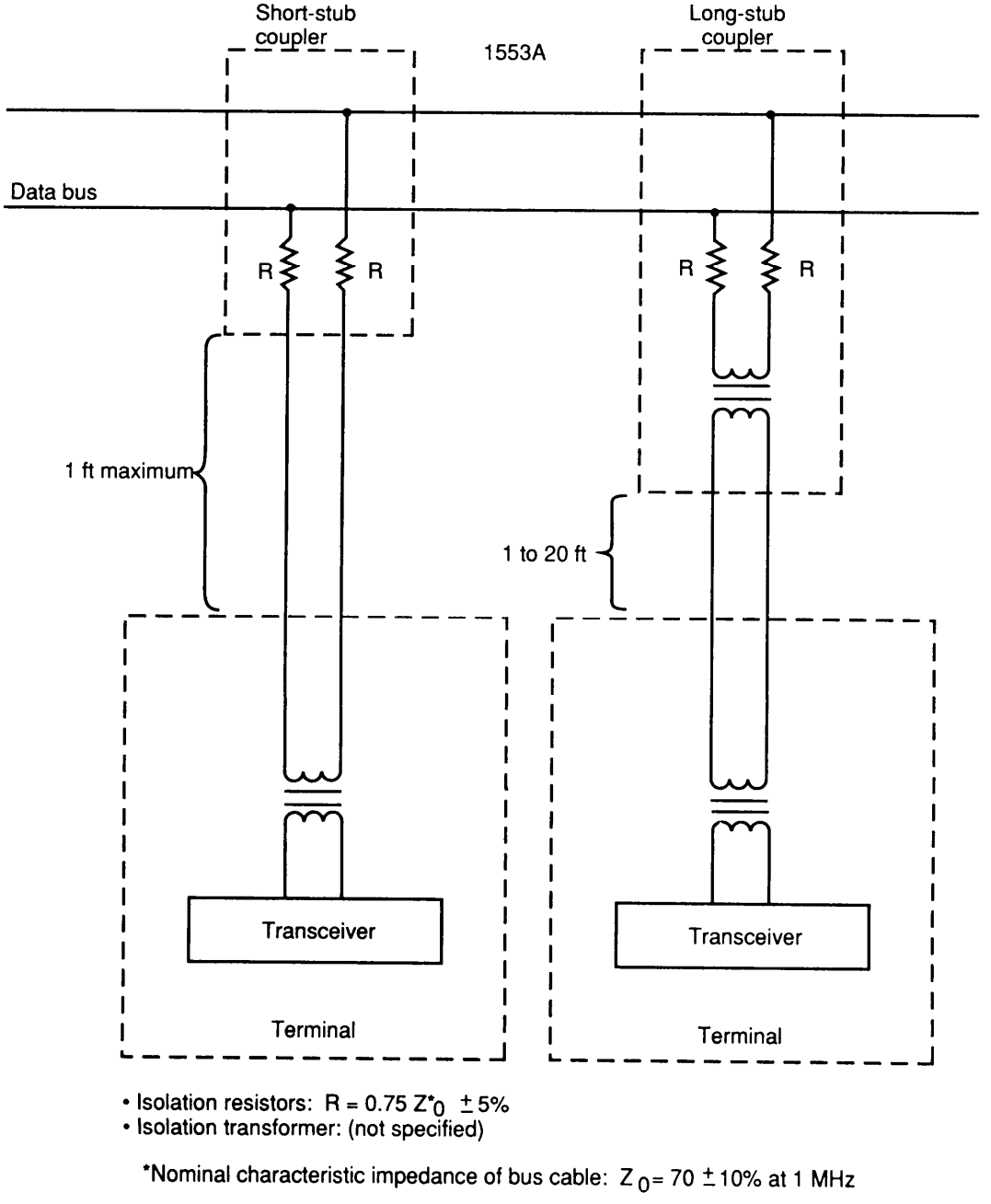
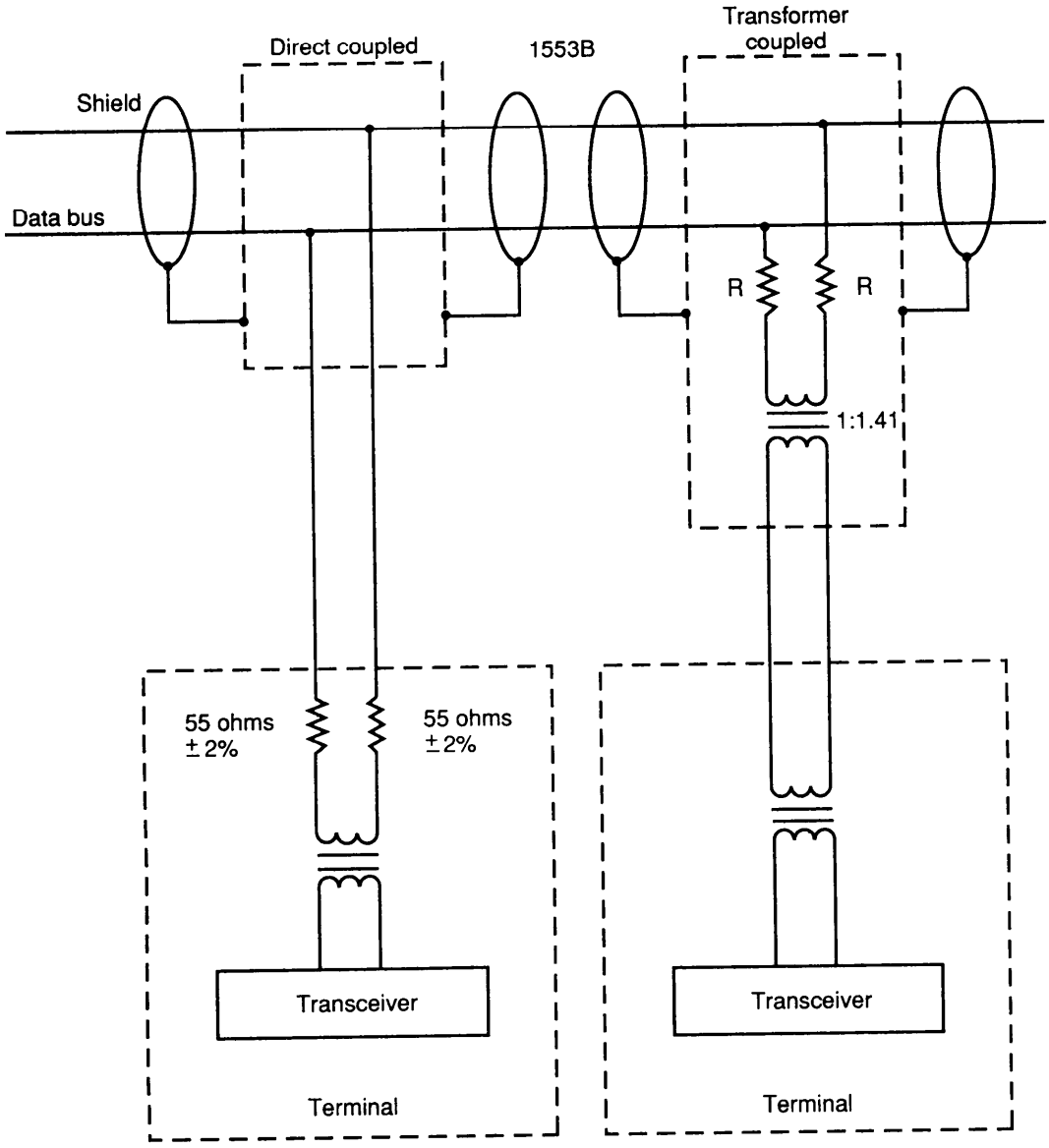


Figure 90-1. MIL-STD-1553A Coupler Characteristics



• Isolation resistors: R = 0.75 Z^*_o ±2%
• Isolation transformer: turns ratio 1:1.41 ±3%
(1-terminal winding)
(1.41-bus winding)

Z_{oc} > 3 kohm at 75 kHz to 1 MHz
1V rms sine wave

Droop: < 20%
Overshoot/ringing: < ±1V
CMR: > 45dB at 1 MHz
} at 27 Vp-p 250 kHz square wave

*Nominal characteristic impedance of bus cable: Z_o = 70 ohm to 85 ohm at 1 MHz

CMR: Common mode rejection

Figure 90-2. MIL-STD-1553B Coupler Characteristics

Note 63. The fault-isolation resistor requirements for terminal-to-bus interface circuits (i.e., stubs) changed from absolute values of resistance in 1553 to values relative to the data bus cable characteristic impedance (Z_o) in 1553A. In 1553B, different fault-isolation resistor requirements were specified, depending on the type of stub. The 1553B resistor requirements were stated in terms of relative values in the case of transformer-coupled stubs and in terms of absolute values in the case of direct-coupled stubs.

Note 64. The terminal output power and voltage requirements were specified in 4.2.5.3.1 and 4.2.5.3.2 of 1553. These requirements were consolidated in 4.2.5.3.1 in 1553A. In 1553B, the output power requirement was eliminated and new output voltage requirements were provided for transformer-coupled and direct-coupled connections in 4.5.2.1.1.1 and 4.5.2.2.1.1, respectively.

Note 65. In 1553A, the point at which the terminal output waveform is to be measured was changed, the lower limit of the rise and fall times of the waveform was reduced, and the distortion limits that were previously specified by 1553 were eliminated. In 1553B, an upper limit for the rise and fall times of the waveform was provided, and distortion limits were reintroduced.

Note 66. In 1553B, different output noise limits were provided for terminals with transformer-coupled stubs versus terminals with direct-coupled stubs. Notice 2 to 1553B provided separate output noise limits applicable during a power-up or power-down sequence.

Note 67. In 1553A, the acceptable range of input waveform peak amplitudes and the point at which the input waveform is to be measured were changed. In 1553B, different input waveform peak-to-peak amplitude limits were provided for terminals with transformer-coupled stubs and terminals with direct-coupled stubs.

Note 68. In 1553A, specific requirements were introduced for proper functioning of terminals in a noise environment. The noise environment was defined in terms of electric and magnetic fields, and proper functioning of a terminal was defined in terms of bit error rate and incomplete message rate. In 1553A, the test conditions were also defined under which noise environment operation shall be evaluated.

Note 69. The upper limit of peak line-to-ground voltage below which the performance of the terminal shall not be degraded was reduced by 1553A. The second (higher) limit of peak line-to-ground voltage that had been specified by 1553 as the value below which a signal should not damage or permanently impair the operation of the terminal was eliminated by 1553A.

Note 70. In 1553A, the previously specified minimum input impedance for frequencies below 100 KHz was eliminated. In 1553B, the frequency range was changed for which a minimum input impedance is specified, and different values were provided for the specified minimum input impedance depending on whether the terminal has a transformer-coupled connection or a direct-coupled connection.

Note 71. In 1553A, the following were added to the data validation criteria: an invalid word count shall be construed as a message transmission error. In 1553B, the word validation description was simplified and were returned to essentially the four basic criteria originally presented in 1553.

Note 72. In 1553B, it was specified that terminals shall have common operating capabilities (see notes 77 and 78).

Note 73. On the subject of transmission continuity, 1553B required the terminal to verify contiguous transmission of command/status and data words and stated that improperly timed data syncs shall be considered message errors.

Note 74. In 1553A, more specific requirements were provided concerning detection of erroneous transmissions and subsequent automatic self-shutdown of terminals, and a requirement was added for a transmission timeout to be included in the self-test circuitry. In 1553B, the allowable duration of a signal transmission,

beyond which the timeout is executed, was raised from 660 to 800 us. In 1553B, the requirement for automatic shutdown was also eliminated and replaced with the requirement that a reset of the timeout function be performed by the reception of a valid command on the bus on which the timeout has occurred.

Note 75. In 1553B, it was specified that different voltages be used to measure word error rate, depending on whether the terminal has a transformer-coupled connection or a direct-coupled connection to the data bus.

Note 76. The 1553 "MTU/SSIU interface" requirements were replaced by the 1553A 'terminal to subsystem interface" requirements.

Note 77. In 1553B, separate requirements were introduced for bus controller (BC), remote terminal (RT), and bus monitor (BM) operations.

Note 78. In 1553B a new section on hardware characteristics was introduced (4.5).

Note 79. Notice 1 to 1553B provided specific restrictions for use of mode code indicators in Air Force avionic applications.

Note 80. Notice 1 to 1553B raised the required cable shield coverage to a minimum of 90.0%.

Note 81. Notices 1 and 2 both specified that the actual (not nominal) characteristic impedance of the data bus is to be within the range of 70.0 ohms to 85.0 ohms.

Note 82. For Air Force avionic applications, Notice 1 to 1553B increased the required amount of coverage provided by the continuous shielding on cable coupling elements from 75% to 90.0%.

Note 83. Notice 2 to 1553B confirmed the requirement for the cable shield to provide a minimum of 90.0% coverage.

Note 84. Notice 2 to 1553B changed the name from "reset data bus transmitter" to "superseding valid command." It also changed the requirement of receiving superseding commands from either bus (dual-redundant systems) to the other bus.

Note 85. Notice 2 specifies connector polarity when using concentric connectors or inserts. The center pin is to be used for the high (positive) Manchester biphase signal. The inner ring is to be used for the low (negative) Manchester biphase signal.

Note 86. Notice 2 specifies the maximum allowable output noise when terminal powered is turned on or off. The maximum allowable output noise amplitude shall be ±250 mV peak, line-to-line for transformer-coupled stubs and ±90 mV peak, line-to-line for direct-coupled stubs.

Note 87. In 1553B, the transformer turns ratio was set at 1:1.41 with 3% tolerance; whereas, 1553A did not specify the turns ratio. The 1553B turns ratio, along with other waveform and electrical details, establishes more uniform waveform quality requirements. Each 1553A terminal must be evaluated to determine if its transformer turns ratio is compatible with 1553B.

Note 88. This note specifically applies to table 90-11 and applies to many of the instances of the use of 1553B bus controllers (BC) and remote terminals (RT) in a system that may have a mix of BCs and RTs that are also 1553B or 1553B Notice 1 or 1553B Notice 2. These three versions of the standard establish use and restrictions of the mode codes and status word bits. For the three versions of 1553B BCs to be interoperable with the three versions of 1553B RTs, the BC must be mechanized to act in a unique way for each 1553B version of BC and RT. Therefore, the options and restrictions of an individual 1553B version RT must be known to establish the BC.

Note 89. Four conditionally required status bits are to be implemented in a 1553B Notice 2 remote terminal (RT).

Note 90. The message error bit in a 1553A remote terminal (RT) may beset, but a 1553A RT will not suppress the status word, as required by 1553B. Therefore, 1553B bus controllers (BC) should be able to recognize that a status word received from a 1553A RT with message error bit set is equivalent to a suppressed status word of 1553B.

SECTION 90 INDEX

SECTION 100

RT VALIDATION TEST PLAN

CONTENTS

FIGURES

100. RT VALIDATION TEST PLAN

Section 100 of this handbook revision supersedes Appendix A of Notice 1 for MIL-HDBK-1553 and should be used in all applications where the previous test plan was specified. The only technical changes made areas listed below:

paragraph	revision
5.1.2.1.1	In second sentence "ideal" was added between "previous" and "zero". This was a clarification.
5.2.1.1.1	The first lines of items d and g were changed to: "Undefined" mode commands (See Table I): (for any one undefined mode command, any single set(l), (2), (3), or (4) is acceptable)" This change was for clarification.
5.2.1.1.2	The introductory paragraph was modified to provide more clarification and alleviate misinterpretation.
5.2.1.4.1	This is a new test: RT-RT superseding command.
5.2.1.5.1	In step 6 the alternate bus was changed to primary bus. This was an error in the original test plan.
5.2.1.5.3	This test was rewritten to better accomplish the original intent of the test.
5.2.1.7	This was changed to an introductory paragraph. The original "RT to RT timeout''test was modified and became 5.2.1.7.1. A new test "RT to RT message format errors" was added as 5.2.1.7.2. A new test for "transmitting RT errors" was added is 5.2.1.7.3.
5.2.1.8	The pass criteria for a, step 1, under RT transmitting was changed to: "... for a step 1-NR, truncated message, or CS...''This adds "NR" as permissible.
5.2.2.1.3	This test was rewritten to better accomplish the original intent of this test.
5.2.2.2.2	Step 6 and Step 7 were deleted as well as the criteria for these two steps. These steps duplicated 5.2.2.5.1.2 and inconsistently handled the BCR limit.
5.2.2.2.4	The pass criteria for step 3 was changed to CS only.
5.2.2.3	This test was rewritten.
5.3	The following two sentences were added to the end of this paragraph to be consistent with 5.1 and 5.2: "A unit under test (UUT) that provides transformer and direct coupled stubs shall be tested on both stubs. The noise test shall be performed on all busses for UUTs with redundant bus configurations.

APPENDIX A RT VALIDATION TEST PLAN

NOTE: THE REMAINDER OF THIS SECTION IS A REPRINT OF THE VERSION PUBLISHED AS PART OF MIL-HDBK-1553 DATED 24 SEPTEMBER 1986

FOREWORD

This section of the handbook provides a sample test plan for MIL-STD-1553B that may sewe several different purposes. This section is intended to be noncontractual when the entire MIL-HDBK-1553 is referenced in an equipment specification or SOW. In this case the test plan, as well as the rest of the handbook, provides guidance to both the DOD procuring engineer and the contractor design engineer. This section is intended to be contractual when specifically called out in a specification, SOW, or when required by a DID. If the contractor is required to submit a test plan for his RT to the government, he may remove this section from the handbook and submit it as a portion of his test plan. A better approach would be to simply reference this section. In either case, any and all contractor changes, alterations, or testing deviations to this section shall be separately listed for easy review by government personnel.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLES

FIGURES

APPENDICES

1.0 SCOPE

1.1 General. This validation test plan defines the test requirements for verifying that the design of remote terminals meet the requirements of MIL-STD-1553B, "Digital Time Division Command/Response Multiplex Data Bus." A remote terminal is considered to have failed to meet the above requirements if that remote terminal fails any test or a portion of any test performed according to this test plan. Passing this test plan does not automatically mean that the remote terminal is acceptable for use by the government. The remote terminal must also meet all the requirements of MIL-STD-1553B over all the environmental, EMI, vibration, and application requirements in the subsystem specification.

1.2 Application. This general test plan is intended for design verification of remote terminals designed to meet the requirements of MIL-STD-1553B, Notice 2. Appendix A and B provide cross references between this test plan and MIL-STD-1553B. Forthose remote terminals not required to meet Notice 2, Appendix C and D list the changes in this test plan for MIL-STD-1553B only and MIL-STD-1553B, Notice 1. These requirements shall apply to the terminal under test, when invoked in a specification or statement of work.

2.0 APPLICABLE DOCUMENTS

2.1 Standards

MILITARY

MIL-STD-1553 Digital Time Division Command/Response Multiplex Data Bus

3.0 DEFINITIONS

3.1 Responses. The following are definitions of the responses of the RT as used in this test plan. In each case the status word must have the correct terminal address and unused status bits set to zero.

3.1.1 Broadcast command received (BCR). The broadcast command received bit (bit time fifteen) is set in status word (and no data words in response to a transmit status mode command or a single data word in response to a transmit last command mode command).

3.1.2 Busy bit (BUSY). CS with the busy bit (bit time sixteen) set in the status word, and no data words.

3.1.3 Clear status (CS). The status word may have the busy bit and/or service request bit set. All other status code bits in the status word must be zero and the associated message must have the proper word count.

3.1.4 Dynamic bus acceptance by (DBA). CS with the dynamic bus control acceptance bit (bit time eighteen) set in the status word.

3.1.5 Service request bit (SRB). CS with the service request bit (bit time eleven) set in the status word.

3.1.6 Message error bit (ME). The message error bit (bit time nine) is set in the status word and no data words (except in response to a transmit last command mode command which requires on data word).

3.1.7 No response (NR). The addressed terminal does not produce any response to the command.

3.1.8 Respond in form. A terminai is said to "respond in form" if its response to an illegal command as defined in the paragraph titled "illegal command" of MIL-STD-1553 consists of a response formatted as though it were a legal command.

3.1.9 Subsystem flag bit (SF). CS with the subsystem flag bit (bit time seventeen) set in the status word.

3.1.10 Terminal flag bit (TF). CS with the terminal flag bit (bit time nineteen) set in the status word.

4.0 GENERAL REQUIREMENTS

4.1 General test requirements. The following paragraphs define the configurations, pass/fail criteria, and general procedures for testing remote terminals (RT). Specifically, this document contains the test configurations and procedures for the Elect rical tests (5.1), the Protocol Tests (5.2), and the Noise Rejection Test (5.3) for MIL-STD-1553 remote terminals. The remote terminal under test is referred to as the unit under test (UUT). Proper terminal responses are defined in each test paragraph. If the hardware/software design of the UUT does not permit a test to be performed, then adequate analysis shall be provided in place of the test results to demonstrate that the design meets the requirements of MIL-STD-1553 as stated in the test.

Any condition which causes the UUT to respond other than as called out in MIL-STD-1553, to lock up, or require a power cycle in order to recover for any reason shall automatically cause that UUT to fail the test. All occurrences of responses with the busy bit set in the status word shall be recorded. If the UUT response does not match the pass criteria for a particular test, then the UUT has failed that test.

4.2 Test for optional requirements. All tests for optional requirements defined in 5.2.2 shall be executed if that MIL-STD-1553 option is required by the subsystem specification or interface control document (ICD) . Any optional capabilities implemented in the RT should also be tested, if possible. Within the constraints imposed by the hardware/software design, optional capabilities must be tested prior to use by system integrators.

4.3 General monitoring requirement . In addition to the specific tests that follow, certain RT parameters must be continuously monitored throughout all tests. These parameters are:

a. response time
b. contiguous data
c. proper Manchester encoding
d. proper bit count
e. odd parity
f. proper word count
g. proper terminal address in the status word
h. reserved status and instrumentation bits in the status word are set to zero
i. proper sync

The UUT shall have failed the test if at any time during the test any of these parameters fail to meet the requirements of MIL-STD-1553. Record the parameters for all failures.

5.0 DETAILED REQUIREMENTS

5.1 Electrical tests.. Each test paragraph contains the requirements for both transformer and direct coupled stubs. A UUT which provides both transformer and direct coupled stubs must be tested on both stubs. Electrical tests shall be performed on all buses for UUTS with redundant bus configurations.

5.1.1 Output characteristics. The following tests are designed to verify that all UUT output characteristics comply with MIL-STD-1553. These tests shall be performed after establishing communications between the test equipment and the UUT. All output electrical tests shall use figure 1A, General Resistor Pad Configuration, with all measurements taken at point “A”, unless otherwise noted.

5.1.1.1 Amplitude. A valid, legal transmit command shall be sent to the UUT, requesting the maximum number of words that it is capable of sending. The amplitude of the waveform transmitted by the UUT shall be measured, peak-to-peak, as shown on figure 2,

The pass criieria for Vpp for transformer coupled stubs shall be 18.0 V minimum, and 27.0 V maximum. The pass criieria forVpp for direct coupled stubs shall be 6.0 V minimum and 9.0 V maximum. The maximum and minimum measured parameters, Vpp, shall be recorded.

5.1.1.2 Risetime/falltime. A valid, legal transmit command shall be sent to the UUT, requesting at least one data word. The rise and fall time of the UUT waveform shall be measured between the 10% and 90% points of the waveform as shown on figure 2. The measurements shall be taken at both the rising and falling edges of a sync waveform and a data bit waveform. The risetime (Tr) and the falltime (Tf) shall be recorded.

The pass criteria shall be 100 ns $\leq$ Tr $\leq$ 300 ns and 100 ns $\leq$ Tf $\leq$ 300 ns. The measured parameters, Tr and Tf, shall be recorded.

Note: The risetime of the sync waveform shall be measured at the mid-crossing of a data word sync, and the fall time of the sync waveform shall be measured at the mid-crossing of the status word sync.

5.1.1.3 Zero crossing stability. A valid legal transmit command shall be sent to the UUT, requesting the UUT to transmit words having zero crossing time intervals of 500 ns, 1000 ns, 1500 ns and 2000 ns. The zero crossing time shall be measured for both the positive (Tzcp) and the negative (Tzcn) waveforms as shown on figure 3.

The pass criteria for each case shall be that Tzcp and Tzcn = 500 ±25 ns, 1000 ±25 ns, 1500 ±25 ns and 2000 ±25 ns. The measured parameters, Tzcp and Tzcn shall be recorded for each case.

5.1.1.4 Distortion, overshoot and ringing. A valid legal transmit command shall be sent to the UUT, requesting the UUT to transmit at least one data word. The distortion of the waveform, distortion voltage (VD) shall be measured as indicated on figure 2.

Pass criteria shall be VD <+ 900 mV peak, line-to-line, for transformer coupled stubs or VD <+ 900 mV peak, line-to-line, for direct coupled stubs. The worst measured parameter, VD, shall be recorded.

5.1.1.5 Output symmetry. A valid legal transmit command shall be sent to the UUT requesting the maximum number of data words that the UUT is capable of transmitting. The output symmetry is determined by measuring the waveform tail-off at the end of each message. The maximum residual voltage (Vr) shall be measured as shown on figure 2. This test shall be run six times with each data word in the message having the same bit pattern. The six data word bit patterns that shall be used are:

8000(HEX), 7FFF(HEX), 0000(HEX), FFFF(HEX),
5555(HEX), AND AAAA(HEX

The pass criteria shall be V4 <+ 250 mV peak, line-to-line, for transformer coupled stubs and Vr <+ 90 mVpeak, line-to-line, for direct coupled stubs after time Tt (the time beginning 2.5 us after the mid-bit zero crossing of the last parity bit). The measured parameter, Vr, shall be recorded for each bit pattern.

5.1.1.6 Output noise. The test configuration shown on figure 4 shall be used to test the UUT inactive bus output noise levels. The test shall reconducted while the UUT is in the power-on receive state and the power-off state. The output noise (Vrms) shall be measured at point “A” as shown on figure 4 for both states. Measurements shall be made with an instrument that has a minimum frequency bandwidth of DC to 10 MHz.

The pass criteria shall be Vrm $\leq$ 14.0 mV for transformer coupled stubs and Vrms $\leq$ 5.O mV for direct coupled stubs. The measured parameters, Vrms, shall be recorded for each case.

5.1.1.7 Output isolation. This test shall be performed only if the UUT is configured with redundant buses. A valid legal transmit command shall be sent to the UUT requesting the maximum number of data words that it is capable of sending. The voltage of the output waveform transmitted by the UUT shall be measured on

the active and redundant bus (or buses). Each data bus shall be alternately activated and measurements taken.

The pass criteria shall be that the ratio in dB between the output peak-to-peak voltage on the active bus and the output peak-to-peak voltage on all inactive buses shall be greater than or equal to 45 dB (figure 5). The measured parameters, output isolation, expressed as a ratio in dB, shall be recorded for each bus combination.

5.1.1.8 Power on/off.

5.1.1.8.1 Power on/off noise. A UUT shall limit any spurious differential output during a power-up or power-down sequence. Power shall be applied to the UUT and any outputs from the UUT shall be measured. Power shall be removed from the UUT and any output from the UUT shall be measured. Repeat the test ten times.

The pass criteria shall be:

a. For transformer coupled stubs any spurious noise pulses produced shall be less than or equal to ±250 mV peak, line-to-line.

b. For direct coupled stubs any spurious noise pulses produced shall be less than or equal to ±9O mV peak, line-to-line.

All measured parameters, output noise amplitudes and pulse widths, shall be recorded.

Note: This test shall be performed using the normal on/off power sequence of the UUT.

5.1.1.8.2 Power on response. The purpose of this test is to verify that the UUT responds correctly to commands after power is applied to the UUT. Using the normal power on sequence for the UUT, repeat the following test sequence a minimum of ten times.

Step 1. Power the UUT off.

Step 2. Send valid, legal, non-broadcast, non-mode commands to the UUT with a maximum intermessage gap of 1 ms.

Step 3. Power on the UUT and observe all the responses for a minimum of 2 s from the first transmission of the UUT after power on.

The pass criteria shall be: step 3 - NR until the first UUT transmission, and CS for the first transmission and all responses thereafter.

5.1.1.9 Terminal response time. The purpose of this testis to verify that the UUT responds to messages within the proper response time. The test sequence shown below shall be performed.

Step 1. A valid legal transmit command shall be sent to the UUT and the response time measured.

Step 2. A valid legal receive command shall be sent to the UUT and the response time measured.

Step 3. A valid legal RT-to-RT command, with the UUT as the receiving terminal, shall be sent to the UUT and the response time measured.

Step 4. A valid legal mode command shall be sent to the UUT and the response time measured.

The pass criteria for step 1, step 2, step 3, and step 4 shall be a response time between 4.0 and 12.0 us at point A of figure 1A and measured as shown on figure 7. The command words used and the response times shall be recorded.

5.1.1.10 Frequency stability. The purpose of this testis to verify that the transmitter clock in the UUT has the proper accuracy and long term stability and proper short term stability. The transmitter clock measured shall be either the main oscillator output or an appropriate derivative of that clock (e.g., either the 16 MHz oscillator or the 1-2 MHz transmitter shift clock). The test sequence shown below shall be performed on the clock output whose ideal frequency is Fi.

Step 1. The short term transmitter clock frequency shall be measured for a single period of the waveform.

Step 2. Repeat step 1 for at least 10,000 samples and record the minimum (Fsmin) and the maximum (Fsmax) frequency from the samples taken.

Step 3. Thetransmitter clock frequency shall be measured with agate time of 0.1s and the mean frequency for at least 1,000 samples (Fav) shall be recorded.

The pass criteria shall be:

Step 1 and step 2 -Ss1 = 100 (Fsmax - Fav)/Fav $\leq$ 0.01 and Ss2 = 100 (Fav-Fsmin)/Fav $\leq$ 0.01;

Step 3- the magnitude of S1 = 100 (Fav-Fi)/Fi $\leq$ 0.1. Record Ss1, Ss2 and S1.

5.1.2 Input characteristics. The input tests are designed to verify that multiplex devices can properly decode hi-phase data. All input electrical tests shall use figure 1A or figure 1B with all measurements taken at point "A," unless otherwise noted. For Air Force applications, all input electrical tests shall use figure 1 B, with all measurements taken at point "A" unless otherwise noted.

5.1.2.1 Input waveform compatibility.

5.1.2.1.1 Zero crossing distoration. A legal valid receive message shall be sent to the UUT and the proper response verified. Positive and negative zero crossing distortions equal to N ns, with respect to the previous ideal zero crossing shall be introduced individually to each zero crossing of each word transmitted to the UUT. The transmitted signal amplitude at point "A" shall be 2.1 Vpp for transformer coupled stubs and 3.0 Vpp for direct coupled stubs. The rise and fall time of the transmitted message (measured at a data bit zero crossing with the prior zero crossing and the next zero crossing at 500 ns intewals from the measured zero crossing) measured at point "A" shall be 200 ns ±20 nS. Each zero crossing distortion shall be transmitted to the UUT a minimum of 1000 times.

The pass criteria is the transmission of a CS by the UUT for each zero crossing distortion sent with N $\geq$ 150 ns. Positive and negative zero crossing distortions shall then be applied in turn to a single zero crossing and adjusted to determine the values at which the first NR of the UUT occurs; these values shall be recorded.

The fail criteria is the transmission of a NR by the UUT for any zero crossing distortion sent with N $\leq$ 150 ns.

5.1.2.1.2 Amplitude variations. A legal valid receive message shall be sent to the UUT. The transmitter's voltage, as measured at point "A" of figure 1A or figure 1 B, shall be decremented from 6.0 Vpp to 0.1 Vpp for transformer coupled stubs and from 9.0 Vpp to 0.1 Vpp for direct coupled stubs in steps no greater than 0.1 Vpp. The rise and fall time of the transmitted message (measured at a data bit zero crossing with the prior zero crossing and the next zero crossing at 500 ns intervals from the measured zero crossing) measured at point "A" shall be 200 ns ±20 ns. The response of the UUT shall be observed at each step. A minimum of 1000 messages shall be transmitted for each setting.

The pass criteria shall be:

a. A CS for 0.86 , ≤ Vpp ≤ 6.0 for transformer coupled stubs and 1.2 ≤ Vpps ≤ 9.0 for direct coupled stubs

b. A NR for Vpp ≤ 0.20 for transformer coupled stubs and Vpps ≤ 0.28 for direct coupled stubs

The measured parameter, Vpp, at which NR first occurs shall be recorded.

5.1.2.1.3 Rise and fall time.

5.1.2.1.3.1 Trapezoidal. A minimum of 1000 valid receive messages shall be sent to the UUT with a signal amplitude of 2.1 Vpp for the transformer coupled stub and 3.0 Vpp for the direct coupled stub. The rise and fall times of the signal shall be less than or equal to 100 ns.

The pass criteria shall be CS by the UUT for each message.

5.1.2.1.3.2 Sinusoidal. A minimum of 1000 valid receive messages shall be sent to the UUT with a signal amplitude of 2.1 Vpp for the transformer coupled stub and 3.0 Vpp for the direct coupled stub. The rise and fall times of the signal shall approximate that of a 1 MHz sinusoidal signal.

The pass criteria shall be CS by the UUT for each message.

5.1.2.2 Common mode rejection. The common mode test configuration, figure 6Aor figure 6B, shall be used for this test. Legal valid receive messages with the UUT'S maximum word count shali be sent to the UUT at a repetition rate which generates a bus activity dut y cycle of 50% ±10% with a common mode voltage injected at point "C", and the UUT response observed. The voltage of the transmitted message measured at point 'A" shaii be .86 Vpp for transformer coupled stubs and 1.2 Vpp for direct coupled stubs. The rise and fall time of the transmitted message (measured at a data bit zero crossing with the prior zero crossing and the next zero crossing at 500 ns intervals from the measured zero crossing) measured at point "A shall be 200 ns ±20 ns. The following common mode voltage levels shall be applied in turn: +10.0 V.D.C. line-to-ground, -10.0 V.D.C. line-to-ground and ±1O Vp line-to-ground sinusoidal signal that is swept through the range of 1 Hz to 2 MHz. Each test condition shall be present for a minimum time period of 90 seconds.

The pass criteria shall be a CS by the UUT for all messages at each setting. lf a failure occurs, the measured parameters, common mode signal injected shall be recorded.

5.1.2.3 Input impedence. The input impedance of the UUT in a stand alone configuration (i.e., disconnected from figure 1A or 1B) shall be measured with the UUT power on and with the UUT power off. The input impedance, Zin, shall be measured with a sinusoidal waveform having an amplitude 1.0 VRMS to 2.0 VRMS, at the following frequencies: 75.0 kHz, 100.0 kHz, 250.0 kHz, 500.0 kHz and 1.0 MHz.

The pass criteria shali be Zin ≥ 1000 ohms for transformer coupled stubs and Zin ≥ 2000 ohms for direct coupied stubs. The measured parameter, Zin, shall be recorded at each frequency.

5.2 Protocol tests. All tests in this section shall use the test configuration as shown on figure 1A or figure 1B. The test signal amplitude shali be 3.0 Vpp ±0.1 Vpp for direct coupled stubs and 2.1 Vpp ±0.1 Vpp for transformer coupied stubs measured at point A. For UUTs having both direct and transformer coupled stubs, the protocol tests need only be performed on one stub type per bus. The protocol tests shaii be performed on all buses for UUTS with redundant bus configurations.

5.2.1 Required remote terminal operation. The following tests verify required operations of a remote terminai.

5.2.1.1 Response to command words. The purpose of this testis to verify that the UUT responds properly to all commands.

5.2.1.1.1 Rt response to command words. All possible command words (65, 536 combinations) meeting the criteria of the paragraph on "Word validation" of MIL-STD-1553 shall be sent to the UUT. Mode commands tested in 5.2.1.5, 5.2.2.1, or 5.2.2.4 maybe omitted from this test since they are tested separately. Each command word shall be followed by the proper number of contiguous valid data words as defined in the paragraph on "Message formats" of MIL-STD-1553. Refer to table I for undefined mode commands. The associated data may be either random or controlled, depending on the UUT requirements. The following sequence shall be executed for all combinations of command words where the varying command word is sent as step 2.

Step 1. Send a valid legal non-broadcast non-mode command to the UUT.

Step 2. Send the variable command word to the UUT.

Step 3. Send a transmit last command mode command to the UUT. (If this mode command is not implemented, then transmit status mode command shall be used and the data word associated with transmit last command mode command shall be deleted from the pass criteria.)

The pass criteria given below is contingent on the type of command sent. All commands which cause the UUT to fail shall be recorded.

Non-Broadcast Commands (including mode commands):

a. Valid legal commands: step 1- CS; step 2- CS; step 3- CS and the data word contains the command word bit pattern from step 2 (except for transmit last command mode command wherethe data word contains the command word bit pattern from step 1).

b. Valid illegal commands:

(1) If illegal command detection option is implemented: step 1 -CS; step 2- ME with no data words; step 3-ME and the data word contains the command word bit pattern from step 2.

(2) If the illegal command detection option is not implemented: step 1- CS; step 2- CS; step 3- CS and th data word contains the command word bit pattern from step 2.

c. Invalid command (wrong RT address): step 1- CS; step 2- NR; step 3- CS and the data word contains the command word bit pattern from step 1.

d. Undefined mode commands (see table 1) (for any one undefined mode command, any single set (1), (2), (3), (4), is acceptable):

(1) step 1- CS; step 2- CS; step 3- CS and the data word contains the command word bit pattern addressed to the UUT from step 2.

(2) step 1- CS; step 2- ME; step 3- ME and the data word contains the command word bit pattern addressed to the UUT from step 2.

(3) step 1- CS; step 2- NR; step 3- CS and the data word contains the command word bit pattern addressed to the UUT from step 1.

(4) step 1- CS; step 2- NR; step 3- ME and the data word contains the command word bit pattern addressed to the UUT from step 2.

Table I. MIL-STD-1553B Undefined Mode Codes

T/R	MODE CODE	ASSOCIATED DATA WORD
0	00000	No
0	01111	No
0	10000	Yes
0	10010	Yes
0	10011	Yes
1	10001	Yes
1	10100	Yes
1	10101	Yes

Broadcast Commands (including mode commands):

e. If there are any broadcast commands that are considered as valid commands:

(1) Legal commands: step 1 -CS; step 2- NR; step 3- BCR and the data word contains the commands word bit pattern from step 2.

(2) Illegal commands (if illegal command detection is implemented): step 1- CS; step 2- NR; step 3- BCR and ME and the data word contains the command word bit pattern from step 2.

(3) Illegal commands (if illegal command detection is not implemented): step 1- CS; step 2- NR; step 3- BCR and the data word contains the command word bit pattern from step 2.

f. If there are no broadcast commands that are considered as valid commands: step 1 -CS; step 2-NR; step 3-CS and the data word contains the command word bit pattern from step 1.

g. Undefined broadcast mode commands (see table 1) (for anyone undefined mode command, any single set (1), (2), (3) is acceptable):

(1) step 1 - CS; step 2- NR; step 3- BCR and the data word contains the command word bit pattern from step 2.

(2) step 1 - CS; step 2- NR; step 3-ME and BCR and the data word contains the command word bit pattern from step 2.

(3) step 1 - CS; step 2- NR; step 3- CS and the data word contains the command word bit pattern from step 1.

5.2.1.1.2 RT-RT response to command words. All possible command words (65,536 combinations) meeting the criteria of the paragraph on “Word validation: of MIL-STD-1553 shall be sent to the UUT embedded in an RT-RT message format. The test equipment shall supply the required responses fortheother RT in order to properly complete the message formats as defined in paragraph on ‘Message format”of MIL-STD-1553. Refer to Table I for undefined mode commands. The associated data maybe either random or controlled, depending on the UUT requirements. The intent of this testis to send all combinations of RT to RT command pairs with a fixed receive command addressed to the UUT and a variable transmit command, which includes all combinations of command words with the T/R bit equal to one and terminal address field different from the UUT’S, to which the status response and data is simulated. Then send all combinations of

RT to RT command pairs with a fixed transmit command adressed to the UUT and a variable receive command, which includes all combinations of command words having the T/R bit equal to zero and the terminal address field different from the UUT'S, to which the status response is simulated. Note that this test includes 1024 transmit comands to RT address 31 (broadcast) which are invalud messages. Mode commands tested in 5.2.1.5, 5.2.2.1 or 5.2.2.4 maybe omitted from this test since they are tested separately. The following sequence shall be executed for all combinations of command words where the varying command word is sent as step 2.

Step 1. Send a valid non-broadcast non-mode command to the UUT.

Step 2. Send the variable command word to the UUT embedded in the RT-RT message format.

Step 3. Send a transmit last command mode command to the UUT. (If this mode command is not implemented, then a transmit status mode command shall be used and the data word associated with transmit last command mode command shall be deleted from the pass criteria.)

The pass criteria shall be as listed in 5.2.1.1.1, except the pass criteria for any RT-RT mode command is as specified in 5.2.1.1.1.d and the pass criieria for any broadcast RT-RT mode command shall be as specified in 5.2.1.1.1.g.

5.2.1.2 Intermessage gap

5.2.1.2.1 Minimum time. The purpose of this testis to verify that the UUT responds properly to messages with a minimum intermessage gap. The message pairs listed in table II shall be sent to the UUT with the minimum intermessage gaps as defined in the paragraph on "Intermessage gap" of MILK-STD-1553. Each message pair shall be sent to the UUT a minimum of 1,000 times. Message pairs which include commands not implemented by the UUT shall be deleted from the test. Each message pair shall have an intermessage gap time (T) of 4.0 us as shown on figure 7.

The pass criteria for this test is CS for each message. All message pairs used shall be recorded and message pairs which cause the UUT to fail the test shall be indicated.

5.2.1.2.2 Tramsmission rate. Thepurposeofthis test istoverifythat the UUTresponds properly to messages sent for a sustained period with a minimum intermessage gap. The message listed in each step shall be sent with an intermessage gap of 7 us ±3 us, i.e. a burst of messages with an inermessage gap of 7 us ±3 us between each message as shown on figure 7. Each step shall be performed for a minimum of 30 s.

Step 1. A valid legal transmit message followed by a valid legal transmit message.

Step 2. A valid legal receive message followed by a valid legal receive message.

Table II. Intermessage gap messages.

COMMAND TYPES

A) BC to UUT Transfer (maximum word count)
B) UUT to BC Transfer (maximum word count)
C) UUT/RT (maximum word count)
D) RT/RT (maximum word count)
E) Mode Command Without Data Word
F) Mode Command With Data Word (Transmit)
G) Mode Command With Data Word (Receive)
H) BC to UUT Transfer (Broadcast) (maximum word count)

l) UUT/RT (Broadcast) (maximum word count)
J) RT/UUT (Broadcast) (maximum word count)
K) Mode Command Without Data Word (Broadcast)
L) Mode Command With Data Word (Broadcast)

MESSAGE PAIRS

1) A (GAP) A
2) B (GAP) A
3) C (GAP) A
4) D (GAP) A
5) E (GAP) A
6) F (GAP) A
7) G (GAP) A
8) H (GAP) A
9) I (GAP) A
10) J (GAP) A
11) K (GAP)A
12) L (GAP) A

Note: This table defines the types and combinations of messages to be used in test 5.2.1.2, e.g., pair number 2 specifies a transmit command with the maximum word count to be followed (after the minimum intermessage gap time specified in the paragraph on "Intermessage gap" of MIL-STD-1553) by a receive command with the maximum word count.

UUT/RT: denotes RT to RT transfer with UUT receiving
RT/UUT: denotes RT to RT transfer with UUT transmitting

Step *3* A valid legal transmit message followed by a valid legal receive message.

The pass criteria for this test is a CS for each message. All messages which cause the UUT to fail the test shall be recorded.

Note: If the busy bit gets set, then increase the intermessage gap until the busy bit is reset. At this time record the intermessage gap and repeat steps 1 thru 3 until the testis completed without the busy bit getting set.

5.2.1.3 Error Injection. The purpose of these tests is to examine the UUT'S response to specific erros in the message stream. Unless otherwise noted, the following test sequence shall be used for all error injection tests. The error to be encoded in step 2 for a given message is specified in each test paragraph.

Test sequence:

Step 1. A valid legal message shall be sent to the UUT. A mode command shall not be used.

Step 2. A legal message containing the specified error shall be sent to the UUT.

Step 3. A transmit status mode command shall be sent to the UUT.

The pass criteria is defined in each test paragraph. All commands and responses shall be recorded.

5.2.1.3.1 Parity. The purpose of these tests is to verify the UUT'S capability of detecting parity errors embedded in different words within a message.

5.2.1.3.1.1 Transmit Command Word. This test verifies the ability of the UUT to detect a parity erroroccurring in a transmit command word. The test sequence as defined in 5.2.1.3 shall be performed with a parity error encoded into a transmit command word for test step 2.

The pass criteira for this test shall be: step 1 -CS; step 2- NR; step 3- CS.

5.2.1.3.1.2 Receive Command Word. This test verifies the ability of the UUT to recognize a parity error occurring in a receive command word. The test sequence as defined in 5.2.1.3 shall be performed with a parity error encoded in a receive command word for test step 2.

The pass criteria for this test shall be: step 1- CS; step 2- NR; step 3-CS.

5.2.1.3.1.3 Receive Data Words. This test verifies the ability of UUT to recognize a parity error occurring in a data word. The test sequence as defined in 5.2.1.3 shall be performed with a pariiy error encoded in a data word fortest step 2. The message shall be a receive command with the maximum number of data words that the UUT is designed to receive. The test sequence must be sent N times, where N equals the number of data words sent.

Individually each data word must have the parity bit inverted. Only one parity error is allowed per message.

The pass criteria for this test shall be: step 1- CS; step 2- NR; step 3- ME.

5.2.1.3.2 Word Length. This test verifies the ability of the UUT to recognize transmit command word length errors. The test sequence as defined in 5.2.1.3 shall be performed with the command word shortened as defined below for test step 2.

a. Transmit command shortened by one bit

b. Transmit command shortened by two bits

The pass criteria for this test shall be: step 1- CS, step 2- NR; step 3- CS.

5.2.1.3.2.2 Receive Command Word. This test verifies the ability of the UUT to recognize receive command word length erros. The test sequence as defined in 5.2.1.3 shall be performed with the command word as defined below for test step 2.

a. Shorten the receive command word by one bit

b. Shorten the receive command word by two bits

c. Lengthen the receive command word by two bits

d. Lengthen the receive command word by three bits

The pass criieria for this test shall be: step 1- CS; step 2- NR; step 3- CS, or alternately for c and d only, the pass criteria may be: step 1- CS; step 2- NR; step 3- ME.

5.2.1.3.2.3 Receive Data Words. This test verfies the ability of the UUTto recognize data word length errors. The test sequence as defined in 5.2.1.3 shall be performed as defined below for test step 2. The message shall be a receive command with the maximum number of data words that the UUT is designed to received.

a. Shortened the data word by one bit

b. Shortened the data word by two bits

c. Lengthen the data word by two bits

d. Lengthen the data word by three bits

The test sequence of 5.2.1.3 shall be performed N times for a and band N-1 times fore and d, where N equals the number of data words sent. High bit errors shall not be tested in the last data word of a receive message. Only one data word shall be altered at a time. Steps a through d shall be performed for each data word in the message.

The pass criteria for this test shall be: step 1- CS; step 2- NR; step 3- ME.

5.2.1.3.3 Bi-Phase Encoding. This test verifies the ability of the UUT to recognize hi-phase errors. A bi-phase encoding error is defined to be the lack of a zero crossing in the center of a bit time. A hi-phase error occurs as either a logic high or low for the duration of a bit time. Each bit location, except the sync period, of each word shall have a single hi-phase error encoded into it. Only a single hi-phase error shall be injected for each message.

5.2.1.3.3.1 Transit Command Word. This test verifies the ability of the UUT to recognize hi-phase encoding errors in transmit command words. The test sequence as defined in 5.2.1.3 shall be performed with a hi-phase encoding error encoded into a transmit command word for test step 2. Each bit location shall have each of the hi-phase erros injected into it. Only one hi-phase error is allowed per command word. A test set involves performing the test sequence 17 times, once for each bit location. A complete test requires two test sets to be performed, one for injecting high hi-phase erros and another for injecting low hi-phase erros.

The pass criteria for this test shall be: step 1- CS; step 2- NR; step 3- CS.

5.2.1.3.3.2 Receive Command Word. This test verifies the ability of the UUT to recognize bi-phaseencoding errors in receive command words. The test sequence as defined in 5.2.1.3 shall be performed with a hi-phase error encoded into a receive command word for test step 2. Each bit location must have each of the hi-phase erros injected into it. Only one hi-phase error is allowed per command word. A test set involves performing the test sequence 17 times, once for each bit location. A complete test requires two test sets to be performed one for injecting high hi-phase errors and another for injecting low hi-phase errors.

The pass criteria for this test shall be: step 1- CS; step 2- NR; step 3- CS.

5.2.1.3.3.3 Receive Data Words. This test verifies the ability of the UUT to recognize hi-phase encoding errors in data words. The test sequence as defined in 5.2.1.3 shall be performed with a hi-phase error encoded into each data word in the message for test step 2. The message shall be a receive command and the maximum number of data words that the UUT is designed to receive. Individually each bit location of each data word shall have a hi-phase error encoded into it. Only one hi-phase error is allowed for each message. A test set involves performing the sequence 17 times. The test set shall be repeated N times, where N equals the number of data words sent, A complete test requires 2*N test sets to be performed, once for high hi-phase errors and once for low hi-phase errors.

The pass criteria for this test shall be: step 1- CS; step 2- NR; step 3- ME.

5.2.1.3.4 Sync Encoding. This test verifies the ability of the UUT to recognize sync errors. The sync pattern, as defined for this test, is a waveform with six 0.5 us divisions. The divisions are represented as a 1 or 0 to indicate the polarity of each division of each division on the data bus. A proper command sync is represented as 111000 and a proper data sync is represented as 000111.

5.2.1.3.4.1 Transmit Command Word. This test shall verify that the UUT rejects transmit commands with invalid sync waveforms. The test sequence as defined in 5.2.1.3 shall be performed with a sync error encoded

in a transmit command word for test step 2. The test sequence shall be performed for each of the following invalid sync patterns:

111100,110000,111001,000111

The pass criteria for this test shall be: step 1- CS; step 2- NR; step 3- CS.

5.2.1.3.4.2 Receive Command Word. This test shall verify that the UUT rejects receive commands with invalid sync waveforms. The test sequence as defined in 5.2.1.3 shall be performed with a sync error encoded in a receive command word for test step 2. The test sequence shall be performed for each of the following invalid sync patterns:

111100,110000,111001,011000,000111

The pass criteria for this test shall be: step 1- CS; step 2- NR; step 3-CS.

5.2.1.3.4.3 Data Word This test shall verify that the UUT rejects invalid data sync waveforms. Perform the test sequence as defined in 5.2.1.3 with a sync error encoded into each data word for test step 2. The message is a valid receive command word and the maximum number of data words that the UUT is designed to receive. Only one data word per message shall have an invalid sync encoded into it. The test sequence shall be performed N times for each of the following invalid sync patterns: where N equals the maximum number of data words in the message.

000011,001111,000110,100111,111000

The pass criteria for this test shall be: step 1- CS; step 2- NR; step 3- ME.

Note: Data words shall not be encoded such that bit times 4 thru 8 match the terminal address of the UUT or be 11111 when the invalid data sync pattern 111000 is being used.

5.2.1.3.5 Message Length. These tests shall verify that the UUT properly detects an error when an incorrect number of data words are received.

5.2.1.3.4.1 Transmit Command. This test verifies the ability of the UUT to respond properly if the data word is contguous to a transmit command word. perform the test sequence as defined in 5.2.1.3 with a data word contiguously following a transmit command word for test step 2.

The pass criteria for this test shall be: step 1- CS; step 2- NR; step 3- ME.

5.2.1.3.5.2 Receive Command. This test shall verify that the UUT recognizes an error in the number of data words that are received. Perform the test sequence as defined in 5.2.1.3 with a data word count error in a receive message for test step 2. This message is a valid legal receive command word with the word count field equal to the maximum number of data words that the UUT is designed to receive but with a different number of data words than specified in the command word. The test sequence shall be performed N+1 times, where N equals the maximum number of data words. The first sequence shall have N+1 data words. The second sequence shall have N-1 data words and each of the remaining sequence shall remove one additional data word until the number of data words equals zero.

The pass criteria shall be: step 1- CS; step 2- NR; step 3- ME.

5.2.1.3.5.3 Mode command Word Count Error. This test verifies the ability of the UUT to respond properly when an incorrect number of words are sent with a mode command. Perform the test sequence defined in 5.2.1.3 using valid receive mode command in step 2 which would normally have an associated data word transmitted with it, but send the number of data words equal to the mode code value used. Repeat the test

sequence with the same mode command but with no data word in step 2. Repeat the test sequence using a valid transmit mode command except send a data word contiguously following the command word.

In all three cases the pass criteria shall be: step 1 -Cs; step 2- NR; step 3- ME.

5.2.1.3.5.4 RT to RT Word Count Error. This test verifies the ability of the UUTto respond properly when an incorrect number of words are sent to it as a receiving RTduring an RT to Retransfer. Perform the following test sequence.

Step 1 Send a valid legal RT to RT command pair followed in 4.0 to 12.0 us by a valid status word and N data words to the UUT, where N is the number of data words requested in the transmit command.

Step 2 Send the same RT to RTcommand pair followed in 4.0 to 12.0 us by a valid status word and N-1 data words.

Step 3 A transmit status mode command shall be sent to the receiving RT.

Step 4 Repeat steps 1 through 3 using a word count of N+1 in step 2.

The pass criieria in both cases shall be that the receiving RT's status is: step 1 -CS; step 2- NR; step 3- ME.

5.2.1.3.6 Contiguous Data. This test verfies that the UUT recognizes discontinuous data in a message. Perform the test sequence as defined in 5.2.1.3 with a 4.0 us data word gap error in a receive message for test step 2. The gap is measured as on figure 7. The receive message shall be a receive command with the maximum number of data words that the UUT is designed to receive with a gap between the command word and the first data word or between a data word pair. The test sequence shall be performed N times, where N equals the maximum number of data words. Only one gap time insertion is allowed per message.

The pass criteria for this test shall be: step 1 -CS; step 2- NR; step 3- ME.

5.2.1.3.7 Terminal Fail-Safe. The purpose of this testis to verify that the terminal fail-safe timer is properly implemented in the UUT. The UUT is required to contain a hardware implemented timer that will cause the transmitter to shutdown if the UUT transmits a message longer than 800.0 us. A fail-safe time-out occurring on one bus shall not affect the transmitter on any other bus. The reception of a valid command on the bus on which the time-out has occurred shall enable the transmitter. The test sequence below shall be performed for each bus:

Step 1. Initiate a condition in the UUT which causes the fail-safe timer to timeout. Measure the duration of the transmission.

Step 2. Remove the condition initiated in step 1.

Step 3. Send the UUT a valid legal message over the bus on which the time-out has occurred.

The pass criteria shall be that the timeout in step 1 occurs and the transmitter is shut down allowing the total transmission time to be between 660.0 us and 800.0 us. The response of the UUT in step 3 shall be CS. Record the measure dparameter at which the fail-safe time-out occurs. For test failures, record the test parameters at which the failure occurred.

5.2.1.4 Superseding Commands. This test verifies that the UUT will not malfunction and responds properly to possible occurrences of superseding commands. The following test sequence shall be used for this test.

Step 1. A valid legal receive message shall be sent to the UUT with the maximum number of words that the UUT is designed to receive encoded in the word count field.

Step 2. Before step 1 is completed, a superseding message shall be sent to the UUT.

Step 3. A transmit status mode command shall be sent to the UUT.

Record the UUT's response to each step when the test is performed with the following superseding command formats (step 2):

a. After at least one data word is transmitted in step 1, but before the last data word is transmitted, follow the selected data word with a gap of 4.0 us (reference figure 7), then a valid legal transmit command requesting the maximum number of data words that the UUT is designed to transmits.

b. Proceed as in "a" above, except transmit a valid legal transmit status mode command as the superseding command.

c. After at least one data word is transmitted in step 1, but before the last data word is transmitted, follow the selected data word contiguously with a valid legal transmit command requesting the maximum number of data words that the UUT is designed to transmit.

d. After the last data word is transmitted in step 1 follow it contiguously with a valid legal transmit command requesting the maximum number of data words that the UUT is designed to transmit.

The pass criteria shall be:

For a, step 1- NR, step 2- CS, step 3- CS
For b, step 1- NR, step 2- ME, step3 -ME
For e, step 1- NR, step 2- NR, step 3 -ME or, step 1- NR, step 2- CS, step 3- CS
For d, step 1- NR, step 2- CS, step 3- CS or, step 1- NR, step 2- NR, step 3- ME

For test failures, record the test parameters for which the failure occurred.

5.2.1.4.1 RT to RT Superseding Command. The purpose of this test is to verify that the UUT will not malfunction and responds properly to a superseding command when operating as the receiving RT in a RT to RT transfer.

Step 1. Send a valid legal RT to RT command pair followed in 4.0 to 12.0 us by a valid status word and N data words to the UUT, where N is the number of data words indicated in the receive command.

Step 2. Send the same RT to RTcommand pair followed in 4.0 to 12.0 us by a valid legal transmit command addressed to the UUT.

Step 3. A transmit status mode command shall be sent to the UUT.

The pass criteria for this test shall be: step 1- CS, step 2- CS, step 3- CS.

5.2.1.5 Required Mode Commands. The purpose of these tests is to verify that the UUT responds properly to the required mode commands. The tests are not intended to verify the mission aspects stated in the equipment specification. The UUTshall be tested for each required mode code with a subaddress field mode code indicator of all zeros and repeated with a subaddress field of all ones.

The pass criteria is defined in each test paragraph. If any test fails, record the UUT response to that test.

5.2.1.5.1 Transmit Status. The putpose of this testis to verify that the UUT has the ability to recognize the transmit status mode command and to transmit its last status word. The following sequence shall be performed:

Step 1. A valid legal message shall be sent to the UUT on the primary bus.

Step 3. A valid legal message shall be sent to the UUT on the alternate bus.

Step 4. A transmit status mode command shall be sent to the UUT on the alternate bus.

Step 5. A valid legal receive command with a parity error is a data word shall be sent on the primary bus.

Step 6. A transmit status mode command shall be sent to the UUT on the primary bus.

Step 7. Repeat step 6.

Step 8. Repeat step 4.

Step 9 Repeat step 1.

Step 10. Repeat step 2.

Step 11. Repeat step 4.

The pass criteria for each of the above steps shall be as follows: step 1- CS; step 2- CS; step 3- CS; step 4- CS; step 5- NR; step 6- ME; step 7- ME; step 8- ME; step 9- CS; step 10- CS; step 11- CS.

5.2.1.5.2 Transmitter Shutdown and Override. This test shall verify that the UUT recognizes the dual redundant mode commands to shutdown the alternate bus transmitter and to override the shutdown. In a dual redundant system each bus must be tested as the alternate bus and as the primary bus. A valid legal transmitter shutdown mode command shall be sent to the UUT to cause an alternate bus transmitter shutdown. A valid legal override transmitter shutdown mode command shall be sent to the UUT to cause an override of the transmitter shut-down. The following test sequence shall be used for each case including verification of the UUT response indicated.

Step 1. A valid legal command shall be sent on the primary bus to the UUT.

Step 2. A valid legal command shall be sent on the alternate bus to the UUT.

Step 3. A valid legal transmitter shutdown mode command shall be sent to the UUT on the primary bus.

Step 4. A valid legal command shall be sent on the alternate bus to the UUT.

Step 5. A valid legal command shall be sent on the primary bus to the UUT.

Step 6. A valid legal override transmitter shutdown mode command shall be sent to the UUT on the alternate bus.

Step 7. A valid legal command shall be sent to the UUT on the alternate bus.

Step 8. A valid legal override transmitter shutdown mode command shall be sent to the UUT on the primary bus.

Step 9. A valid legal command shall be sent on the alternate bus to the UUT.

Step 10. A valid legal command shall be sent on the primary bus to the UUT.

The pass criteria for each of the above steps shall be as follows: step 1- CS; step 2- CS; step 3- CS; step 4- NR; step 5- CS; step 6- NR; step 7- NR; step 8- CS; step 9- CS; step 10- CS.

5.2.1.5.3 Reset Remote Terminal. The purpose of this test is to verify that the UUT has the ability to recognize and properly operate when the reset remote terminal mode command is received. Note that this test provides characterization of reset time as a first step. If the reset time is variable, the test must be performed with conditions in the UUT set such that a maximum reset time results. The following sequence shall be performed.

Step 1. A reset remote temrinal mode command shall be sent to the UUT on one bus.

Step 2. After time T from step 1, as measured per figure 7, a valid legal command shall be sent to the UUT on the same bus.

Starting with time T_R not less than 5 ms, repeat step 1 and step 2 while decreasing time T to 4.0 us in steps no greater than 10.0 us.

The minimum time, T_R, between step 1 and step 2, as measured per figure 7, in which the UUT's response to step 2 is CS (with busy bit reset), shall be recorded.

Step 3. A valid legal transmitter shutdown mode command shall be sent to the UUT on the same bus.

Step 4. A valid legal command shall be sent to the UUT on the alternate bus.

Step 5. A reset remote terminal mode command shall be sent to the UUT on the first bus.

Step 6. After an intermessage gap to T_R, a valid legal command shall be sent to the UUT on the alternate bus.

The pass criteria for each of the above steps shall be as follows: step 1- CS; step 2- CS (with BUSY bit rest) for all time T >5.0 ms, and CS or NR for T <5.0 ms; step 3-CS; step 4- NR; step 5- CS; step 6- CS.

Having established the time, T_R, that the UUT requires in order to complete its reset function, the following sequence shall be performed.

Step 7. A reset remote terminal mode command shall be sent to the UUT on one bus.

Step 8. Send a valid legal receive command to the UUT on the same bus time T after the status response in step 7, where (T_R-40.0 us < T < (T_R-20.0 us), but not less than 4 us, as measured in figure 7

Step 9. Send a valid legal command to the UUT on the same bus time T after the status response in step 8 (if the response of the UUT during the reset period is NR, then time T shall be measured after the last data word of step 8), where 4.0 us< T < 5.0 us, as measured in figure 7.

The pass criteria for each of the above steps shall be as follows: step 7- CS; step 8- CS or NR, step 9- CS (with BUSY bit reset).

5.2.1.6 Data Wrap-Around. The purpose of this testis to verify that the UUT properly implements the data wrap-around capability. The following sequence shall be performed 10,000 times, with random data patterns for each data word in each sequence. The messages used shall contain the maximum number of data words that the RT is capable of transmitting or receiving, e.e., Record the number of correct responses and the number of incorrect repsonses.

Step 1. Send a receive message to the UUT at subaddress 30 (11110) or the appropriate receive wrap-around subaddress defined for the UUT.

Step 2. Send a transmit command to the UUT with the appropriate transmit wrap-around subaddress and with the same word coundt as step 1.

The pass criteria shall be: step 1- CS; step 2- CS with each data word having the same bit pattern as the corresponding data word in step 1.

5.2.1.7 RT to RT Message Errors. The purpose of this test is to examine the UUT's response to specific errors in the message stream when operating as the receiving RT in an RT to RT transfer. For these tests, the bus tester shall act as the bus controller and the transmitting remote terminal as required.

5.2.1.7.1 RT to RT Timeout. The purpose of this test is to verify that the UUT functions properly when operating as the receiving RT in a Retransfer. The UUT must not respond after receiving a RT to RT command pair if the data is not received within 54 us to 60 us as shown on figure 8. This is measured from the zero crossing of the parity bit of the receive command to the mid sync zero crossing of the first data word. The following test sequence shall be performed:

Step 1. Send a valid legal RT to RT command pair followed in 4.0 μs to 12.0 μs by a valid status word with the RT address of the transmit command and the proper number of data words shall be sent to the UUT.

Step 2. Send a transmit status mode command to the UUT.

Repeat step 1 and step 2 incrementing the time in step 1 between the transmit command and the status word in no greater than 0.5 μs increments until the time is equal to 30.0 μs.

When the UUT (receiving RT) stops responding, the time T, as specified in figure 8, shall be measured and recorded.

The pass criteria shall be: step 1- CS for T < 54.0 ps, CS or NR for 54.0 < T <60.0 μs, and NR for T > 60.0 us; step 2- CS if step 1 is CS, ME if step 1 is NR.

5.2.1.7.2 RT to RT message format errors. The purpose of this test is to verify that the UUT will not malfunction and responds properly to errors in the message stream associated with the transmitting RT when the UUT is the receiving RT in a RT to RT transfer. The following test sequence shall be used:

Step 1. Send a valid legal RT to RT command pair followed in 4.0 to 12.0 μs by a valid status word and N data words to the UUT, where N is the number of data words indicated in the receive command.

Step 2. Send the same RT to RT message as in steps 1 injecting one of the errors indicated below.

Step 3. Send a transmit status mode command to the UUT.

Record the UUT's response to each step when the test is performed with each of the following format errors (step 2):

a. Invalid transmit command word. Inject an invalid sync pattern in the transmit command word followed in 4.0 to 12.0 μs with a receive command with the same address as the transmit command followed by N data words and no status response. This command combination will appear to the UUT as the same message format in step 1 with an invalid transmitting RT's command word.

b. Invalid transmitting RT's status word. Inject an invalid sync pattern in the transmitting RT's status word.

c. Wrong sync type in the transmitting RT's status word. Send the same RT to RT command pair as in step 1 followed in 4.0 to 12.0 μs by N+1 data words.

The pass criteria for each of the test formats shall be as follows: step 1- CS; step 2- NR, step 3 ME.

5.2.1.7.3 Transmitting RT errors. The purpose of this test is twofold: first to determine whether the UUT verifies the proper occurrence of the transmitting RTs command and status word and, secondly, to verify that the UUT will not malfunction and responds properly to errors in the message stream associated with the transmitting RT when the UUT is the receiving RT in an RT to Retransfer. Although recommended by Notice 2, the standard does not require the receiving RT to verify the proper occurrence of the transmitting RTs command and status word. Therefore, the first purpose of this test is for characterization of the UUT only. The following test sequence shall be used:

Step 1. Send a valid legal RT to RT command pair followed in 4.0 to 12.0 μs by a valid status word and N data words to the UUT, where N is the number of data words indicated in the receive command.

Step 2. Send the same RT to RT command pair as in step 1 followed in 4.0 to 12.0 μs by a status word containing a terminal address different from both the transmit command and the UUT, followed by N data words.

Step 3. A transmit status mode command shall be sent to the UUT.

The pass criteria shall be the following: step 1- CS; step 2- CS or NR, step 3- CS if step 2 is CS; ME if step 2 is NR.

5.2.1.8 Bus Switching. This test shall be performed only if the UUT is configured with dual redundant buses. This test verifies that the dual redundant remote terminal properly performs the bus switching requirements of MIL-STD-1553 (para on "Data Bus Activity"). The requirements are as follows:

a. If the UUT is receiving or operating on a message on one bus, and another valid, legal command to the UUT occurs on the opposite bus later in time, then the UUT is required to reset and respond appropriately to the later command on the opposite bus.

b. An invalid command on the alternate bus shall not affect the response of the UUT to commands on the original bus.

Unless otherwise specified, legal messages are used in this test. The interrupting message on the alternate bus shall be swept through the command word, the response time gap, the UUT's status status word, and the UUT's data transmission on the first bus. For all tests, record the command words used. The following test sequences shall be performed twice for each interrupting command, once for each redundant bus.

RT transmitting:

Step 1. Send a valid transmit command to the UUT requesting the maximum number of data words that the UUT is designed to transmit.

Step 2. Send the interrupting command on the alternate bus beginning 4.0 μs after the beginning of the first command.

Step 3. Send a valid transmit status mode command after the messages on both buses have been completed.

Step 4. Repeat step 1 through step 3 increasing the time between step 1 and step 2 in no greater than 0.25 μs increments until the messages no longer overlap.

Perform the test with the following interrupting messages for step 2.

a. A valid legal message

b. A message with a parity error in the command word.

c. A valid message with a terminal address different than that of the UUT.

The pass criteria shall be: for a, step 1- NR, truncated message or CS, step 2- CS and step 3- CS; and for b and c, step 1 CS; step 2- NR and step 3- CS. For test failures, record the test parameters at which the failure occurred.

RT receiving:

Step 1. Send a valid RT to RT message command to the UUT and a second RT with the UUT the receiving terminal with the maximum number of data words that the UUT is designed to receive.

Step 2. Send the interrupting command on the alternate bus beginning 4.0 us after the beginning of the first command.

Step 3. Send a valid transmit status mode command after the messages on both buses have been completed.

Step 4. Repeat step 1 through step 3 varying the time between step 1 and step 2 in no greater than 0.25 us increments until the messages no longer overlap.

Perform the test with the following interrupting messages for step 2.

a. A valid legal messasge

b. A message with a parity error in the command word.

c. A valid messag with a terminal address different than that of the UUT.

The pass criteria shall be: for a, step 1- NR or CS, step 2- CS and step 3- CS; and for b and c, step 1- CS, step- NR and step 3- CS. For test failures, record the test parameters at which the failure occurred.

5.2.1.9 Unique Address. The purpose of this test is to verify that the UUT can be assigned any unique address from an external connector on the UUT. The following sequence shall be performed for the UUT:

Step 1. Send a valid, legal command to the UUT.

Step 2. Repeat step 1 thirty-one times with the same command word except use all other possible bit combinations in the RT address field of the command word.

Step 3. Repeat step 1 and step 2 after externally changing the RT address for all possible combinations from 00000 thru 11110.

Step 4. After externally changing the RT address to simulate a single point address validation failure (e.g., parity error on the address lines), repeat step 1 and step 2.

The pass criteria shall be: step 1- CS; step 2- NR for each combinations; step 3- same as step 1 and step 2; step 4- NR for each combination.

Note: Power cycling may be required after externally changing the RT address.

5.2.2 Optional Operation. This section provides for testing the optional requirements of MIL-STD-1553. If a remote terminal implements any of the options, it shall be tested in accordance with the test herein identified for the option. If the transmit status mode command shall be used.

5.2.2.1 Optional Mode Commands. The purpose of these tests is to verify that the UUT responds properly to implemented mode commands. The tests are not intended to verify the mission aspects stated in the equipment specification. The UUT shall be tested for each mode code implemented with a subaddress field mode code indicator of all zeros and repeated with a subaddress field of all ones.

The pass criteria is defined in each test paragraph. If any test fails, record the UUT repsonse to that test.

5.2.2.1.1 Dynamlc Bus Control. The purpose of this test is to verify that the UUT has the ability to recognize the dynamic bus control mode command and to take control of the data bus. A valid legal dynamic bus control mode command shall be sent to the UUT. The UUT shall take control of the data bus when its response is DBA as required in the UUT's design specification.

The pass criteria shall be that the UUT respond with a DBA upon acceptance of bus control or a CS upon rejection of bus control.

5.2.2.1.2 Sychronize. The following paragraphs provide the test criteria for the synchronize mode commands.

5.2.2.1.2.1 Synchronize (without data word). The purpose of this test is to verify that the UUT has the ability to recognize a synchronization mode command without using a data word. A valid legal synchronize (without data word) mode command shall be sent to the UUT.

The pass criteria shall be that the UUT respond with CS.

5.2.2.1.2.2 Synchronize (with data word. The purpose of this test is to verify that the UUT has the ability to recognize a synchronization mode command which uses a data word. A valid legal synchronize (with data word) mode command shall be sent to the UUT.

The pass criteria shall be that the UUT respond with CS.

5.2.2.1.3 Initiate Self-Test. The purpose of this test is to verify that the UUT has the ability to recognize and properly operate when the initiate self-test mode command is received. Note that this test provides characterization of self-test time as a first step. If the self-test time is variable, the test must be performed with conditions in the UUT set such that a maximum self test time results. The following sequences shall be performed:

Step 1. An initiate self-test mode command shall be sent to the UUT on one bus.

Step 2. After time T from step 1, as measured per figure 7, a valid legal command shall be sent to the UUT on the same bus.

Starting with time T not less than 100 ms, repeat step 1 and step 2 while decreasing time T to 4.0 us in steps no greater than 1.0 ms. Finer granularity, 10.0 us maximum steps, shall be used to more accurately determine the self-test time when the time of self-test is determined using the coarser steps.

The minimum time T_s between step 1 and step 2, as measured per figure 7 in which the UUT's response to step 2 is CS (with BUSY bit reset), shall be recorded.

The pass criteria for each of the above steps shall be as follows: step 1- CS; step 2- CS (with BUSY bit reset) for all time $T \geq 100$ ms, and CS or NR for time $T \leq 100$ ms.

Having established the time, T_s, that the UUT requires in order to complete its self-test function, the following sequence shall be performed.

Step 3. An initiate self-test mode command shall be sent to the UUT on one bus.

Step 4. Send a valid legal receive command to the UUT on the same bus time T after the status response in step 3, where (T_s-40.0 us) $\leq$ T $\leq$ (T_s-20.0 us), but not less than 4.0 us, as measured in figure 7.

Step 5. Send a valid legal command to the UUT on the same bus time T after the status response in step 4 (if the response of the UUT during the reset period is NR, then time T shall be measured after the last data word of step 4), where 4.0 us $\leq$ T $\leq$ 5.0 us, as measured in figure 7.

The pass criteria for each of the above steps shall be as follows: step 3- CS, step 4- CS or NR, step 5- CS (with BUSY bit reset).

5.2.2.1.4 Transmit BIT Word. The purpose of this test is to verify that the UUT has the ability to recognize this mode command. A valid legal transmit BIT mode command shall be sent to the UUT.

The pass criteria shall be that the UUT respond with CS.

5.2.2.1.5 Selective Transmitter shutdown and Override. This test shall verify that the UUT recognizes the muiti-redundant mode code commands to shut down a selected bus transmitter and to override the shutdown. in a multi-redundant system, each bus must be tested as the primary bus with the remaining busses as alternate busses. A valid legal selected transmitter shutdown mode command shall be sent to the UUT accompanied by the appropriate data word to cause a selective bus transmitter shutdown. A valid legal override selected transmitter shutdown mode command shall be sent to the UUT accompanied by the appropriate data word to cause an override of the selected bus transmitter shutdown. The following test sequence shall be performed using each bus as the primary bus and each of the remaining busses in turn as the alternate bus, including verification of the UUT response indicated.

Step 1. A valid legal command shall be sent on the first bus to the UUT.

Step 2. A valid legal command shall be sent on the alternate bus to the UUT.

Step 3. A valid legal selected transmitter shutdown mode command shall be sent to the UUT on the first bus with the data word encoded to shutdown the alternate bus.

Step 4. A valid legal command shall be sent on the alternate bus to the UUT.

Step 5. A valid legal command shall be sent on the first bus to the UUT.

Step 6. A valid legal override selected transmitter shutdown mode command shall be sent to the UUT on the alternate bus with the same data word as sent in step 3.

Step 7. A valid legal command shall be sent to the UUT on the alternate bus.

Step 8. A valid legal override selected transmitter shutdown mode command shall be sent to the UUTk on the first bus with the same data word as sent in step 3.

Step 9. A valid legal command shall be sent on the alternate bus to the UUT.

Step 10. A valid legal command shall be sent on the first bus to the UUT.

Step 11. Repeat step 3 except that the data word shall be encoded with a bit pattern that would normally shutdown the first bus if it was sent on the alternate bus.

Step 12. Repeat step 4.

Step 13. Repeat step 5.

The data words associated with step 3 and step 11 for each bus shall be recorded.

The pass criteria for each of the above steps shall be as follows: step 1- CS, step 2- CS, step 3- CS, step 4- NR, step 5- CS, step 6- NR, step 7- NR, step 8- CS, step 9- CS, step 10- CS, step 11- CS, step 12—CS, step 13- CS.

5.2.2.1.6 Terminal Flag Bit Inhibit and Override. This test verifies that the UUT recognizes and responds properly to the mode code commands of inhibit terminal flag bit and override inhibit terminal flag bit. Beginning in step 2 of the test sequence below, the UUT shall be caused to set the terminal flag bit.

Step 1. A valid legal receive command with at least one data word shall be sent to the UUT.

Step 2. Procedures as defined for the UUT, shall be performed that will set the terminal flag in the UUT status response. Send a valid legal receive command with at least one data word to the UUT.

Step 3. A valid legal inhibit terminal flag mode code command shall be sent to the UUT.

Step 4. Repeat step 1.

Step 5. A valid legal override inhibit terminal flag mode code command shall be sent to the UUT.

Step 6. A valid legal receive command with at least one data word shall be sent to the UUT.

Step 7. Procedures, as defined for the UUT, shall be performed which resets the TF bit.

Step 8. Repeat step 1.

The pass criteria for each of the above steps shall be as follows: step 1- CS, step 2- TF, step 3- CS or TF, step 4- CS, step 5- CS or TF, step 6- TF, step 8- CS.

5.2.2.1.7 Transmit Vector Word. This test verifies the capability of the UUT to recognize and respond properly to a transmit vector word mode code command. A valid legal transmit vector word mode code command shall be sent to the UUT.

The pass criteria shall be that the UUT repsond with CS.

5.2.2.1.8 Transmit Last Command.. This test verifies that the UUT recognizes and responds properly to a transmit last command mode code. The following test sequence shall be used:

Step 1. A valid legal receive command with at least one data word shall be sent to the UUT.

Step 2. A valid legal receive command different from that used in step 1 above with at least one data word shall be sent to the UUT and a parity error shall be encoded into the first data word.

Step 3. A valid transmit last command mode command shall be sent to the UUT.

Step 4. A valid transmit status mode command shall be sent to the UUT.

Step 5. A valid legal transmit last command mode command shall be sent to the UUT.

Step 6. A valid legal transmit last command mode command shall be sent to the UUT.

Step 7. A valid legal receive command with at least one data word shall be sent to the UUT.

Step 8. A valid legal transmit last command shall be sent to the UUT.

Step 9. A valid legal transmit command shall be sent to the UUT.

Step 10. A valid legal transmit last command mode command shall be sent to the UUT.

The pass criteria for each of the above steps shall be as follows: step 1- CS; step 2- NR; step 3- ME, followed by a data word containing the command word from step 2; step 4-ME; step 5- ME, followed by a data word containing the command word form step 4; step 6- ME, followed by a data word containing the command word from step 4; step 7- CS; step 8- CS, followed by a data word containing the command word form step 7; step 9- CS; step 10- CS, followed by a data word containing the command word from step 9.

5.2.2.2 Status Word Bits. The following tests verify that all implemented status code bits are properly used and cleared. Implementation of all status code bits in the status word except the ME bit is optional. In addition to the separate tests, for each of the following status bits: service request, busy, subsystem flag, and terminal flag, provide the analysis as listed below.

a. What conditions set the status bit in the status word transmitted on the data bus.

b. What conditions reset the status bit in the status word transmitted on the data bus.

c. If the condition specified in item a. occurred and disappeared without intervening commands to the UUT, list the cases where the status bit is set and reset in response to a valid, non-mode command to the UUT.

d. Given that the status bit was set, and the condition which set the bit has gone away, list the cases where the status bit is still set in response to the second valid, non-mode command to the UUT.

The UUT has failed a test sequence if it does not respond as indicated in each of the separate tests below.

5.2.2.2.1 Service Request. This test verifies that the UUT sets the service request bit as necessary and clears it when appropriate. The UUT shall set bit time eleven of the status word when a condition in the UUT warrants the RT to be serviced. A reset of the bit shall occur as defined by each RT. The following steps shall be performed and the appropriate responses verified.

Step 1. A valid legal receive command with at least one data word shall be sent to the UUT.

Step 2. Acondition which causes the service request bit to be set shall be introduced into the UUT. A valid legal command that does not servce the request shall be sent to the UUT.

Step 3. A valid legal command that does not service the request shall be sent to the UUT.

Step 4. Procedures, as defined for the UUT, shall be performed which resets the service request bit.

Step 5. A valid legal receive command with at least one data word shall be sent to the UUT.

The pass criteria for each of the above steps shall be as follows: step 1- CS, with the service request bit reset; step 2- SRB; step 3- SRB; step 5- CS, with the service request bit reset. All commands and UUT responses shall be recorded.

5.2.2.2.2 Broadcast command Received. This test verifies that the UUT sets the broadcast command received bit of the status word after receiving a broadcast command. The UUT shall set status bit fifteen to a logic one after receiving the broadcast command. The following test sequence shall be performed using either the transmit last command or transmit status mode code command to verify the bit condition.

Step 1. A valid legal broadcast receive message shall be sent to the UUT.

Step 2. A valid legal transmit last ocmmand shall be sent to the UUT.

Step 3. A valid, legal, non-broadcast command shall be sent to the UUT.

Step 4. Repeat step 1.

Step 5. Repeat step 3.

Step 6. Deleted.

Step 7. Deleted.

The pass criteria for each of the above steps shall be as follows: step 1- NR; step 2- BCR, and the data word contains the bit pattern of the command word in step 1; step 3- CS; step 4- NR; step 5- CS; step 6- NR; step 7-ME and BCR, and the data word contains the bit pattern of the command word in step 6. All commands and UUT responses shall be recorded.

5.2.2.2.3 Busy. This test verifies the capability of the UUT to set the busy bit of the status word. Bit time sixteen of the status word shall be set when the UUT is busy. Prior to performing the test sequence below, a condition which sets the busy bit must be received.

Step 1. A valid legal transmit command shall be sent to the UUT.

Step 2. Procedures, as defined for the UUT, shall be peformed which resets the busy bit.

Step 3. A valid legal transmit command shall be sent to the UUT.

The pass criteria for each of the above steps shall be as follows: step 1- BUSY; step 3- CS. All commands and UUT responses shall be recorded.

5.2.2.2.4 Subsystem Flag. This test verifies the capability of the UUT to set the subsystem flag of the status word. Bit time seventeen of the status word shall be set to a logic one when a subsystem fault has been determined fault has been determined. Prior to performing the test sequence below, a condition which sets the subsystem flag bit must be activated.

Step 1. A valid legal transmit command shall be sent to the UUT.

Step 2. Remove the condition which sets the subsystem flag bit. Cycling powertothe UUTshall not be part of these procedures to reset the SF bit.

Step 3. A valid legal transmit command shall be sent to the UUT.

Step 4. Repeat step 3.

The pass criteria for each of the above steps shall be as follows: step 1- SF; step 3- CS; step 4- CS. All commands and UUT responses shall be recorded.

5.2.2.2.5 Terminal Flag. This test verifies that the UUT sets the terminal flag bit as necessary and clears it when appropriate. The UUT shall set bit time nineteen of the status word when an occurrence in the UUT shall set causes a terminal fault condition. Prior to performing the test sequence below, a condition which sets the terminal flag bit must be activated.

Step 1. A valid legal receive command with at least one data word shall be sent to the UUT.

Step 2. Remove the condition which sets the terminal flag bit. Cycling power to the UUT shall not be part of this procedure.

Step 3. A valid legal transmit command shall be sent to the UUT.

Step 4. Repeat step 3.

The pass criteria for each of the above steps shall be as follows: step 1- TF; step 3- CS or TF; step 4- CS. All commands and UUT responses shall be recorded.

5.2.2.3 Illegal Command. This test verifies that the UUT recognizes and responds properly to illegal commands when the illegal command detection option is implemented. The following sequence shall be performed:

Step 1. Send an illegal receive command to the UUT.

Step 2. Send a transmit status mode command to the UUT.

Step 3. Send a valid legal transmit command to the UUT.

Step 4. Send an illegal receive command to the UUT with a parity error in one of the data words.

Step 5. Send a transmit status mode command to the UUT.

Step 6. Repeat step 3.

Step 7. Send an illegal transmit command to the UUT.

Step 8. Send a transmit status mode command to the UUT.

Step 9. Repeat step 3.

Step 10. Send an illegal command to the UUT with a parity error in the command word.

Step 11. Send a transmit last command mode command to the UUT. If the transmit last command mode command is not implemented in the RT, send a transmit status mode command instead.

The pass criteria shall be: step 1- ME; step 2- ME; step 3- CS; step 4- NR; step 5- ME; step 6- CS; step 7- status only with ME bit set; step 8- ME; step 9- CS; step 10- NR; step 11- CS, if the transmit last command mode command was used, the data word shall be the command word sent in step 9.

5.2.2.4 Broadcast Mode Command. The purpose of this testis to verify that the UUT responds properly to implemented broadcast mode commands. This test is not intended to verify the mission aspects stated in the equipment specification. The UUT shall be tested for each mode code implemented with a subaddress field mode code indicator of all zeros and repeated with a subaddress field of all ones. Use the following test sequence unless otherwise noted.

Step 1. A valid receive message shall be sent to the UUT.

Step 2. A valid legal broadcast message shall be sent to the UUT.

Step 3. A transmit last command mode command shall be sent to the UUT.

5.2.2.4.4 Broadcast Transmitter Shutdown and Override. The purpose of this text is to verify that the UUT has the ability to recognize and properly execute these broadcast mode commands. The pass criteria for each individual test is contained in the paragraph below.

The following sequence shall be performed for each test:

Step 1. A valid legal command shall be sent on the first bus to the UUT.

Step 2. A valid legal command shall be sent on the alternalte bus to the UUT.

Step 3. A valid legal broadcast transmitter shutdown command shall be sent to the UUT on the first bus.

Step 4. A transmit last command mode shall be sent on the first bus to the UUT.

Step 5. A valid legal command shall be sent on the alternate bus to the UUT.

Step 6. A valid legal command shall be sent on the first bus to the UUT.

Step 7. A valid legal broadcast override transmite shutdown mode command shall be sent to the UUT on the alternate bus.

Step 8. A valid legal command shall be sent to the UUT on the alternate bus.

Step 9. A valid legal broadcast override transmitter shutdown mode command shall be sent to the UUT on the first bus.

Step 10. A transmit last command mode command shall be sent on the first bus to the UUT.

Step 11. A valid legal command shall be sent on the alternate bus to the UUT.

Step 12. A valid legal command shall be sent on the first bus to the UUT.

The pass criteria for each of the above steps shall be as follows: step 1-CS; step 2- CS; step 3- NR; step 4- BCR(and the data word contains the command word of step 3); step 5- NR; step 6- CS; step 7- NR; step 8- NR; step 9- NR; step 10- BCR (and the data word contains the command of step 9); step 11- CS; step 12- CS.

5.2.2.4.5 Broadcast Selective Transmitter Shutdown and Override This test shall verify that the UUT recognizes the multi-redundant broadcast mode code commands to shutdown a selected bus transmitter and to override the shutdown. In a multi-redundant system each bus must be tested as the primary bus with the remaining busses as alternate busses. A valid legal broadcast selected transmitter shutdown mode command shall be sent accompanied by the appropriate data word to cause a selectvie bus transmitter shutdown. A valid legal broadcast override selected transmitter shutdown mode command shall be sent accompanied by the appropriate data word to cause an override of the selected bus transmitter shutdown. The following test sequence shall be performed using each bus as the primary bus and each of the remaining busses in turn as the alternate bus, including verification of the UUT response indicated.

Step 1. A valid legal command shall be sent on the first bus to the UUT.

Step 2. A valid legal command shall be sent on the alternate bus to the UUT.

Step 3. A valid legal broadcast selected transmitter shutdown mode command shall be sent to the UUT on the first bus with the data word encoded to shutdown the alternate bus.

Step 4. A transmit last command mode shall be sent on the first bus to the UUT.

Step 5. A valid legal command shall be sent on the alternate bus to the UUT.

Step 6. A valid legal command shall be sent on the first bus to the UUT.

Step 7. A valid legal broadcast override selected transmitter shutdown mode command shall be sent to the UUT on the alternate bus with the same data word as sent in step 3.

Step 8. A valid legal command shall be sent to the UUT on the alternate bus.

Step 9. A valid legal broadcast override selected transmitter shutdown mode command shall be sent to the UUT on the first bus with the same data as sent in step 3.

Step 10. Repeat step 4.

Step 11. A valid Iegal command shall be sent on the alternate bus to the UUT.

Step 12. A valid legal command shall be sent on the first bus to the UUT.

Step 13. Repeat step 3 except that the data word shall been coded with a bit pattern that would normally shutdown the first bus if it was sent on the alternate bus.

Step 14. Repeat step 4.

Step 15. Repeat step 5.

Step 16. Repeat step 6.

The data words associated with step 3 and step 13 for each bus shall be recorded.

The pass criteria for each of the above steps shall be as follows: step 1- CS; step 2- CS; step 3- NR; step 4- BCR (and the data word contains the command word of step 3); step 5- NR; steP 6- CS; step7- NR; step 8- NR; step 9-NR; step 10- BCR (and the data word contains the command word of step 9); step 11- CS; step 12- CS; step 13- NR; step 14- BCR (and the data word contains the command word of step 13); step 15- CS step 16- CS.

5.2.2.4.6 Broadcast terminal flag bit inhibit and override. This test veri-fies that UUT recognizes and responds properly to the broadcast mode code commands of inhibit terminal flag bit and override inhibit terminal flag bit. Beginning in step 2 of the test sequence below, the UUT shall be caused to set the terminal flag bit.

Step 1. A valid legal receive command with at least one data word shall be sent to the UUT.

Step 2. Procedures, as defined for the UUT, shall be performed that will set the terminal flag in the UUT status response. Send a valid legal receive command with at least one data word to the UUT.

Step 3. A valid legal inhibit terminal flag broadcast mode code command shall be sent to the UUT.

Step 4. A transmit last command mode command shall be sent to the UUT.

Step 5. Repeat step 1.

Step 6. A valid legal override inhibit terminal flag broadcast mode code command shall be sent to the UUT.

Step 7. A transmit last command mode command shall be sent to the UUT.

Step 8. A valid legal receive command with at least one data word shall be sent to the UUT.

Step 9. Procedures, as defined for the UUT, shall be performed which resets the TF bit.

Step 10. Repeat step 1.

The pass criteria for each of the above steps shall be as follows: step 1- CS; step 2- TF; step 3- NR; step 4- BCR or (BCR and TF) and in either case the data word contains the command word of step 3; step 5- CS; step 6- NR; step 7- BCR or (BCR and TF) and in either case the data word contains the command word of step 6; step 8- TF; step 10- CS.

5.2.2.4.7 Broadcast reset remote terminal. The purpose of this test is to verify that the UUT has the ability to recognize the broadcast mode code com-mand to reset itself to a power up initialized state. The following sequence shall be performed:

Step 1. A broadcast reset remote terminal mode command shall be sent to the UUT on one bus.

Step 2. After time T from step 1, as measured per figure 7, a valid legal transmit command shall be sent to the UUT on the same bus.

Step 3. The time T shall be obtained by repeating step 1 and step 2 while varying the intermessage gap from 100.0 ms down to 4.0 us in the following steps: from 100.0 ms to 6 ms in no greater than 1.0 ms steps, and from 6.0 ms to 4.0 us in no greater than 10.0 us steps. When the time T is between 5.0 ms and 100.0 ms then in addition to each command sent in step 2, a minimum of one valid legal command shall be sent to the UUT positioned within 4.0 ms after step 1.

Step 4. A valid legal transmitter shutdown mode command shall be sent to the UUT on the same bus.

Step 5. A valid legal command shall be sent to the UUT on the alternate bus.

Step 6. A broadcast reset remote terminal mode command shall be sent to the UUT on the first bus.

Step 7. After 5 ms repeat step 5.

The minimum time between step 1 and step 2 as measured per figure 7 in which the UUT'S response to step 2 is CS (with BUSY bit reset), shall be recorded.

The pass criteria for each of the above steps shall be as follows: step 1- NR; step 2- CS (with BUSY bit reset) for all time T $\geq$ 5 ms and CS or NR for T < 5 ms; step 4- CS; step 5- NR; step 6- NR; step 7- CS.

5.2.2.4.8 Broadcast dynamic bus control. The purpose of this test is to insure that the UUT does not take over bus control function in response to a broadcast mode command. The following sequence shall be performed:

Step 1. A broadcast dynamic bus control mode command shall be sent to the UUT.

Step 2. A transmit status mode command shall be sent to the UUT.

The pass criteria shall be: step 1- NR; step 2- CS (the BCR bit shall be set, ME bit maybe set, but the DBA bit shall not be set).

5.2.2.5 Error injection-broadcast messages. The purpose of this test is to verify the UUT's response to data specific errors in broadcast messages. Unless otherwise noted, the following test sequence shall be used for all error injection tests. The error to be encoded in step 4 for a given message is specified in each test paragraph. The pass criteria is defined in each test paragraph. All responses shall be recorded.

Test sequence:

Step 1. A valid legal broadcast message shall be sent to the UUT.

Step 2. A transmit last command mode command shall be sent to the UUT.

Step 3. A valid legal receive message shall be sent to the UUT.

Step 4. A broadcast message containing the specified error shall be sent to the UUT.

Step 5. A transmitlast command mode command shall be sent to the UUT.

Step 6. Repeat Step 3.

5.2.2.5.1 Parity: bus controller (BC)-RT broadcast. The purpose of this test is to verify the UUT's capability to detect parity errors embedded in different words within a message.

5.2.2.5.1.1 Command word error. This test verifies the ability of the UUT to recognize a parity error in the broadcast command. The test sequence as defined in 5.2.2.5 shall be performed with a parity error encoded in a broad-cast command for test step 4.

The pass criteria for this test shall be: step 1- NR; step 2- BCR and the data word contains the command word of step 1; step 3- CS; step 4- NR; step 5- CS and the data word contains the command word of step 3; step 6- CS.

5.2.2.5.1.2 Data word error. This test verifies the ability of the UUT to recognize a parity error occurring in a data word. The test sequence as defined in 5.2.2.5 shall be performed with a parity error encoded in a data word for step 4. The message shall be a BC-RT (broadcast) command with the maximum number of data words that the UUT is designed to receive. The test sequence must be executed N times, where N equals the number of data words in the message. Each data word in the message will be transmitted with a pariiy error. Only one parity error is allowed per message.

The pass criteria for this test shall be: step 1- NR; step 2- BCR and the data word contains the command word of step 1; step 3- CS; step 4- NR; step 5-ME (BCR may beset) and the data word contains the command word of step 4; step 6- CS.

5.2.2.5.2 Message length. BC to RT broadcast. This test shall verify that the UUT recognizes an error in the number of data words that are received. Perform the test sequence as defined in 5.2.2.5 with the data word count error in a BC - RT (broadcast) message for test step 4. The message is a valid legal broadcast command word with the word count field equal to the maximum number of data words that the UUT is designed to receive and a different number of data words than specified in the command word. The test sequence shall be performed N+1 times, where N equals the maximum number of data words. The first sequence shall have N+1 data words. The second sequence" shall have N-1 data words. Other sequences shall remove one additional data word until the number of data words equals zero.

The pass criteria forth is test shall be: step 1- NR; step 2- BCR and the data word contains the command word of step 1; step 3- CS; step 4- NR; step 5-ME (BCR may beset) and the data word contains the command word of step 4; step 6- CS.

5.3 Noise Rejection Test. This test verifies the RT's ability cooperate in the presence of noise. The maximum word error rate for a RT is one part in 107. While performing this test, all words received by the UUT shall be in presence of an additive white Gaussian noise distributed over a bandwidth of 1.0 kHz to 4.0 MHz at an RMS amplitude of 140 mV for transformer could stubs or 200 mV for direct coupled stubs measured at point A of figure 9A or figure 10A. This test shall be conducted with a signal level of 2.1 V peak-to-peak, line-to-line, for transformer coupled stubs or 3.0 V peak-to-peak, line-to-line, for direct coupled submeasured at point A of figure 9A or figure 10A. The rise and fall time of the transmitted message (measured at a data bit zero crossing with the prior zero crossing and the next zero crossing at 500 ns intervals from the ensured zero crossing) measured at point "A" shall be 200.0 ns ± ns. Figure 9A and figure 10A depict the configurations for conducting the noise rejection test. Air force applications shall only use the configuration in figure 10A. Figure 9B and figure 10B depict suggest configurations for the noise rejection test. The noise test shall run continuously with intermessage gaps of $\geq$ 100.0 us until the total number of all words received by the UUT exceeds the required number for acceptance of the UUTor is less than the required number for rejection of the terminal, as specified in table Ill. All data words used in the tests shall contain random bit patterns. These bit patterns shall be unique for each data word in a message and shall change randomly from message to message. A unit under test (UUT) that provides transformer and direct coupled stubs shall be tested on both stubs. The noise test shall be performed on all buses for UUTs with redundant bus configurations

TABLE III. Criteria for Acceptance or Rejection of a Terminal for the Noise Rejection Tests

total number of words received by the terminal (in multiples of 10^7)

NO. OF ERRORS	REJECT (EQUAL OR LESS)	ACCEPT (EQUAL OR MORE)
0	N/A	4.40
1	N/A	5.21
2	N/A	6.02
3	N/A	6.83
4	N/A	7.64
5	N/A	8.45
6	0.45	9.27
7	1.26	10.08
8	2.07	10.89
9	2.88	11.70
10	3.69	12.51
11	4.50	13.32
12	5.31	14.13
13	6.12	14.94
14	6.93	15.75
15	7.74	16.56
16	8.55	17.37
17	9.37	18.19
18	10.18	19.00
19	10.99	19.81
20	11.80	20.62
21	12.61	21.43
22	13.42	22.24
23	14.23	23.05
24	15.04	23.86
25	15.85	24.67
26	16.66	25.48
27	17.47	26.29
28	18.29	27.11
29	19.10	27.92
30	19.90	28.73
31	20.72	29.54
32	21.53	30.35
33	22.34	31.16
34	23.15	31.97
35	23.96	32.78
36	24.77	33.00
37	25.58	33.00
38	26.39	33.00
39	27.21	33.00
40	28.02	33.00
41	33.00	N/A

APPENDIX A
TEST PLAN TO MIL-STD-1553B
CROSS REFERENCE

P = Primary Reference
R = Related Reference

Test Plan			MIL-STD-1553B
5.0	Detailed requirements		
5.1	Electrical tests		
5.1.1	Output characteristics		
5.1.1.1	Amplitude	(Transformer coupled)	4.5.2.1.1.1-P
		(Direct coupled)	4.5.2.2.1.1-P
5.1.1.2	Rise time/fall time	(Transformer coupled)	4.5.2.1.1.2-P
		(Direct coupled)	4.5.2.2.1.2-P
5.1.1.3	Zero crossing stability		
		(Transformer coupled)	4.5.2.1.1.2-P
		(Direct coupled)	4.5.2.2.1.2-P
5.1.1.4	Distortion, overshoot & ringing		
		(Transformer coupled)	4.5.2.1.1.2-P
		(Direct coupled)	4.5.2.2.1.2-P
5.1.1.5	Output symmetry	(Transformer coupled)	4.5.2.1.1.4-P
		(Direct coupled)	4.5.2.2.1.4-P
5.1.1.6	Output noise	(Transformer coupled)	4.5.2.1.1.3-P
		(Direct coupled)	4.5.2.2.1.3-P
5.1.1.7	Output isolation		4.6.1-P
			30.10.6-P
5.1.1.8	Power on/off		
5.1.1.8.1	Power on/off noise	(Transformer coupled)	30.10.6-P
		(Direct coupled)	30.10.6-P
5.1.1.8.2	Power on response		30.5.1-P
			3.16-R
5.1.1.9	Terminal response time		4.3.3.8-P
5.1.1.10	Frequency stability		4.3.3.3-P
5.1.2	Input characteristics		
		(Transformer coupled)	4.5.2.1.2-P
		(Direct coupled)	4.5.2.2.2-P
5.1.2.1	Input waveform compatibility		
		(Transformer coupled)	4.5.2.1.2.1-P
		(Direct coupled)	4.5.2.2.2.1-P
5.1.2.1.1	Zero crossing distortion		
		(Transformer coupled)	4.5.2.1.2.1-P
		(Direct coupled)	4.5.2.2.2.1-P
5.1.2.1.2	Amplitude variations		
		(Transformer coupled)	4.5.2.1.2.1-P
		(Direct coupled)	4.5.2.2.2.1-P
5.1.2.1.3	Rise and fall time		4.5.2.1.2.1-P
5.1.2.1.3.1	Trapezoidal		4.5.2.1.2.1-P
5.1.2.1.3.2	Sinusoidal		4.5.2.1.2.1-P
5.1.2.2	Common mode rejection		
		(Transformer coupled)	4.5.2.1.2.2-P
		(Direct coupled)	4.5.2.2.2.2-P

Test Plan		MIL-STD-1553B
5.1.2.3	Input impedance	
	(Transformer coupled)	4.5.2.1.2.3-P
	(Direct coupled)	4.5.2.2.2.3.-P
5.2	Protocol tests	4.4.1.3-P
5.2.1	Required remote terminal operation	4.4.3-P
5.2.1.1	Response to command words	
5.2.1.1.1	RT response to command words	4.3.3.6-P
5.2.1.1.2	RT-RT response to command words	4.3.3.6-P
5.2.1.2	Intermessage gap	
5.2.1.2.1	Minimum time	4.3.3.7-P
5.2.1.2.2	Transmission rate	4.3.3.7-P
		4.3.3.8-R
5.2.1.3	Error injection	4.3.3.5.1.6-R
		4.3.3.5.3.3-P
		4.4.1.1-R
		4.4.3.1-R
		4.4.3.3-R
		4.4.3.5-R
		4.4.3.6-R
5.2.1.3.1	Parity	4.3.3.5.1.6-R
		4.3.3.5.3.3-P
		4.4.1.1-R
		4.4.3.1-R
		4.4.3.3-P
5.2.1.3.1.1	Transmit command word	4.3.3.5.1.6-R
		4.3.3.5.3.3-P
		4.4.1.1-R
		4.4.3.3-P
		4.4.3.5-R
		4.4.3.6-R
5.2.1.3.1.2	Receive command word	4.3.3.5.1.6-R
		4.3.3.5.3.3-P
		4.4.1.1-R
		4.4.3.3-P
		4.4.3.5-R
		4.4.3.6-R
5.2.1.3.1.3	Receive data word	4.3.3.5.1.6-R
		4.3.3.5.3.3-P
		4.4.1.1-R
		4.4.3.1-R
		4.4.3.3-P
		4.4.3.5-R
		4.4.3.6-R
5.2.1.3.2	Word length	4.3.3.4-R
		4.3.3.5.3.3-P
		4.4.1.1-R
		4.4.3.1-R
		4.4.3.3-P
5.2.1.3.2.1	Transmit command word	4.3.3.4-P
		4.3.3.5.3.3-P
		4.4.1.1-R
		4.4.3.3-P
		4.4.3.5-R

Test Plan		MIL-STD-1553B
5.2.1.3.2.2	Receive command word	4.3.3.4-P 4.3.3.5.3.3-P 4.4.1.1-R 4.4.3.3-P 4.4.3.6-R
5.2.1.3.2.3	Receive data words	4.3.3.4-P 4.3.3.5.3.3-P 4.4.1.1-R 4.4.3.6-R
5.2.1.3.3	Bi-phase encoding	4.3.3.2-P 4.3.3.5.3.3-R 4.4.1.1-R 4.4.3.5-R 4.4.3.6-R
5.2.1.3.3.1	Transmit command word	4.3.3.2-P 4.3.3.5.3.3-R 4.4.1.1-R 4.4.3.3-R
5.2.1.3.3.2	Receive command word	4.3.3.2-P 4.3.3.5.3.3-R 4.4.1.1-R 4.4.3.3-R
5.2.1.3.3.3	Receive data word	4.3.3.2-P 4.3.3.5.3.3-R 4.4.1.1-R 4.4.3.5-R 4.4.3.6-R
5.2.1.3.4	Sync encoding	4.3.3.5.1.1-P 4.3.3.5.2.1-P 4.3.3.5.3.1-P 4.4.1.1-R 4.4.3.3-R 4.4.3.5-R 4.4.3.6-R
5.2.1.3.4.1	Transmit command word	4.3.3.5.1.1-P 4.4.1.1-R 4.4.3.3-R
5.2.1.3.4.2	Receive command word	4.3.3.5.1.1-P 4.4.1.1-R 4.4.3.3-R
5.2.1.3.4.3	Data word	4.3.3.5.2.1-P 4.4.1.1-R 4.4.3.6-R
5.2.1.3.5	Message length	4.3.3.5.1.5-P
5.2.1.3.5.1	Transmit command	4.3.3.5.1.5-P 4.3.3.6-R 4.3.3.6.2-R
5.2.1.3.5.2	Receive command	4.3.3.5.1.5-P 4.3.3.6-R 4.3.3.6.1-R
5.2.1.3.5.3	Mode command word count error	4.3.3.6-R
5.2.1.3.5.4	RT to RT word count error	4.3.3.5.1.5-P 4.3.3.6-R

Test plan		MIL-STD-1553B
5.2.1.3.6	Contiguous data	4.3.3.6.1-P 4.4.1.2-R 4.4.3.5-R
5.2.1.3.7	Terminal fail-safe	4.4.1.3-P
5.2.1.4	Superseding commands	4.4.3.2-P
5.2.1.5	Required mode commands	30.4.2.1-P 4.3.3.5.1.7-P
5.2.1.5.1	Transmit status	4.3.3.5.1.7.3-P
5.2.1.5.2	Transmitter shutdown & override	4.3.3.5.1.7.5-P 4.3.3.5.1.7.6-P
5.2.1.5.3	Reset remote terminal	4.3.3.5.1.7.9-P 30.4.3-P
5.2.1.6	Data wrap-around	30.7-P
5.2.1.7	RT to RT timeout	30.9-P 4.3.3.9-P
5.2.1.8	Bus switching	4.6.3-P 30.2-R
5.2.1.9	Unique address	30.3-P 4.3.3.5.1.2-R
5.2.2	Optional operation	
5.2.2.1	Optional mode commands	4.3.3.5.1.7-P
5.2.2.1.1	Dynamic bus control	4.3.3.5.1.7.1-P 4.3.3.5.3.10-R
5.2.2.1.2	Synchronize	
5.2.2.1.2.1	Synchronize without data word	4.3.3.5.1.7.2-P
5.2.2.1.2.2	Synchronize with data word	4.3.3.5.1.7.12-P
5.2.2.1.3	Initiate self-test	4.3.3.5.1.7.4-P 30.4.4-P
5.2.2.1.4	Transmit bit word	4.3.3.5.1.7.14-P
5.2.2.1.5	Selective transmitter shutdown & override	4.3.3.5.1.7.15-P 4.3.3.5.1.7.16-P
5.2.2.1.6	Terminal flag bit inhibit and override	4.3.3.5.1.7.7-P 4.3.3.5.1.7.8-P
5.2.2.1.7	Transmit vector word	4.3.3.5.1.7.11-P
5.2.2.1.8	Transmit last command	4.3.3.5.1.7.13-P
5.2.2.2	Status word bits	4.3.3.5.3-P 30.5.2-P
5.2.2.2.1	Service request	4.3.3.5.3.5-P
5.2.2.2.2	Broadcast command received	4.3.3.5.3.7-P
5.2.2.2.3	Busy	4.3.3.5.3.8-P 30.5.3-P
5.2.2.2.4	Subsystem flag	4.3.3.5.3.9-P
5.2.2.2.5	Terminal flag	4.3.3.5.3.11-P
5.2.2.3	Illegal command	4.4.3.4-P
5.2.2.4	Broadcast mode commands	4.3.3.6.7.3-P 4.3.3.6.7.4-P
5.2.2.4.1	Broadcast synchronize(without data word)	4.3.3.5.1.7.2-P 4.3.3.6.7.3-P
5.2.2.4.2	Broadcast synchronize (with data word)	4.3.3.5.1.7.12-P 4.3.3.6.7.4-P
5.2.2.4.3	Broadcast initiate self-test	4.3.3.5.1.7.4-P 4.3.3.6.7.3-P

Test Plan			MIL-STD-1553B
5.2.2.4.4	Broadcast transmitter shutdown and override		4.3.3.5.1.7.5-P 4.3.3.5.1.7.6-P 4.3.3.6.7.3-P
5.2.2.4.5	Broadcast selective transmitter shutdown and override		4.3.3.5.1.7.15-P 4.3.3.5.1.7.16-P
5.2.2.4.6	Broadcast terminal flag bit inhibit and override		4.3.3.5.1.7.7-P 4.3.3.5.1.7.8-P 4.3.3.6.7.3-P
5.2.2.4.7	Broadcast reset remote terminal		4.3.3.5.1.7.9-P 4.3.3.6.7.3-P
5.2.2.4.8	Broadcast dynamic bus control		4.3.3.5.1.7.1-P
5.2.2.5	Error injection - broadcast messages		4.3.3.5.3.3-P 4.3.3.5.3.7-R 4.4.1.1-R 4.4.3.1-R 4.4.3.3-R 4.4.3.5-R 4.4.3.6-R
5.2.2.5.1	Parity: BC-RT broadcast		4.3.3.5.1.6-P 4.3.3.6.7.1-R
5.2.2.5.2	Command word error		4.3.3.5.1.6-P 4.3.3.5.1-R
5.2.2.5.3	Data word error		4.3.3.5.1.6-P 4.3.3.5.2-R
5.2.2.5.4	Message length, BC to RT broadcast		4.3.3.6.7.1-P 4.4.3.6-P 4.3.3.5.3.7-R
5.3	Noise rejection	(Transformer coupled) (Direct coupled)	4.5.2.1.2.4-P 4.5.2.2.2.4-P

APPENDIX B
MIL-STD-1553B TO TEST PLAN CROSS REFERENCE

MIL-STD-1553B		Test Plan
4.	General requirements	
4.1	Test & operating requirements	none
4.2	Data bus operation	5.2
4.3	Characteristics	
4.3.1	Data form	none
4.3.2	Bit priority	none
4.3.3	Transmission method	
4.3.3.1	Modulation	none
4.3.3.2	Data code	5.2.1.3.3
4.3.3.3	Transmission bit rate	5.1.1.10
4.3.3.4	Word size	5.2.1.3.2
4.3.3.5	Word formats - command	5.2.1.1
	- data	none
	- status	5.2.2.2
4.3.3.5.1	Command word	5.2.1.1
4.3.3.5.1.1	Sync	5.2.1.3.4.1
4.3.3.5.1.2	Remote terminal addres (not 11111)	5.2.1.1
	(11111)	5.2.1.1
4.3.3.5.1.3	Transmit/receive	5.2
4.3.3.5.1.4	Subaddress/mode - subaddress	5.2.1.1
	- mode	5.2.2.1
4.3.3 .5.1.5	Data word count/mode code - word count	5.2.1.3.5
	- mode code	5.2.2.1
4.3.3.5.1.6	Parity	5.2.1.3.1
4.3.3.5.1.7	Optional mode control	5.2.2.1
4.3.3.5.1.7.1	Dynamic bus control	5.2.2.1.1
4.3.3.5.1.7.2	Synchronize (without data word)	5.2.2.1.2.1
4.3.3.5.1.7.3	Transmit status word	5.2.1.5.1
4.3.3.5.1.7.4	Initiate self test	5.2.2.1.3
4.3.3.5.1.7.5	Transmitter shutdown	5.2.1.5.2
4.3.3.5.1.7.6	Override transmitter shutdown	5.2.1.5.2
4.3.3.5.1.7.7	Inhibit T/F bit	5.2.2.1.6
4.3.3.5.1.7.8	Override inhibit T/F flag	5.2.2.1.6
4.3.3.5.1.7.9	Reset remote terminal	5.2.1.5.3
4.3.3.5.1.7.10	Reserved mode codes (01001-01111)	5.2.1.1
4.3.3.5.1.7.11	Transmit vector word	5.2.2.1.7
4.3.3.5.1.7.12	Synchronize (with data word)	5.2.2.1.2.2
4.3.3.5.1.7.13	Transmit last command word	5.2.2.1.8
4.3.3.5.1.7.14	Transmit built-in-test (BIT) word	5.2.2.1.4
4.3.3.5.1.7.15	Selected transmitter shutdown	5.2.21.5
4.3.3.5.1.7.16	Override selected transmitter shutdown	5.2.2.1.5
4.3.3.5.1.7.17	Resewed mode codes (10110 to 11111)	5.2.1.1
4.3.3.5.2	Data word	
4.3.3.5.2.1	sync	5.2.1.3.4.2
4.3.3.5.2.2	Data	none
4.3.3.5.2.3	Parity	4.1
4.3.3.5.3	Status word	5.2.2.2
4.3.3.5.3.1	Sync	4.2

MIL-STD-1553B		Test Plan
4.3.3.5.3.2	RT address	4.2
4.3.3.5.3.3	Message error bit	5.2.1.3
4.3.3.5.3.4	Instrumentation bit	4.2
4.3.3.5.3.5	Service request bit	5.2.2.2.1
4.3.3.5.3.6	Reserved status bits	4.2
4.3.3.5.3.7	Broadcast command received bit	5.2.2.2.2
4.3.3.5.3.8	Busy bit	5.2.2.2.3
4.3.3.5.3.9	Subsystem flag bit	5.2.2.2.4
4.3.3.5.3.10	Dynamic bus control acceptance bit	5.2.2.1.1
4.3.3.5.3.11	Terminal flag bit	5.2.2.2.5
4.3.3.5.3.12	Parity bit	4.2
4.3.3.5.4	Status word reset	5.2.2.2
4.3.3.6	Message formats	n/a
4.3.3.6.1	BC to RT transfers	5.2.1.1.1
4.3.3.6.2	RT to BC transfers	5.2.1.1.1
4.3.3.6.3	RT to RT transfers	5.2.1.1.2
4.3.3.6.4	Mode command w/o data word	5.2.2.1
4.3.3.6.5	Mode command with data word (transmit)	5.2.2.1
4.3.3.6.6	Mode command data word (receive)	5.2.2.1
4.3.3.6.7	Optional broadcast command	5.2.1.1
4.3.3.6.7.1	BC to RT transfer (broadcast)	5.2.1.1
4.3.3.6.7.2	RT to RT transfer (broadcast)	5.2.1.1
4.3.3.6.7.3	Mode commands w/o data word (broadcast)	5.2.2.4
4.3.3.6.7.4	Mode commands with data word (broadcast)	5.2.2.4
4.3.3.7	Intermessage gap	5.2.1.2
4.3.3.8	Response time	4.2 5.1.1.9
4.3.3.9	Minimum no-response time-out	5.2.1.7
4.4	Terminal operation	
4.4.1	Common operation	
4.4.1.1	Word validation	5.2.1.3
4.4.1.2	Transmission continuity	5.2.1.3.6
4.4.1.3	Terminal fail-safe	5.2.1.3.7
4.4.2	Bus controller operation	n/a
4.4.3	Remote terminal	5.2
4.4.3.1	Operation	5.2.1.1
4.4.3.2	Superseding valid commands	5.2.1.4
4.4.3.3	Invalid commands	5.2.1.3
4.4.3.4	Illegal commands	5.2.2.3
4.4.3.5	Valid data reception	5.2.1.3
4.4.3.6	Invalid data reception	5.2.1.3
4.4.4	Bus monitor operation	n/a
4.5	Hardware characteristics	
4.5.1	Data bus characteristics	
4.5.1.1	Cable	n/a
4.5.1.2	Characteristics impedance	n/a
4.5.1.3	Cable attenuation	n/a
4.5.1.4	Cable termination	n/a
4.5.1.5	Cable stub requirements	n/a
4.5.1.5.1	Transformer coupled stubs	n/a
4.5.1.5.1.1	Coupling transformer	n/a
4.5.1.5.1.1.1	Transformer input impedance	n/a

MIL-STD-1553B		Test Plan
4.5.1.5.1.1.2	Transformer waveform integrity	n/a
4.5.1.5.1.1.3	Transformer common mode rejection	n/a
4.5.1.5.1.2	Fault isolation	n/a
4.5.1.5.1.3	Cable coupling	n/a
4.5.1.5.1.4	Stub voltage requirements	n/a
4.5.1.5.2	Direct coupled stubs	n/a
4.5.1.5.2.1	Fault isolation	n/a
4.5.1.5.2.2	Cable coupling	n/a
4.5.1.5.2.3	Stub voltage requirements	n/a
4.5.1.5.3	Wiring & cabling for EMC	n/a
4.5.2	Terminal characteristics	5.1
4.5.2.1	Terminals with transformer coupled stubs	5.1
4.5.2.1.1	Terminal output characteristics	5.1.1
4.5.2.1.1.1	Output levels	5.1.1.1
4.5.2.1.1.2	Output waveform	5.1.1.2 5.1.1.3 5.1.1.4
4.5.2.1.1.3	Output noise	5.1.1.6 5.1.1.8
4.5.2.1.1.4	Output symmetry	5.1.1.5
4.5.2.1.2	Terminal input characteristics	5.1.2
4.5.2.1.2.1	Input waveform compatibility	5.1.2.1
4.5.2.1.2.2	Common mode rejection	5.1.2.2
4.5.2.1.2.3	Input impedance	5.1.2.3
4.5.2.1.2.4	Noise rejection	5.3
4.5.2.2	Terminals with direct coupled stubs	5.1
4.5.2.2.1	Terminal output characteristics	5.1.1
4.5.2.2.1.1	Output levels	5.1.1.1
4.5.2.2.1.2	Output waveform	5.1.1.2 5.1.1.3 5.1.1.4
4.5.2.2.1.3	Output noise	5.1.1.6 5.1.1.8
4.5.2.2.1.4	Output symmetry	5.1.1.5
4.5.2.2.2	Terminal input characteristics	5.1.2
4.5.2.2.2.1	Input waveform compatibility	5.1.2.1
4.5.2.2.2.2	Common mode rejection	5.1.2.2
4.5.2.2.2.3	Input impedance	5.1.2.3
4.5.2.2.2.4	Noise rejection	5.3
4.6	Redundant data bus requirements	5.2.1.8
4.6.1	Electrical isolation	5.1.1.7
4.6.2	Single event failures	n/a
4.6.3	Dual standby redundant data bus	5.2.1.8
4.6.3.1	Data bus activity	5.2.1.8
4.6.3.2	Superseding valid commands	5.2.1.8
30.	GENERAL REQUIREMENTS	n/a
30.1	Option selection	n/a
30.2	Application	n/a
30.3	Unique address	5.2.1.9
30.4	Mode codes	n/a
30.4.1	Subaddress/mode	5.2.1.5

MIL-STD-1553B		Test Plan
30.4.2.1	Remote terminal required mode codes	5.2.1.5
30.4.2.2	Bus controller required mode codes	n/a
30.4.3	Reset remote terminal	5.2.1.5.3
30.4.4	Initiate RT self-test	5.2.2.1.3
30.5	Status word bits	n/a
30.5.1	Information content	5.1.1.8.2
30.5.2	Status bit requirements	5.2.2.2
30.5.3	Buy bit	5.2.2.2.3
30.6	Broadcast	5.2.1.1
30.7	Data wrap-around	5.2.1.6
30.8	Message formats	n/a
30.9	RT to RT validation	5.2.1.7
30.10	Electrical characteristics	n/a
30.10.1	Cable shielding	n/a
30.10.2	Shielding	n/a
30.10.3	Connector polarity	n/a
30.10.4	Characteristic impedance	n/a
30.10.5	Stub coupling	n/a
30.10.6	Power on/off noise	5.1.1.8

APPENDIX C

TEST PLAN CHANGES FOR MIL-STD-1553B ONLY RTs

For remote terminals designed to only comply with MIL-STD-1553B, the following changes shall be made for the pass criteria in this document.

1. The following paragraphs are optional and are subject to the same require ments as 5.2.2.

5.2.1.5	Required mode commands
5.2.1.5.1	Transmit status
5.2.1.5.2	Transmitter shutdown and override
5.2.1.5.3	Reset remote terminal
5.2.1.6	Data wrap-around
5.2.1.7	RT to RT timeout
5.2.1.8	Bus switching
5.2.1.9	Unique address

2. For the following paragraphs, the pass criteria for step 2 shall be changed to delete the words “(with BUSY bit reset).”

5.2.2.1.3	Initiate self-test
5.2.1.5.3	Reset remote terminal
5.2.2.4.3	Broadcast initiate self-test
5.2.2.4.7	Broadcast reset remote terminal

3. For 5.1.1.8.1 Power on/off noise, the pass criteria shall not be defined in this document.

4. For the following paragraphs, the requirement to implement both mode code indicators of all zeros and all ones is optional and subject to the same requirements as 5.2.2. The RT must meet the pass criteria for either all zeros or all ones, but is not required to meet both.

5.2.1.5	Required mode commands
5.2.2.1	Optional mode commands
5.2.2.4	Broadcast mode commands

5. The following note shall be added to the end of 5.2.1.3.

Note: If transmit status mode command is not implemented, then transmit last command mode command shall be used. If neither mode command is implemented, then step 3 shall be deleted.

APPENDIX D

TEST PLAN CHANGES FOR MIL-STD-1553B, NOTICE 1 RTs

For remote terminals designed to comply with MIL-STD-1553B, Notice 1, the following changes shall be made for the pass criteria in this document.

1. The following paragraphs are optional, and are subject to the same requirements as 5.2.2.

5.2.1.5	Required mode commands
5.2.1.5.1	Transmit status
5.2.1.5.2	Transmitter shutdown and override
5.2.1.5.3	Reset remote terminal
5.2.1.6	Data wrap-around
5.2.1.7	RT to RT timeout
5.2.1.9	Unique address

2. For the following paragraphs, the pass criteria for step 2 shall be changed to delete the words "(with BUSY bit reset)."

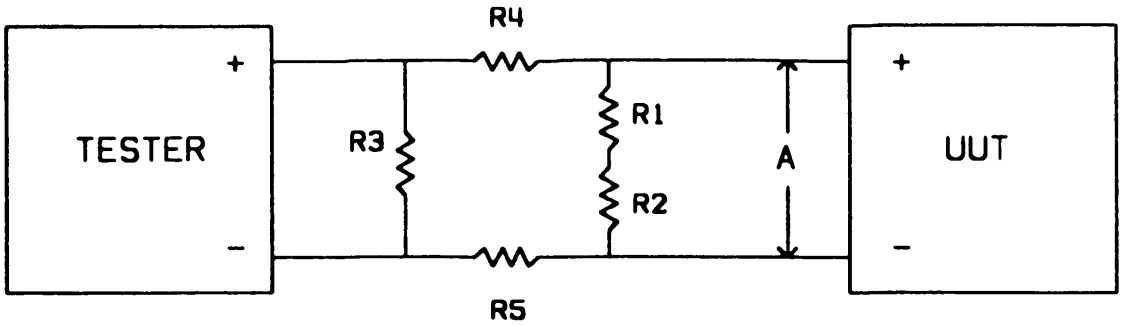
5.2.2.1.3	Initiate self-test
5.2.1.5.3	Reset remote terminal
5.2.2.4.3	Broadcast initiate self-test
5.2.2.4.7	Broadcast reset remote terminal

3. For 5.1.1.8, the pass criteria shall not be defined in this document.

4. For the following paragraphs the requirement to implement mode code indicator of all ones is optional and subject to the same requirements as 5.2.2.

5.2.1.5	Required mode commands
5.2.2.1	Optional mode commands
5.2.2.4	Broadcast mode commands

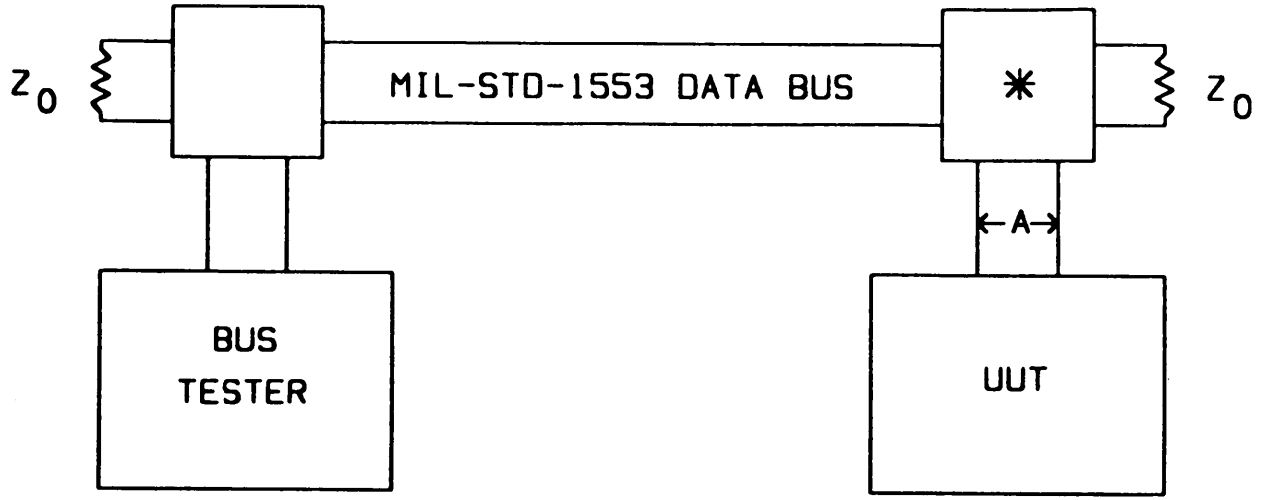
5. The following note shall be added to the end of 5.2.1.3.



	DIRECT COUPLED	TRANSFORMER COUPLED
	35 ohms ±2%	70 ohms ±2%
R1, R2	20	46.5
R3, R4, R5	100	93.1

GENERAL RESISTOR PAD CONFIGURATION

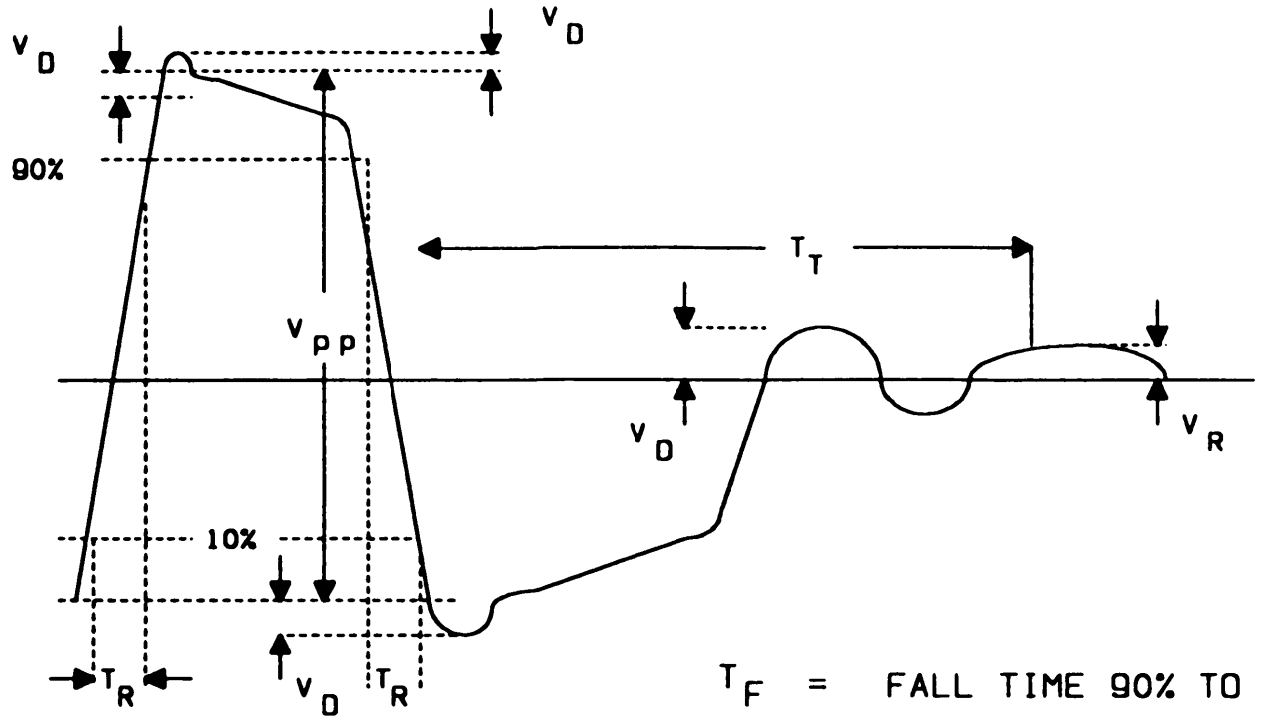
FIGURE 1A.



* NOTE: REFERENCE FIGURES 9A AND 10A OF MIL-STD-1553 FOR DATA BUS INTERFACE COUPLING. REFERENCE FIGURE 10B OF THIS TEST PLAN FOR SUGGESTED CABLE TYPE, BUS AND SUB LENGTHS, ETC.

GENERAL BUS CONFIGURATION

Figure 1B



T_F = FALL TIME 90% TO 10%

T_R = RISE TIME 10% TO 90%

T_T = WAVEFORM TAILOFF TIME = 2.5 SEC

V_R = RESIDUAL VOLTAGE

V_D = DISTORTION VOLTAGE

V_{pp} = PEAK-TO-PEAK VOLTAGE

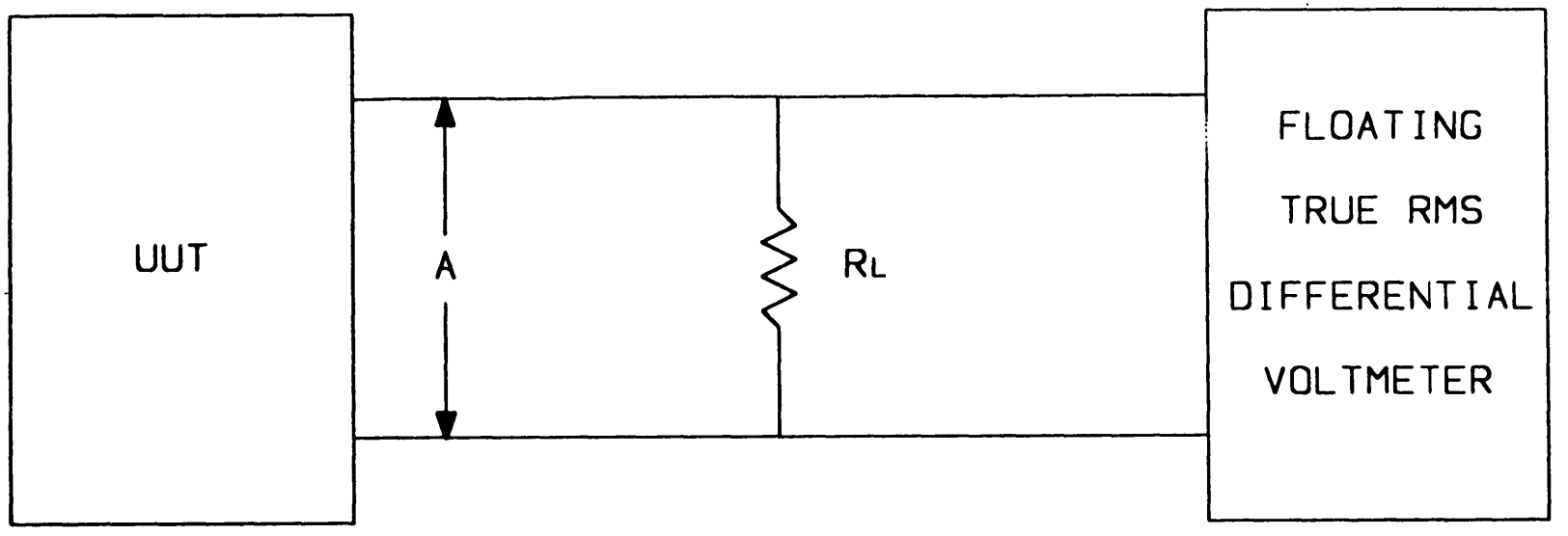
WAVEFORM MEASUREMENTS

Figure 2.

F_2

ZERO CROSSING INTERVAL MEASUREMENTS

Figure 8.

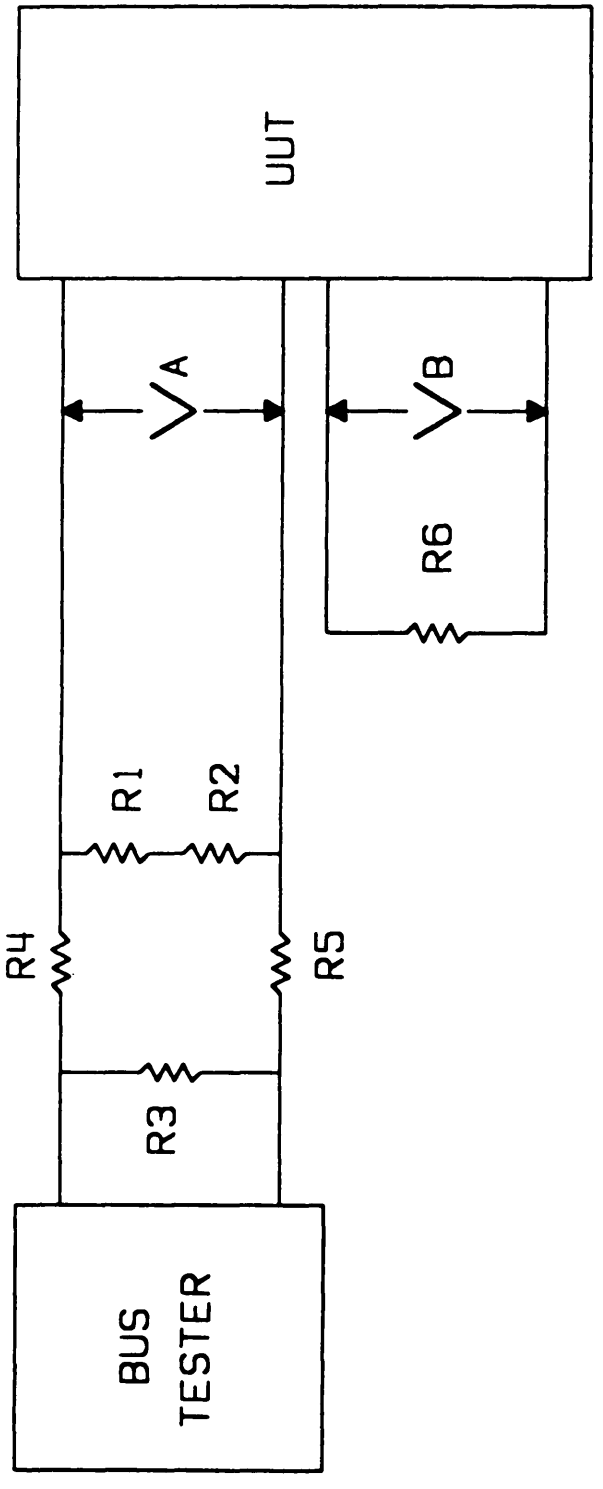


TRANSFORMER COUPLED R_L = 70.0 ohms $\pm$2%

DIRECT COUPLED R_L = 35.0 ohms $\pm$2%

OUTPUT NOISE CONFIGURATION

Figure 4.

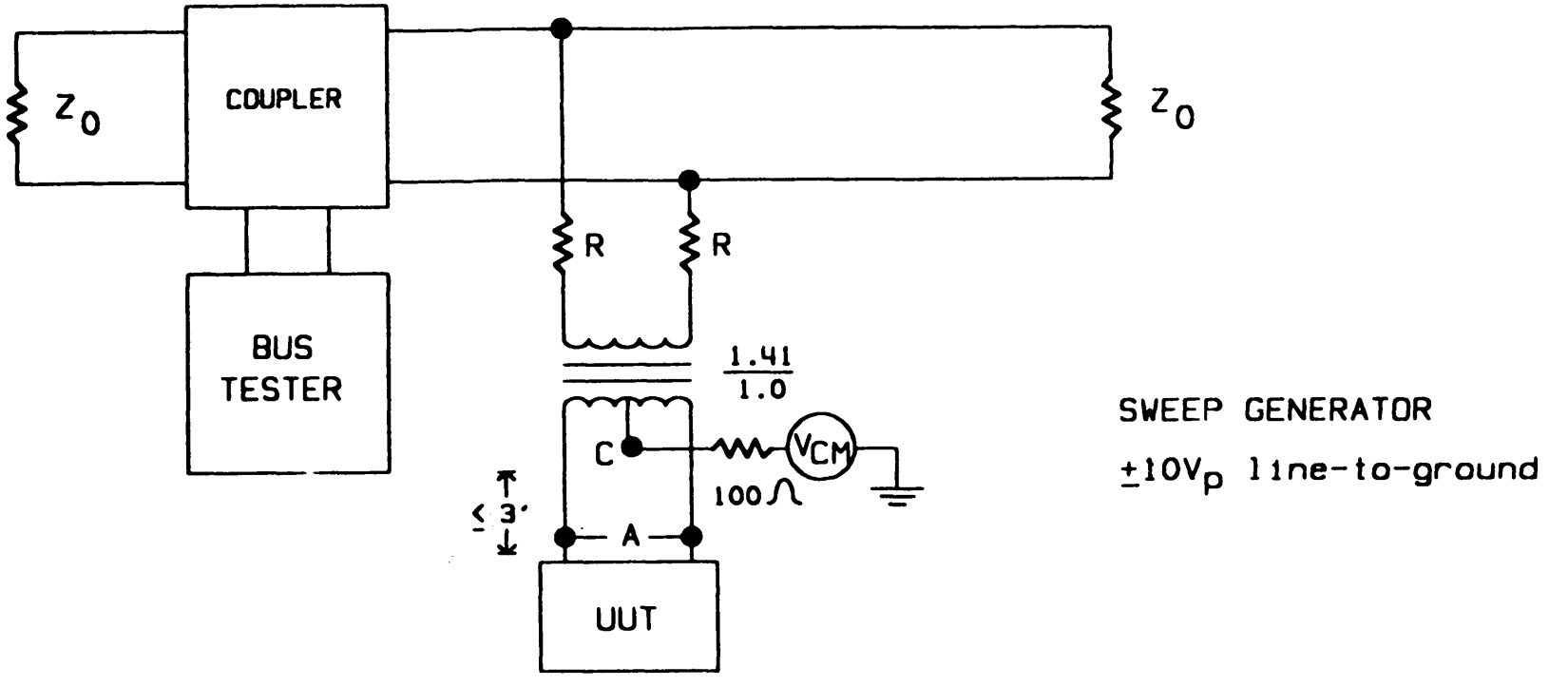


	DIRECT COUPLED		TRANSFORMER COUPLED	
	35 ohms	±2%	70 ohms	±2%
R1, R2	20		46.5	
R3, R4, R5	100		93.1	
R6	35		70	

$$dB = 20 \log \frac{V_A}{V_B}$$

OUTPUT ISOLATION

Figure 5.



R = 0.75 Z_0 ±2%

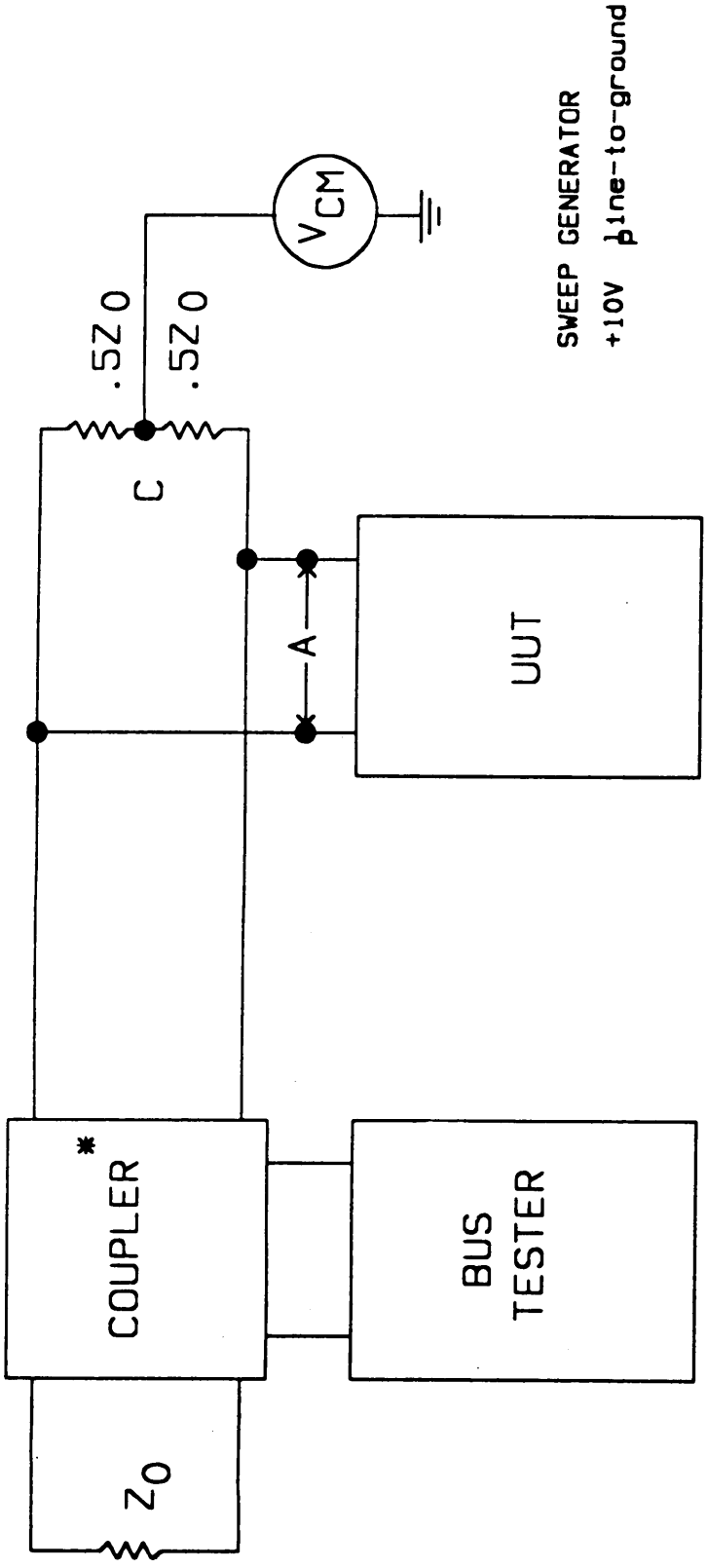
Z - Selected Cable Nominal Characteristic Impedance

TRANSFORMER COUPLED

COMMON MODE CONFIGURATION

Figure 6A.

F-6A

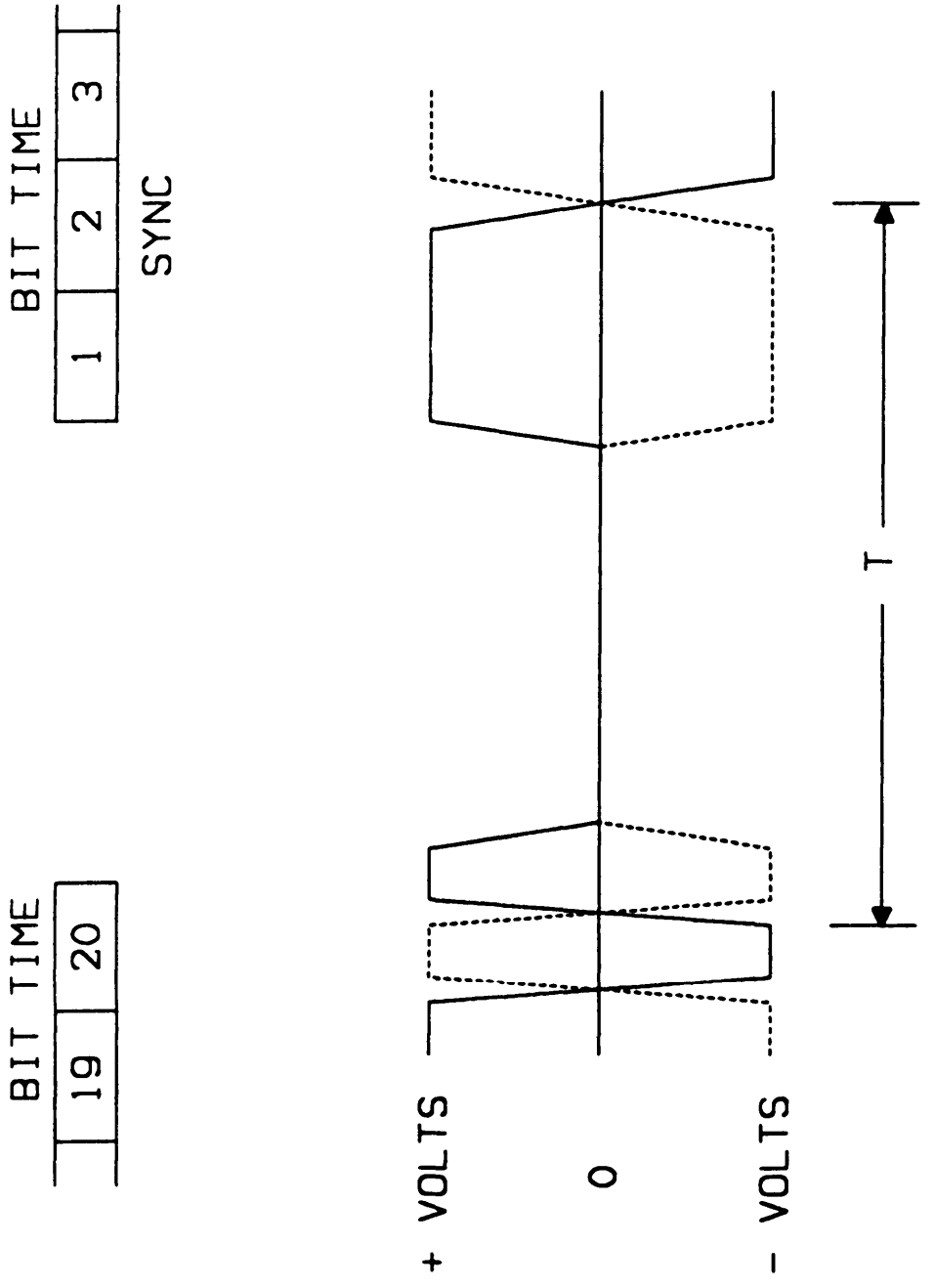


* – Transformer Coupled Stub Must Be Used

Z_0 – Selected Cable Nominal Characteristic Impedance

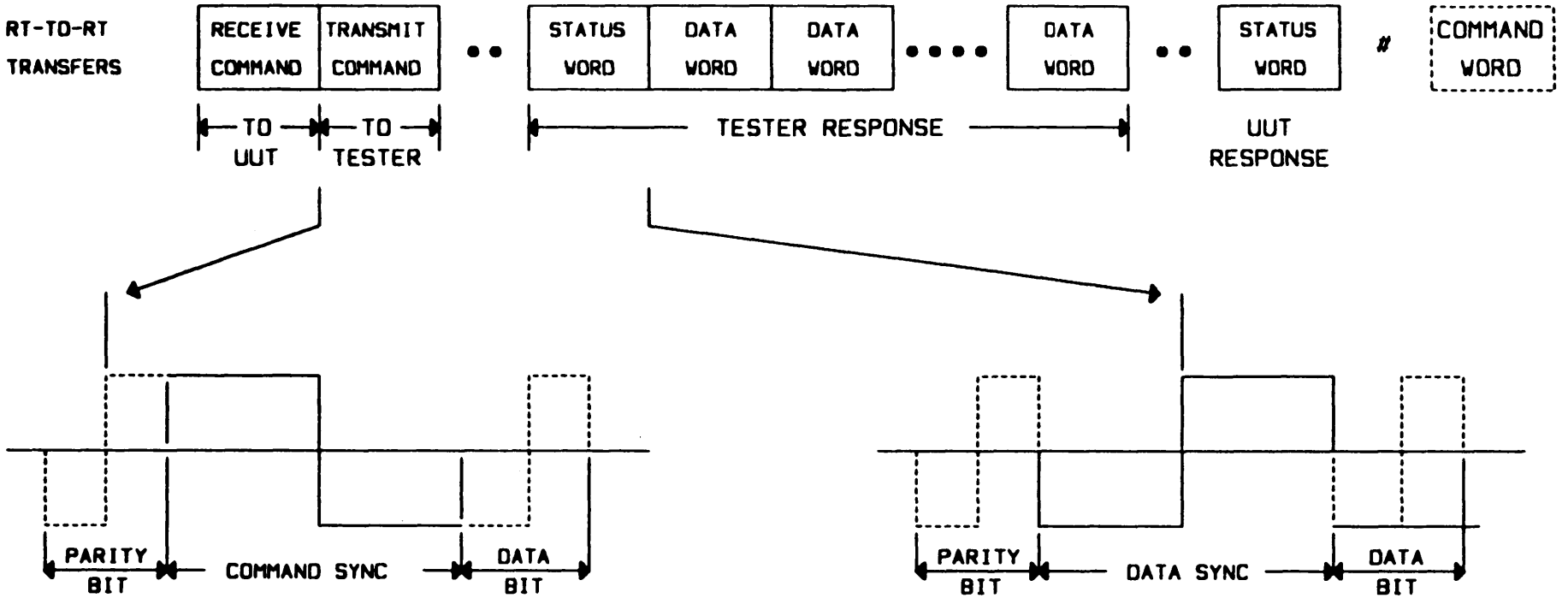
DIRECT COUPLED
COMMON MODE CONFIGURATION

Figure 6B.



GAP TIME MEASUREMENT

Figure 7.

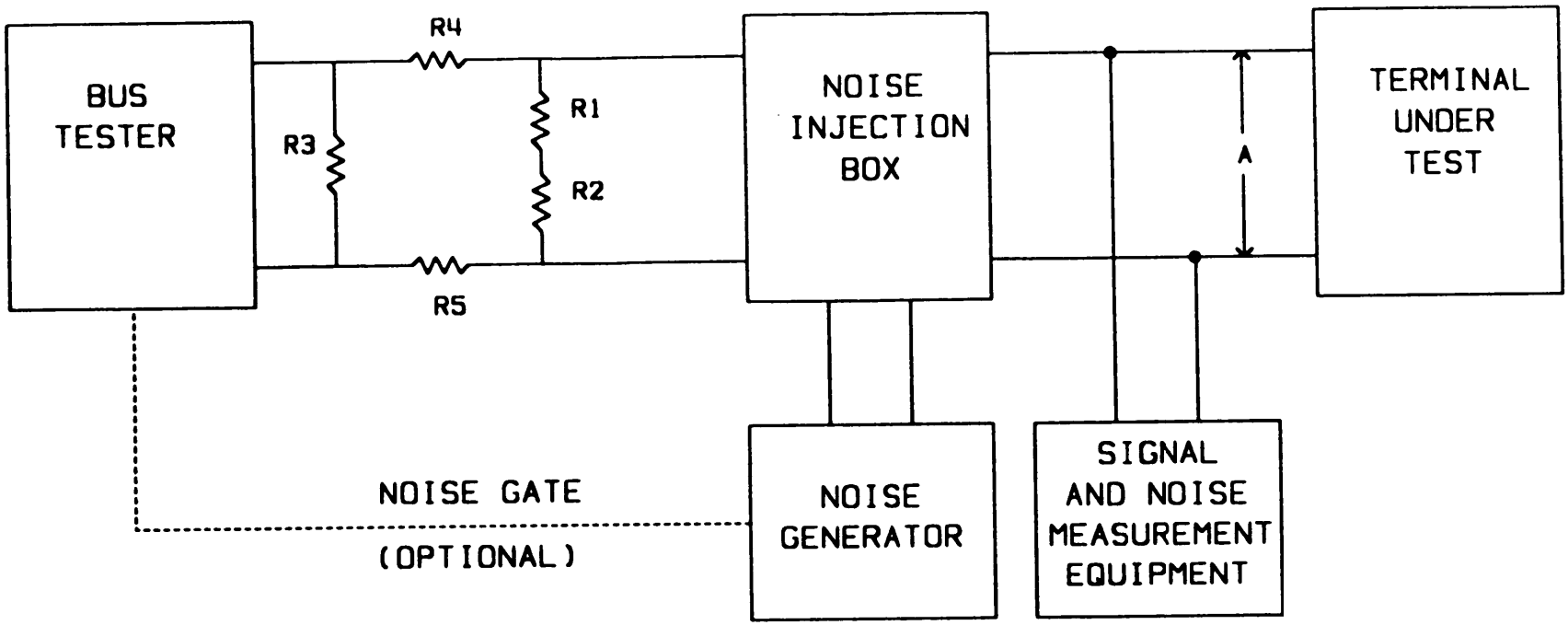


T = 54 to 60 usec measured as shown

Delay tester respone until UUT response goes away

RT - RT TIMEOUT MEASUREMENT

Figure 8.

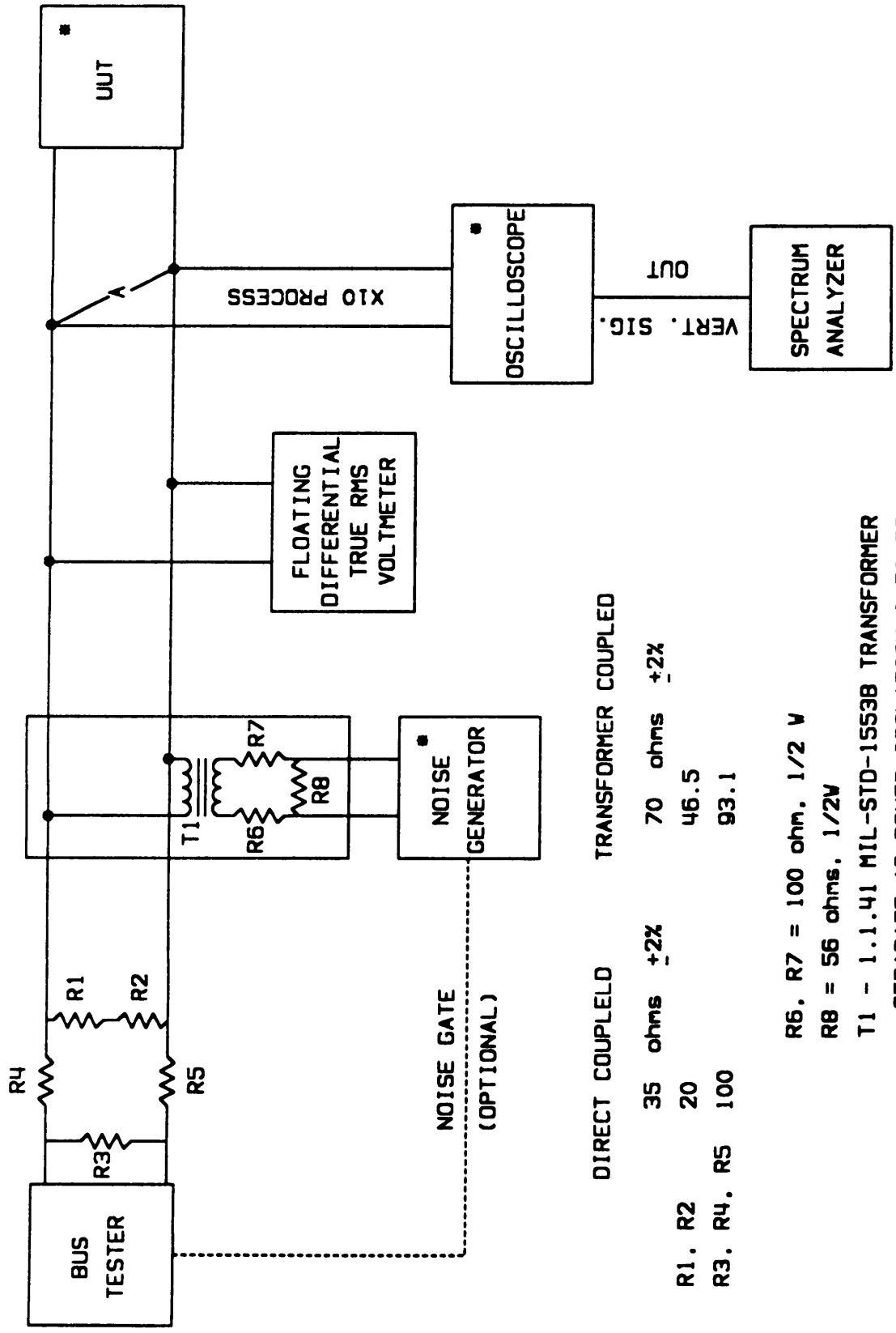


	DIRECT COUPLED	TRANSFORMER COUPLED
	35 ohms ±2%	70 ohms ±2%
R1, R2	20	46.5
R3, R4, R5	100	93.1

CONFIGURATION FOR NOISE REJECTION TEST

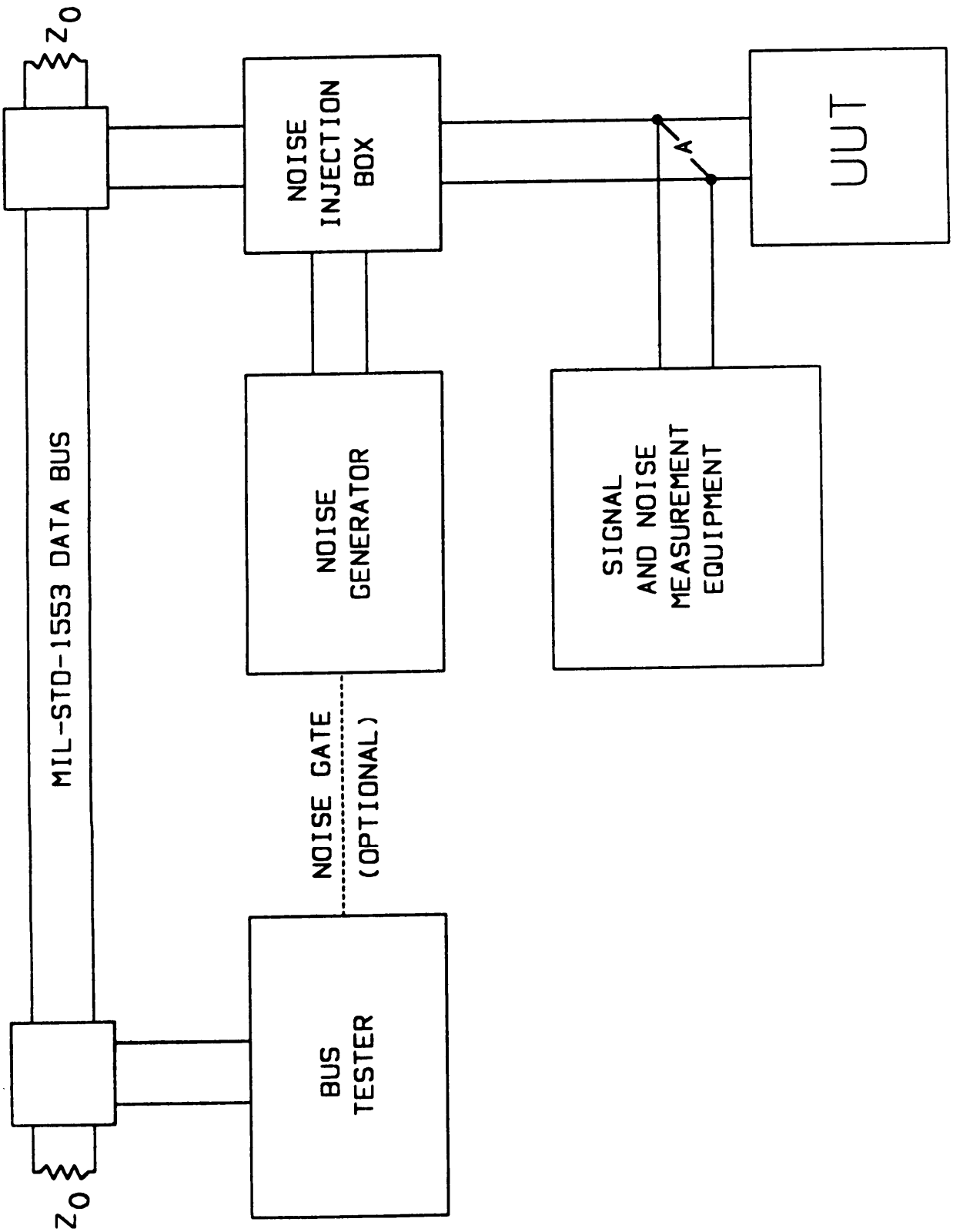
Figure 9A.

F-9A



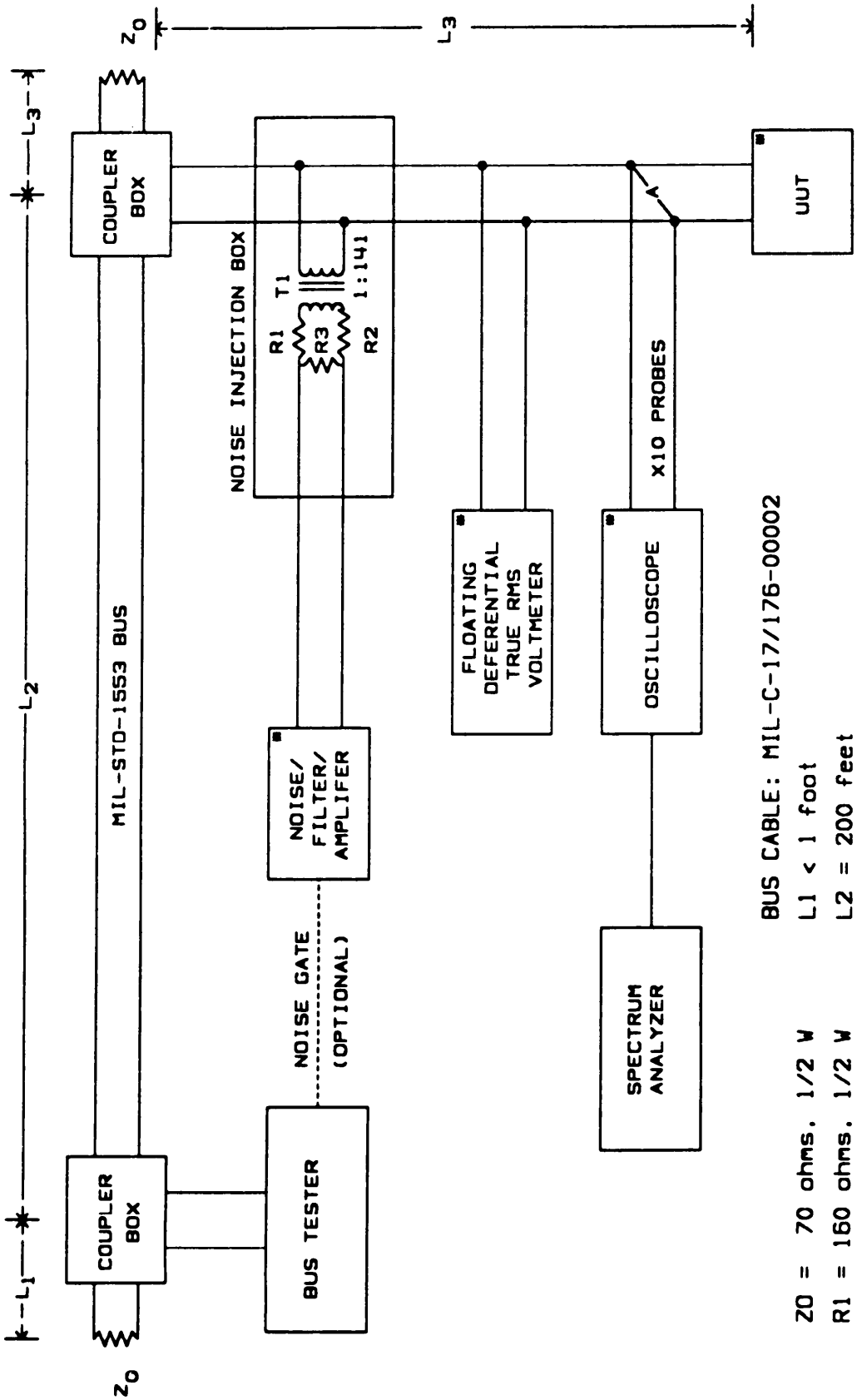
SUGGESTED CONFIGURATION FOR NOISE REJECTION TEST

Figure 9B.



CONFIGURATION FOR NOISE REJECTION TEST

Figure 10A.



SUGGESTED CONFIGURATION FOR NOISE REJECTION TEST

Figure 10B.

SECTION 110

OTHER TEST PLANS

110. OTHER TEST PLANS

110.1 INTRODUCTION

The test plans referenced here represent extensive work by many companies contributing in an SAE committee forum over several years;thus, represent the best quality test plans obtainable from any industry group on MIL-STD-1553B. The DoD does not control any portion of these referenced test plans. The referenced plans may be used for validation, development, acceptance, production, or system integration test requirements.

110.2 REFERENCES

The Society of Automotive Engineers (SAE) committee AS-1 has assembled the following test plans:

1. The RT Production Test Plan (AS4112)

2. The BC Validation Test Plan (AS4113)

3. The BC Production Test Plan (AS4114)

4. The System Test Plan (AS4115).

These test plans are available from the following address:

SAE
400 Commonwealth Drive
Warrendale, PA 15096-00001 U.S.A.
Telephone (412) 776-4641

Additional plans containing test requirements for bus monitor functions and for some bus components (couplers, terminators, and wire) may also be available from the SAE.

SECTION 120

MULTIPLEX TERMS

AND DEFINITIONS

120. MULTIPLEX TERMS AND DEFINITIONS

1553. Military standard that establishes requirements for digital, command/response timedMision multiplexing techniques. In this handbook, 1553 is used as a generic name for MIL-STD-1553(USAF), MIL-STD-1553A, and MIL-STD-1553B. Where a specific revision is referenced, the revision suffix is added, e.g., 1553B.

Address Programming. The method by which an RT is made unique from all others.

Analog Front End of a Terminal. The analog front-end portion of a 1553B terminal (see 50.3) consists of one or more channels, each of which contains an interface to translate the 1553B bus signal into a digital signal with voltage levels appropriate for the remainder of the terminal. The fact that most terminals being designed today use purchased hybrid or VLSI IC parts has gone far toward simplifying terminal design.

Aperiodic. Events occurring at indefinite or unscheduled time periods. This term is used to describe the timing of messages that are not assigned a regular transmission update rate. “Asynchronous” is another word used to express the same condition.

Applications Software. Those programs whose purpose is dedicated to specific functions (e.g., navigation, fire control, I/O conversion). This distinguishes applications software from executive software.

Architecture. The functional structure of a multiplex system as defined by the physical interconnection (topology) and the multiplex system control. See configuration.

Asynchronous Operation. For purpose of the standard, asynchronous operation is the use of an independent clock source in each terminal for message transmission. Decoding is achieved in receiving terminals using clock information derived from the message.

Avionics. All electronic and electromechanical systems and subsystems (hardware and software) installed in an aircraft or attached to it.

Avionics Hot Bench. Hot bench is a commonly used term to describe a system development laboratory (SDL) or system integration laboratory (SIL).

Bit. Contraction of binary digit—may be either zero or one. In information theory, a binary digit is equal to one binary decision or the designation of one of two possible values or states of anything used to store or convey information.

Bit Rate. The number of bits transmitted per unit time, usually, per second.

BLACK. The designation applied to all wirelines, components, equipment, and systems which handle only encrypted or unclassified signals, and areas in which no unencrypted or classified signals occur.

Broadcast. Operation of a data bus system such that information transmitted by the bus controller using a unique broadcast address is addressed to all of the terminals connected to the data bus.

Broadcast Command Received Bit. This bit is set by an RT that implements Broadcast Commands any time that a valid Broadcast Command has been received. Since there is no response to a Broadcast Command, the setting of this bit allows the Bus Controller to subsequently check that the command was received properly by issuing a ‘Transmit Status” or “Transmit Last Command” Mode Command.

Built-in Test (BIT). The capability of an LRU to perform some form of self-test.

Bus. In this handbook (unless noted in the text) bus refers to 1553 data bus, which is the part of the network which is terminated in its characteristic impedance, and to which stubs are attached. See data bus.

Bus controller. The terminal assigned the task of initiating information transfers on the data bus. There is one (and only one) BC on a 1553B bus (at any given time), and this terminal totally controls the flow of information on the bus. No other terminal may transmit anything on the bus except as instructed by the BC.

Bus coupler. The circuit which is used to couple signals between the main bus cable and transformer coupled stub cables. A single stub bus coupler consists of a transformer, two isolation resistors, and a shielded enclosure. Multiple stub bus couplers are also commercially available.

Bus Interface Unit (BIU) Function. This term is generally interchangeably with "terminal," as defined in 1553B: "The electronic module necessary to interface the data bus with the subsystem and the subsystem with the data bus. Terminals may exist as separate line replaceable units (LRUs) or be contained within the elements of the subsystem."

Bus Interface Unit (BIU) Hardware. This term describes a particular set of hardware that performs the interface between the data bus and the internal portion of an embedded or standalone remote terminal. As a minimum, it refers to the digital decode and encode logic that expands to the complete analog-to-digital interface between the data bus and the internal remote terminal electronics or the subsystem for embedded terminals.

Bus Monitor. The terminal assigned the task of receiving bus traffic and extracting selected information to be used at a latertime. A Bus Monitor does not transmit status words or anything else on the bus. It may have no terminal address, and in fact, can receive information addressed to any (or all) terminals on the bus. As defined in section 4.4.4 of 1553B, a Bus Monitor may have an assigned terminal address, in which case it will act just like an RT for commands to that address. The two most common applications of Bus Monitors are:

1. Instrumentation, for recording bus traffic from many or all terminals for off-line analysis.

2. Backup BC, to provide a terminal with enough information to become the BC on the bus if commanded to do so, either with a "Dynamic Bus Control" Mode Command or by some other method.

Busy Bit. An RT that is functional but that cannot transfer data to or from the subsystem on command from the Bus Controller is busy. An RT that is busy should set the "Busy" bit in its Status Word responses on the bus.

Characteristic Impedance (Z_o). The value of impedance which, if it terminates a transmission line, results in no reflection along the line. Z_o is usually specified at a certain frequency (1.0 MHz in 1553B, paragraph 4.5.1.2). $Z_0 \cong \sqrt{L/C}$ where L = inductance and C = capacitance per unit length of cable.

Clock Rate. The signal from the 1553B bus is asynchronous with any clock in the terminal, since a Manchester code is by its nature self-clocking. That is, all Manchester-encoded bits have a zero-crossing in the middle, and it is to this zero-crossing time that the data is referenced.

Command/Response. Operation of a data bus system such that remote terminals receive and transmit data only when commanded to do so by the bus controller.

Communications Protocol. See protocol.

Compool (global/local) (communication pool). This is a JOVIAL language term used to declare or define data by name that will subsequently be set or used by program procedures. The JOVIAL compiler establishes locations in memory for compool data. As such, it is the means of data communications, and the scope of the declaration can be limited, hence the restriction "local."

Configuration. The specific functional structure of a given integrated system consisting of physical interconnection (topology) and system control. See architecture.

Controller. See Bus Controller.

Data. This term is used in this handbook to denote the content (16 bits) of information transferred on the 1553 data bus in one data word.

Data Bus. Whenever a data bus or bus is referenced in this handbook, it implies all the hardware, including twisted-shielded pair cables, isolation resistors, transformers, etc., required to provide a single data path between the bus controller and all the associated remote terminals.

Data Bus Connectors. The two physically separate connectors provided on the RT interface to the data bus.

Data Bus Interface. The part of the digital interface which is concerned with transferring data. See Digital Interface.

Data Bus Loading. Data bus loading is the percent utilization of the total information transfer capacity of a multiplexed data bus.

Data Latency. Data latency is the age of the data, or how long it has been since the data was measured or calculated to the point where it is used.

Data Wrap-Around. Many RTs include a "data wrap-around" function, in which data words sent to the RT with a receive command are send back to the bus controller with a subsequent transmit command.

Digital Interface. Embedded, high speed interface to the subsystem used to transfer control, status information and data to and from the subsystem.

Digital Section. The remainder of the terminal other than the analog front end.

Direct Coupled. A method of connecting terminals to the 1553 data bus using only a wire splice.

Dispersion. Dispersion is transmission line effects on lossy transmission lines on propagating waveforms. It is a result of frequency-dependent velocity and frequencydependent attenuation which distorts the propagating wave.

DMA Interface. DMA hardware and DMA-CPU protocol establish the means by which data may be transferred to and from memory without direct CPU intervention.

Droop. The transient exponential decay of voltage across an inductor (typically a transformer winding) due to voltage drop across the output impedance of the source driving the inductor as the current in the winding increases (proportionally to the integral in time of the voltage).

Dual-redundant. Use of two twisted, shielded cable pairs and interfaces for the purpose of greater reliability.

Dynamic Bus Control. The operation of a data bus system in which designated terminals are offered control of the data bus, i.e., they become a BC when the terminal offering control relinquishes control.

Embedded Interface. 1553 interface circuitry housed within a subsystem.

Encryption Designs. Encryption techniques used by the data bus network and its associated terminals and processors to convert RED data into BLACK data and to isolate multiple classification levels and compartments of RED data. The specific encryption technique and system design must be approved by the government agency responsible for encryption certification.

Equipment Specifications. See specifications.

Error Management. General term used to descibe the detection of transient events that temporarily degrade bus timing or performance and the step-by-step sequence to branch to alternate functions, procedures, or equipment use.

Event. A single occurrence at a precise time.

Fail-Safe Timer. MIL-STD-1553B requires (4.4.1.3 of 1553B) that every RT or BC contain a hardware timer to prevent any transmission on the bus longer than 800 us. Since no valid transmission is longer than 660 us, only a failure in the terminal could result in a transmission of 800 us or longer. The fail-safe timer is required to prevent such a failure from causing a continuous transmission on the bus and thus rendering it (the bus) unusable for other transmissions.

Fault Management. General term used to describe the detection of intermittent or permanent events that require changes to system structure or operation and the step-by-step sequence to branch to alternate functions, procedures, or equipment use.

Function. The special work done by a subsystem or a software task.

Fundamental Impedance. See Characteristic Impedance.

Fundamental Waveform. Defined in this document to be the original impinging waveform. The waveform that is transmitted.

Gateway. A unit that passes data between two data buses of similar bus type.

Half Duplex. Operation of a data transfer system in either direction over a single line, but not in both directions on that line simultaneously.

Hierarchical Control. A form of distributing all system control in a system, where one level of control is subordinate to a higher level of control.

Hierarchical Network. A description of a physical topology that has both global and local levels of data buses.

Illegal Commands. A valid command that is not implemented in the receiving RT.

Input Threshold Adjustment. Some receivers allow the input voltage thresholds to be adjusted. It may be desirable to adjust the voltage thresholds to alter the noise performance for some special applications. Receivers are generally supplied with the input voltage threshold adjusted for optimum performance, and the range of acceptable threshold values is not wide.

Input-Output (I/O). This term is used to describe both the function of hardware and software to receive and transmit data and the physical hardware section that is the interface between a 1553 interface and subsystems of a remote terminal or bus controller.

Instrumentation. The purpose of the “Instrumentation” bit is to enable the differentiation of Status Words and Command Words, which are otherwise differentiated only by their position in a message.

Intregration. In this handbook, integration refers to the cooperative need for shared information and the means for achieving that cooperation.

Intersymbol Interference (ISI). The effect seen as a pulse in a string of pulses distorting subsequent pulses as a result of being passed through a network that has less bandwidth than the spectrum of the pulses.

ISI. Intersymbol interference (ISI) is the effect seen where a waveform is distorted by passing it through a network which either has less bandwidth than the signal, or is dispersive.

Invalid Command. A command in which the command word fails to meet validation criteria.

Isolation Resistors. Terminals for direct-coupled stubs require two isolation resistors between the terminal output and the bus connection. Their function is to isolate the bus from a terminal that has shorted (i.e., a terminal that, due to some failure, is presenting an abnormally low impedance to the bus).

Linked Lists. In linked list message processing, each message points to the next message to be transmitted. This method makes it easy to insert messages into the middle of a particular minor frame's message stream.

Lossy. In the context of lossy transmission line, the term lossy acknowledges the fact that transmission lines do not have infinite, bandwidth and contribute to frequency shaping of a propagating pulse above and beyond ideal reflective effects.

Main Bus. See bus.

Major Cycle. A period of scheduled time during which all periodic transmissions and computations occur at least once. Major cycles are divided into subcycles called minor cycles.

Manchester-coded Format Encoding and Decoding. Each channel of the digital section contains an encoder/decoder function that deals with the data on a bit and single-word level. Its purpose is to change the data from its Manchester-coded format into the proper digital data format (typically 16-bit parallel) needed by the rest of the terminal (and vice-versa), and to perform error detection for word-level 1553B errors (e.g., bit count errors, Manchester coding errors, etc). There must be a separate decoder for each channel, but there may be only one encoder.

Message. In 1553 terms, a message is a part of an information transfer format, such as 1 to 32 data words. A message may also refer to the entire transmission by both bus controller and responding remote terminal, which includes not only the data words but the overhead. This second usage is more correctly called an information transfer format.

Definition from 1553: "A single message is the transmission of a command word, status word, and data words if they are specified. For the case of a remote terminal to remote terminal (RT to RT) transmission, the message shall include the two command words, the two status words and data words."

Message Stacks. The stack method is the simplest to implement and allows for the implementation of minor and major frames by use of separate stacks for each minor frame. The subsystem processor simply re-initializes the stack pointer to the appropriate stack each time the particular minor frame is to begin.

Minor Cycle. A period of scheduled time during which the most frequently occurring periodic transmission or computation will occur, or a period scheduled for a frequently occurring transmission or computation. Multiple minor cycles may be required to achieve a major cycle. See major cycle.

Mode Code. A means by which the bus controller can communicate with the multipiex-bus-related hardware in order to assist in the management of the information flow.

Mode Command. An information transfer format with the subaddress/mode fieid in the command word set to indicate that the next following field is a mode code. An RT that implements Mode Commands is required to know that a Subaddress/Mode field in a Command Word equal to 00000 or 11111 defines a Mode Command, and that, in this case, the Word Count field is to be treated as the Mode Code rather than the number of words.

Modem. Modulator/Demodulator. In this handbook, this term is used to mean the analog transceiver circuitry used to convert to digital form. It is also used (loosely) to denote a bus interface unit function.

Modulation. The signaling method used to convey data on the data bus.

Multiple-message Terminals. A multiple-message terminal is a processor or sequencer in its own right. This type of terminal only makes sense as a BC, although some multiple-message BCs are capable of being configured to act as RTs upon command from the subsystem or with a discrete signal. It is capable of chaining several messages together, maintaining a schedule of messages required on the bus, and initiating all transfers at the required times and in the required sequence. In system terms, the multiple-message BC would be programmed with a whole minor frame or even major frame at a time.

Multiplex Protocol. See protocol.

Multiplex System Topology. Multiplex system topology is the network of the data bus terminals, the components that comprise the data bus, and the physical arrangement of redundant elements (whether terminals, bus controllers, or bus cables, coupler, or terminators). It includes all terminals and data buses involved in integrating the data buses into the vehicle.

Multiplexing. The transmission of information from several signal sources through one communication system.

Network. Collection of connectors, cable, transformers and resistors used to connect a group of terminals together in order to allow them to communicate. Often used interchangeably with the word bus.

Noise. Noise is mainly due to reflections from impedance discontinuities in the bus network. Another source of noise is electromagnetic interference (EMI) or coupling of signals into the cable from other parts of the system. Both of these types of noise are mostly higher in frequency than the 1553B fundamental frequency of 1 MHz.

This noise and signal distortion can cause multiple zero-crossings to occur in a bit time (1 microsecond) and can also cause a large error in the time of a zero-crossing (a zero-crossing shift error). This could cause the word to be misinterpreted by the decoder. It is most likely that the decoder would detect a Manchester error, which is a bit that does not have opposite values in the two halves of the bit time. Also, if one bit is distorted sufficiently that it is decoded as valid but of the wrong value, the decoder detects this error with the parity bit. Experience has shown that there is little need for filtering of low-frequency noise.

Good performance of the terminal in the presence of noise on the bus depends on input filtering and the proper setting of the input voltage thresholds.

Output Short Circuit Protection. Some devices are protected against short circuits applied to their outputs. This could be used to protect parts in debugging or breadboarding activities. Note that this is somewhat inherent in the design of a current-mode transmitter.

Output Voltage Adjustment. Some transmitters offer adjustable output voltage. This feature could be very useful in the design of test equipment but is of limited usefulness otherwise.

Over-temperature Shutdown. Some devices include a temperature sensor that shuts down the transmitter if it gets too hot. This is to protect the part from damage, so it is desirable. However, this feature increases the cost and may slightly decrease the device reliability.

Partitioning. The method used to divide a complex system or function into manageable size before allocating these smaller pieces to devices to perform the required job.

Periodic. Event(s) recurring at specific time intervals. See aperiodic.

Polling. This is the method of communicating with multiple terminals within a system to determining information transfer priorities or servicing needs. RTs might be polled to determine whether they have aperiodic or high priority messages to transmit, state of health, or capability of accepting bus control.

Protocol. The conventions imposed on serial data to ensure that the receiver correctly interprets the transmitted data; also, the procedures used for initiating messages and responding to them.

Pulse Code Modulation (PCM). The form of modulation in which the modulation signal is sampled, quantized, and coded so that each element of information consists of different types or numbers of pulses and spaces.

Receiver Input Filtering. The input filter is a key element in determining receiver performance. The bus signal is corrupted by the addition of noise, often to the point that it is difficult to decode.

Receivers. The receiver is the terminal element that translates the analog waveform received from the bus into a digital signal of appropriate characteristics (typically differential TTL) for the rest of the terminal. It does no decoding or checking of the signal. A receiver contains an input filter (to remove noise) and a threshold comparator. It produces an output of 1 (i.e., receiver output high and receiver output low) when the plus signal of the 1553 bus is sufficiently greater than its minus signal, an output of 0 when the minus signal of the 1553 bus is sufficiently greater than its plus signal, and both differential outputs high (or low, see 50.3.1.2) when there is no sufficiently large plus or minus signal on the 1553 bus.

RED. A designation applied to: a) all wirelines within the terminals or data routing equipment carrying classified plain language, b) all wirelines between the unencrypted side of on-line cryptographic equipment used and individual subscriber terminal equipment, c) equipment originating or terminating classified plain text language, and d) areas containing these wirelines, equipment, and the interconnecting lines.

Redundancy. The method of replicating a function for the purpose of increasing the reliability of the function. Most RT designs today are dual redundant. The commonly available VLSI parts all support this mode of operation.

Redundant Data Bus. The use of more than one data bus to provide more than one data path between the subsystems (i.e., dual-redundant data bus and tri-redundant data bus).

RED/BLACK. The concept that electrical circuits, components, equipment, systems, etc., which handle classified plain language data in electrical form (RED) be separated from those which handle encrypted or unclassified information (BLACK).

Reflection Coefficient. The ratio of the voltage wave reflected back toward the source over the incident voltage wave at an impedance discontinuity (referred to in this document by its abbreviation CR). The value of the reflection coefficient will be between -1 and +1.

Remote Terminal (RT). RT's are defined in 3.13 of 1553B as "All terminals not operating as the bus controller or as a bus monitor." An RT cannot initiate any data transfer on the bus (like a BC can) and must respond to commands issued by the BC (unlike a bus monitor). It is important to note that an RT cannot initiate information transfers on the bus; only the BC may do this. Each RT has a unique terminal address assigned to it; information may thus be directed to each specific RT.

Retrofitting. The process of updating a system with new or modernized equipment.

Sample Consistency. Relates to the consistency of data in a message. Messages transmitted shall contain only mutually consistent samples of information, (i.e. all parameters shall be of the same sample set).

Sensor. The hardware and software required to perform a specific system function, such as inertial measurement, radar detection.

Service Request Bit. The purpose of this bit is to inform the Bus Controller that the RT wants the Bus Controller to request a particular message to be transmitted from the RT to the BC.

Single-message Terminals. A single-message terminal has enough capability to construct or process a complete message without any action by the subsystem. Subsystem action is required only at the beginning or end of the message or in the event of an error. The subsystem is responsible for processing any errors and interpreting the status word contents, to decide what the next message should be, and then issuing it. This type of terminal is typically used with a microprocessor-based subsystem; the messages to be sent are all constructed by the subsystem processor and placed in defined memory locations (to be read by the terminal via direct memory access (DMA)) or written to registers in the terminal.

Single-word Terminals. In a system with a single-word terminal, the subsystem must process each word in each message individually. That is, a single-word terminal requires subsystem intervention or action for every word. After all the words have been received, the subsystem processor must determine the validity of the message and construct the proper response. The response must then be transferred to the terminal and transmitted one word at a time.

Specification. A document prepared specifically to support procurement that clearly and accurately describes the essential technical requirements for purchased material. Also included are procedures necessary to determine that the requirements have been met for the purchased material covered by the document.

Standard. A military standard is a document that establishes engineering and technical requirements for processes, procedures, practices, and methods that have been adopted as standard.

Status Flags. Specific one bit fields in the status word generated by the RT to indicate its status.

Stub. The connection of a terminal to the main bus, usually kept as short as possible to minimize distortion. May be either director transformer coupled.

Stub Coupling. The method of coupling an RT to the bus. These are generally transformer coupled, but some Navy applications require both transformer and direct coupled stubs (Notice 2).

Subsystem. The subsystem is defined in 3.8 of 1553B as "The device or functional unit receiving data transfer service from the data bus." The subsystem is considered to be the portion of the LRU (line replaceable unit—the entire item of electronics) other than the terminal. In other words, it is the hardware interfacing with the nonbus side of the terminal. See sensor.

System Flag Bit. A status word bit that indicates that there is some fault condition in the subsystem associated with the RT.

Synchronous. Events occurring at specific time intervals. See aperiodic.

System. The interacting assembly of hardware, software, data, personnel, and facilities capable of performing a designated function with specified results.

System Architecture. Includes the externally visible parts of a multiplex system, the internal partitioning of multiplex interfacing elements, and the hardware and software used for data transport and transport control. A multiplex system architecture consists of two major parts: system topology and system control.

System Block Diagram. A graphic presentation of the partitions among functions. The blocks may represent actual parts or maybe schematic representations. In a real system functions may be partitioned among the parts used to implement the design.

System Configuration. A 1553 bus system includes a BC (and possibly one or more backup BCs), one or more RTs (up to a maximum of 31), and zero or more bus monitors (typically not more than one, but could be any number). The BC has control of the system. It initiates messages that transfer data to or from an RT or control the operation of an RT. Each RT receives data sent to it by the BC, transmits to the BC or to another RT the data requested by the BC, or performs the commanded control function. A bus monitor listens to the traffic on the bus and extracts whatever information it has been programmed to extract.

System Control. The part of the architecture that implements the dynamic functioning of the multiplex system. System control methodology is used to implement the protocol required for data transfers, the rules used in achieving media control and the procedures for initialization or startup, normal data bus transfer operations (such as, time synchronization, data security and data integrity), system error and fault management techniques, and bus control mechanization.

TEMPEST. An unclassified short name referring to investigations and studies or compromising emanations. It is sometimes used synonymously for the term “compromising emanations” (e.g. TEMPEST tests, TEMPEST inspections, TEMPEST control plan).

Terminal. The electronic module necessayto interface the data bus with the subsystem and the subsystem with the data bus. Terminals may exist as separate LRUs or be contained within the elements of the subsystem. The unit connects to the end of a stub which may be a transmitter or receiver. This definition allows a terminal to be a totally separate LRU, a circuit card, or a small portion of a circuit card; there is no restriction on the physical partitioning of the system. However, the current trend in technology is for smaller size and fewer parts.

A terminal is either a Bus Controller (BC), a Remote Terminal (RT), or a Bus Monitor. Nothing in 1553B precludes a terminal from including the capability of performing the functions of more than one of these three types of terminals, but a terminal may perform only one function at anyone time.

Terminal Flag Bit. This bit indicates that there is some fault condition in the RT. Remember that the RT is only that portion of the LRU necessary to communicate with the 1553 bus.

Terminal Partitioning. Terminals may have various proportions of their design in hardware, firmware, and software. Typically, an older design, simple terminal would be almost all hardware, while a newer design, complex terminal would consist largely of software or firmware.

Time Division Mulplexing (TDM). The transmission of information from several signal sources through one communication system with different signal samples staggered in time to form a composite pulse train.

Topology. The interconnectivity of the data bus(es) and their associated elements (terminals and controllers) to accomplish the desired data path required by the integration.

Transceivers. Receivers and transmitters are generally packaged together as transceivers.

Transformer. Another major analog component is the isolation transformer. It turns out that, to meet the terminal characteristics that are specified in 1553B, especially the common-mode rejection ratio (CMRR) requirement, an isolation transformer is the most appropriate design choice.

As in the case of the transceiver, transformers are usually bought and not built. There are many available on the market that are specifically designed to work with available transceivers to meet the requirements of 1553B.

Transformer Coupled. A method of connecting a stub to the 1553 data bus that uses a transformer and isolation resistors.

Transmitters. The transmitter is the element in the terminal that outputs waveforms to the bus. It accepts as its input the digital signal from the encoder (typically differential TTL) and produces a signal on the 1553 bus that meets the requirements of 1553. It typically contains two drivers, one for each side of the differential 1553 bus. Each is designed to control the rise and fall times and the waveshape of the outputs. A transmitter also typically contains an inhibit input by which it maybe disabled.

Twisted Shielded Pair. A twisted, shielded pair of wires is used to interconnect the elements of a network (transformers, resistors and connectors). It is the primary constituent of the network and is commonly referred to as cable.

Transmission Coefficient. The ratio of the voltage wave transmitted beyond an impedance discontinuity over the incident voltage wave (referred to as CT in this document). It is the number between 0 and 2.

Waveform Quality. A phrase which addresses the amount of distortion with which a waveform arrives at its destination.

Word. A 1553 word is a sequence of 20 bit times consisting of a 3 bit-time sync, 16 bits of data, and 1 parity bit. This is the word as it is transmitted on the bus; 1553 terminals add the sync and parity before transmission and remove them during reception. Therefore, the nominal word size is 16 bits; most significant bit first. There are three types of words: command, status, and data.

SECTION 130

INDEX

130. INDEX

* U.S. GOVERNMENT PRINTING OFFICE:1989 605-431

(TO DETACH THIS FORM, CUT ALONG THIS LINE.)

STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

(See Instructions – Reverse Side)

1. DOCUMENT NUMBER	2. DOCUMENT TITLE
MIL-HDBK-1553A	Multiplex Applications Handbook

3a. NAME OF SUBMITTING ORGANIZATION	4. TYPE OF ORGANIZATION *(Mark one)*
	☐ VENDOR ☐ USER ☐ MANUFACTURER ☐ OTHER *(Specify)*: _____
b. ADDRESS *(Street, City, State, ZIP Code)*	

5. PROBLEM AREAS

a. Paragraph Number and Wording:

b. Recommended Wording:

c. Reason/Rationale for Recommendation:

6. REMARKS

7a. NAME OF SUBMITTER *(Last, First, MI)* – Optional	b. WORK TELEPHONE NUMBER *(Include Area Code)* – Optional
c. MAILING ADDRESS *(Street, City, State, ZIP Code)* – Optional	8. DATE OF SUBMISSION *(YYMMDD)*

DD FORM 82 MAR 1426 PREVIOUS EDITION IS OBSOLETE. ASD/ENES OVERPRINT, JAN 85

INSTRUCTIONS: In a continuing effort to make our standardization documents better, the DoD provides this form for use in submitting comments and suggestions for improvements. All users of military standardization documents are invited to provide suggestions. This form may be detached, folded along the lines indicated, taped along the loose edge *(DO NOT STAPLE)*, and mailed. In block 5, be as specific as possible about particular problem areas such as wording which required interpretation, was too rigid, restrictive, loose, ambiguous, or was incompatible, and give proposed wording changes which would alleviate the problems. Enter in block 6 any remarks not related to a specific paragraph of the document. If block 7 is filled out, an acknowledgement will be mailed to you within 30 days to let you know that your comments were received and are being considered.

NOTE: This form may not be used to request copies of documents, nor to request waivers, deviations, or clarification of specification requirements on current contracts. Comments submitted on this form do not constitute or imply authorization to waive any portion of the referenced document(s) or to amend contractual requirements.

(Fold along this line)

(Fold along this line)

DEPARTMENT OF THE AIR FORCE
ASD/ENES
Wright-Patterson AFB OH 45433-6503

NO POSTAGE NECESSARY IF MAILED IN THE UNITED STATES

OFFICIAL BUSINESS
PENALTY FOR PRIVATE USE $300

BUSINESS REPLY MAIL
FIRST CLASS PERMIT NO. 73230 WASHINGTON D. C.
POSTAGE WILL BE PAID BY THE DEPARTMENT OF THE AIR FORCE

ASD/ENES
Wright-Patterson AFB OH 45433-6503